Ordering number : ENN6124

CMOS IC

LC73815M

FSK 1200 Baud Modem and DTMF Receiver

Overview

The LC73815M is a telephone IC that integrates on a single chip both an FSK modem, which receives pre-call reporting services such as caller ID and performs other data send/receive functions, and a DTMF receiver circuit that can handle remote control functions for telephone answering machine applications.

Applications

Pre-call reporting services, such as Caller ID, reception, other data send/receive functions, and remote control of telephone answering machine applications.

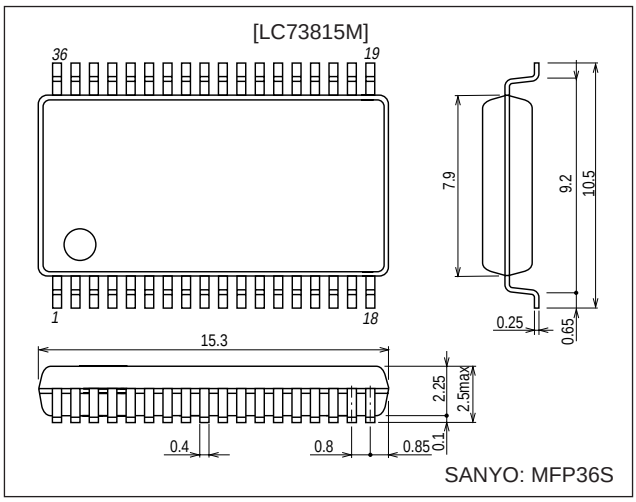
Features

- FSK modem (1200 bps)
- Circuit that automatically generates the start and stop bits used during FSK modulation
- Circuit that automatically generates the continuous mark signal at the start of transmission in FSK modulation mode
- Circuit that automatically inserts the idle bits (5 or more bits) used in FSK modulation mode
- Built-in clock synchronous I/O shift register
- Detection of all 16 DTMF signals
- Digital guard timer circuits for the DTMF signal detection signal pins
- Operating voltage range: 4.5 to 5.5 V
- Low-power mode that can contribute to energy savings
- 36-pin package (MFP-36S)

Package Dimensions

unit: mm

3129-MFP36S



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Maximum input voltage	V_{IN} max		–0.3 to V_{DD} + 0.3	V
Maximum input current	I_{IN} max		–10 to +10	mA
Allowable power dissipation	Pd max	Ta ≤ 70°C	250	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

SANYO Electric Co.,Ltd. Semiconductor Company

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

D2200RM (OT) No. 6124-1/17

Allowable Operating Ranges at Ta = –30 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Operating current drain	I_{DD}(OP1)	V_{DD} = 5.0 V, when the DTMF receiver is used.		5.5	10	mA
	I_{DD}(OP2)	V_{DD} = 5.0 V, during FSK reception		7.5	15	mA
	I_{DD}(OP3)	V_{DD} = 5.0 V, during FSK transmission		7.5	15	mA
Quiescent current	I_{DD}(ST)	$\overline{RES}$ pin = low			10	µA
Oscillator frequency	f_{OSC}		3.5757965	3.579545	3.583125	MHz

DC Electrical Characteristics at Ta = 25°C, V_{DD} = 5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level input voltage	V_{IH}	Pins other than ACK and $\overline{RES}$	0.7 V_{DD}			V
	V_{IHS}	The ACK and $\overline{RES}$ input pins	0.8 V_{DD}			V
Low-level input voltage	V_{IL}	Pins other than ACK and $\overline{RES}$			0.3 V_{DD}	V
	V_{ILS}	The ACK and $\overline{RES}$ input pins			0.2 V_{DD}	V
Input leakage current	V_{IH}	V_{IN} = V_{DD}			10	µA
	I_{IL}	V_{IN} = GND	–10			µA
High-level output current	I_{OH}	V_{OUT} = V_{DD} – 0.4 V		–0.8	–0.4	mA
Low-level output current	I_{OL}	V_{OUT} = 0.4 V	1.0	2.5		mA

AC Electrical Characteristics 1 (FSK reception/transmission) at Ta = 25°C, V_{DD} = 5 V, V_{SS} = 0 V, f_{OSC} = 3.579545 MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input signal detection level		FSK reception	–38		+3	dBm
Reception data transmission speed		FSK	1188	1200	1212	baud
Reception frequency		FSK (Mark)	1180	1250	1320	Hz
		FSK (Space)	2070	2150	2280	Hz
Shift register data shift speed	f_{ACK}				1	MHz
	t_{CKL}		500			ns
	t_{CKH}		500			ns
External oscillator input	EXTOI		0.5			Vrms
FSK transmission frequency	B/$\overline{V}$ = H	FSK (Mark)		1200		Hz
	(BELL202)	FSK (Space)		2204		Hz
	B/$\overline{V}$ = L	FSK (Mark)		1300		Hz
	(V.23)	FSK (Space)		2101		Hz
FSK output amplitude			0.5	0.8		Vp-p
Transfer rate				1200		bps
FSK modulation delay time	t_{DDEM}	See the timing chart.	0	0.83		ms
Data output setup time	t_{SDATA}	See the timing chart.	0	0.42	0.83	ms
DR output setup time	t_{SDR}	See the timing chart.		2.2	3.3	µs
ACK - DATA setup time	t_{SCKD}	See the timing chart.	0		300	ns
ACK - DR setup time	t_{SCKDR}	See the timing chart.	1.1		9.0	µs

Conditions: For the dBm ratings, 0 dBm is defined to be a 1 mW output into a 600 Ω load.

AC Electrical Characteristics 2 (DTMF reception) at Ta = 25°C, V_{DD} = 5 V, V_{SS} = 0 V, f_{OSC} = 3.579545 MHz

Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Input signal detection level			1, 2, 3, 5, 6, 9	–45		+0	dBm
Allowable twist			2, 3, 6, 9, 11		±10		dB
Frequency detection band			2, 3, 5, 9	±1.5% ±2 Hz			
Frequency non-detection band			2, 3, 5	±3.5			%
Allowable third tone			2, 3, 4, 5, 9, 10		–16		dB
Allowable dial tone			2, 3, 4, 5, 8, 9, 10		22		dB
Allowable noise			2, 3, 4, 5, 7, 9, 10		–12		dB
Input signal invalid time		$t_{\overline{REC}}$	See the timing chart.			20	ms
Input signal valid time		t_{REC}	See the timing chart.	45			ms
Interdigit pause invalid time		t_{DO}	See the timing chart.			20	ms
Interdigit pause valid time		t_{ID}	See the timing chart.	40			ms
Guard time	(Present)	t_{GDP}	See the timing chart.		30		ms
	(Absent)	t_{GDA}	See the timing chart.		20		ms
Input signal detection time	(Present)	t_{DP}	See the timing chart.	3		20	ms
	(Absent)	t_{DA}	See the timing chart.	0.5		20	ms

Conditions
1. The 0 dBm level is defined to be a 1 mW output into a 600 Ω load.
2. All combinations of the 16 DTMF signals.
3. A 40 ms DTMF signal period, and a 40 ms pause period
4. The nominal frequencies are used for DTMF signals.
5. The signal levels of the low group and high group signals are identical.
6. The tolerance for DTMF signal frequency is within ±1.5% or ±2 Hz.
7. Gaussian noise with a band of 0 to 3 kHz
8. Dial tone pair of 350 and 440 Hz
9. The error ratio is under 1 error in 10,000 operations.
10. Referenced to the frequency component with the lowest level in the DTMF signal.
11. Twist: the ratio of the high group tone level to the low group tone level

Note: This IC contains a Switched Capacitor Filter (SCF) circuit on chip.

Since the internal SCF clock frequency is OSC/56 (= 63.92 kHz), a power supply related noise whose frequency is OSC/56 multiplied by some integer ±3 kHz will prevent the ratings shown above from being achieved.

Therefore, care must be taken for the power supply related noise.

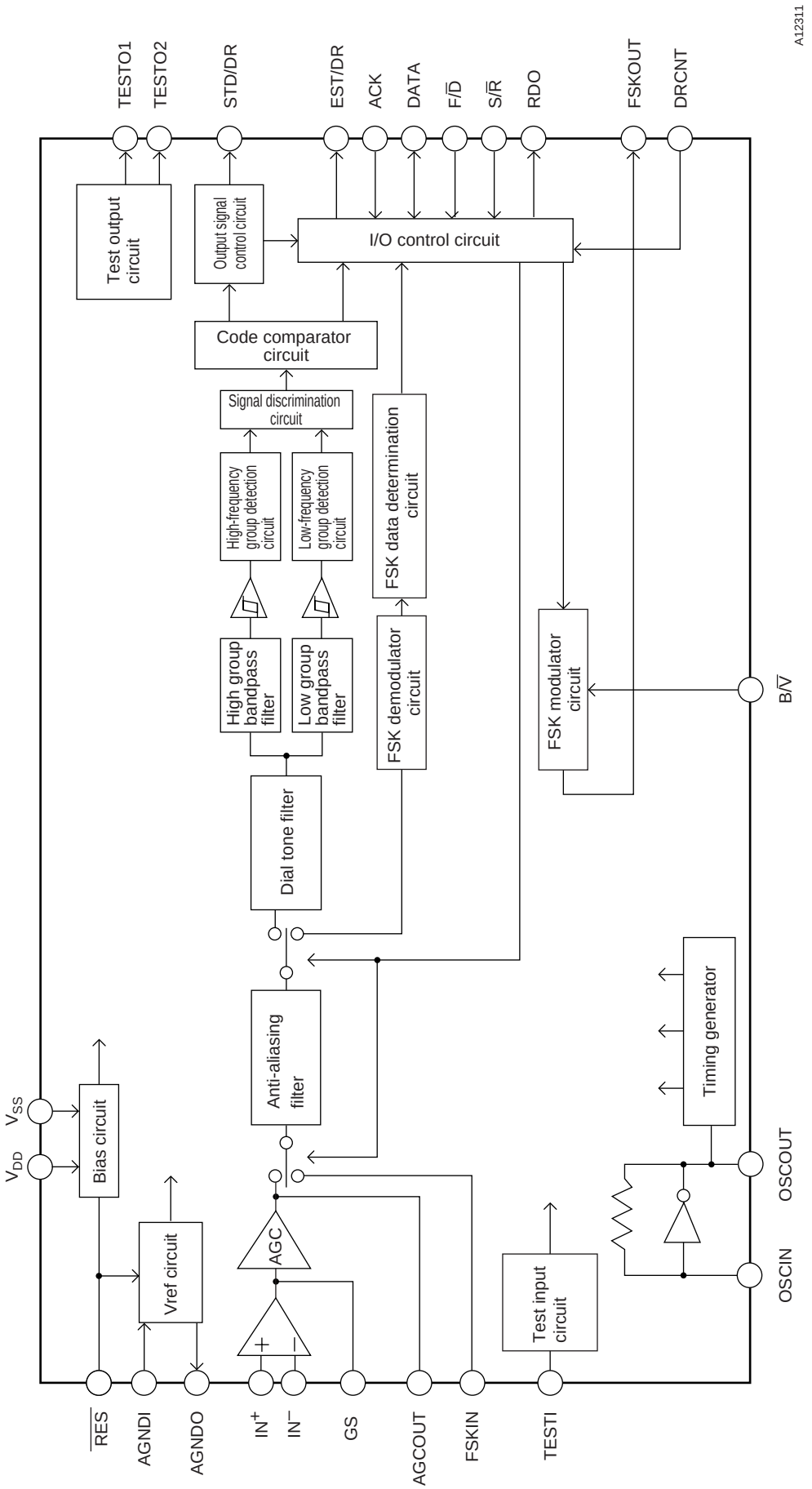
Input Amplifier Characteristics at Ta = 25°C, V_{DD} = 5 V, V_{SS} = 0 V, f_{OSC} = 3.579545 MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input offset voltage	V_{IO}		–25		+25	mV
Input offset current	I_{IO}	$V_{SS} \le V_{IN} \le V_{DD}$		±100		nA
Power supply rejection ratio	PSRR	1 kHz		60		dB
Common-mode rejection ratio	CMRR			60		dB
Open loop voltage gain	AO			65		dB
0 dB bandwidth	f_T			1.5		MHz
Maximum output voltage	V_O	$R_L \ge 100$ kΩ		$V_{DD} - 0.5$		Vp-p
Allowable load capacitance	C_L			100		pF
Allowable load resistance	R_L			50		kΩ
Common-mode input voltage range	V_{CM}	No load		3.0		Vp-p

Pin Functions

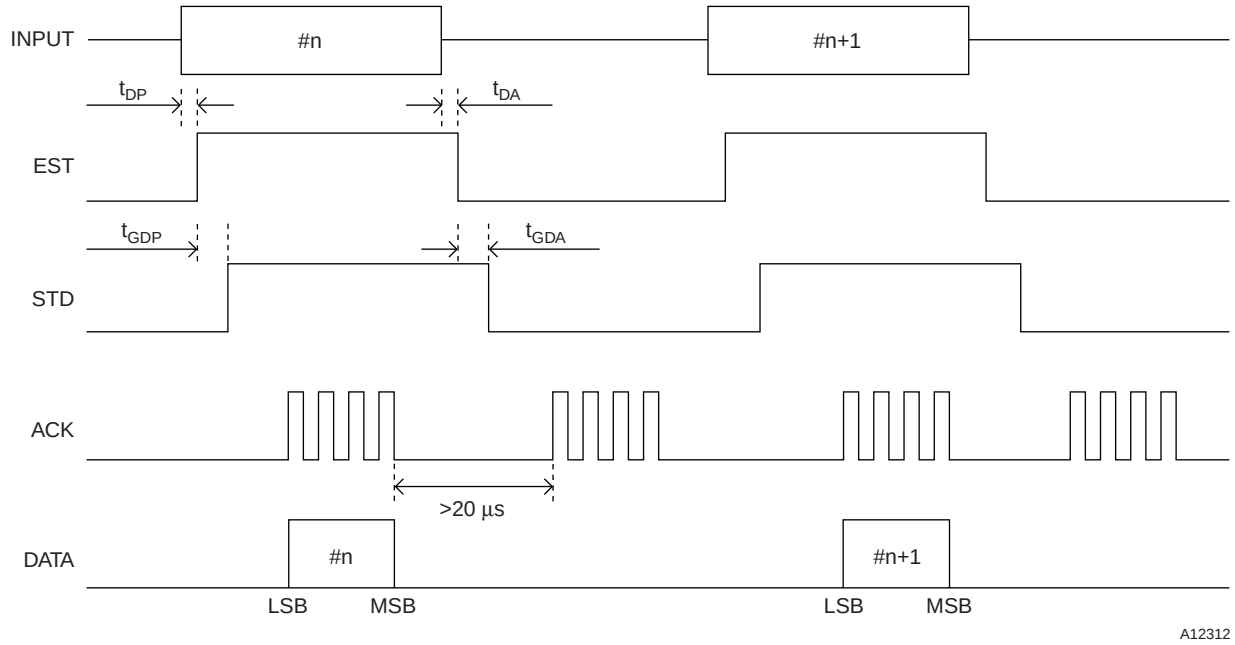
Pin No.	Pin	I/O	Function
1	IN^+	I	Differential operational amplifier noninverting input
2	IN^-	I	Differential operational amplifier inverting input
3	GS	O	Differential operational amplifier output
4	AGND	O	IC internal analog ground output
5	NC		
6	FSKOUT	O	FSK signal output. This is an npn transistor emitter-follower output.
7	AGCO	O	Connect to pin 8 through a capacitor. Make no other connections to this pin.
8	FSKIN	I	Connect to pin 7 through a capacitor. Make no other connections to this pin.
9	NC		
10	AGND	I	IC internal analog ground input
11	NC		
12	TESTI	I	IC test input. This pin must be tied low during normal operation.
13	B/$\overline{V}$	I	Transmission FSK frequency switching input (Bell 202, V.23) High: Bell 202, Low: V.23
14	NC		
15	OSCIN	I	Connect a 3.579545 MHz oscillator element between these pins. An external 3.579545 MHz may also be supplied. (Consult oscillator element manufacturers concerning the combination of their products with this IC.)
16	OSCOUT	O	
17	NC		
18	V_{SS}		Ground
19	V_{DD}	I	Power supply. Connect a capacitor of at least 0.1 µF between this pin and GND.
20	NC		
21	S/$\overline{R}$	I	FSK send/receive mode switching input. High: Send, Low: Receive.
22	F/$\overline{D}$	I	FSK modem/DTMF receiver operating mode switching input. High: FSK modem, Low DTMF receiver.
23	NC		
24	DATA	I/O	Serial output of the FSK or DTMF received data in synchronization with the ACK input pin. Also used for serial input of FSK transmission data.
25	ACK	I	Synchronization clock input for serial data readout and write.
26	EST/DR	O	In DTMF receiver mode (EST), a high level indicates the presence of a valid DTMF signal. Monitor this pin (or the STD pin), and, after an appropriate wait period has passed, read out the data by applying four pulses to the ACK pin. Note that the received DTMF data is latched internally to the IC on the rising edge of this pin. In FSK reception mode (DR), this pin outputs a high level when the received data is valid, and goes low after the received data has been read out by applying pulse inputs to the ACK pin. In FSK transmission mode (DR), this pin indicates the input ready state for transmission data. A high level indicates that the IC is ready to accept the input of transmission data.
27	STD/DR	O	In DTMF receiver mode (STD), a high level indicates the presence of a valid DTMF signal. The rise of this signal occurs later than that of the EST signal. However, this signal is not sensitive to burst waveforms. In FSK mode, this pin functions identically to pin 26.
28	RDO	O	FSK demodulated signal output
29	$\overline{RES}$	I	Reset input. Apply a low level to this pin when power is first applied and after low-power mode. At least 1 µs of low-level input is required for the reset operation.
30	DRCNT	I	This input controls DR during FSK reception. DR is invalid if this input is high in FSK reception mode. If this pin is low (note that it is pulled down internally) DR is enabled. This pin also functions to select continuous mark signal generation at the start of transmission mode in FSK transmission mode. Low: If the S/$\overline{R}$ pin is high, continuous mark signals are generated automatically. FSK data will be output following the continuous mark signals generated after the CPU inputs another FSK data to this pin. High: FSK is not output until the CPU inputs the next FSK data, even if the S/$\overline{R}$ pin is set high.
31	TEST01	O	IC test output pin
32, 33	NC		
34	TEST02	O	IC test output pin
35, 36	NC		

Block Diagram

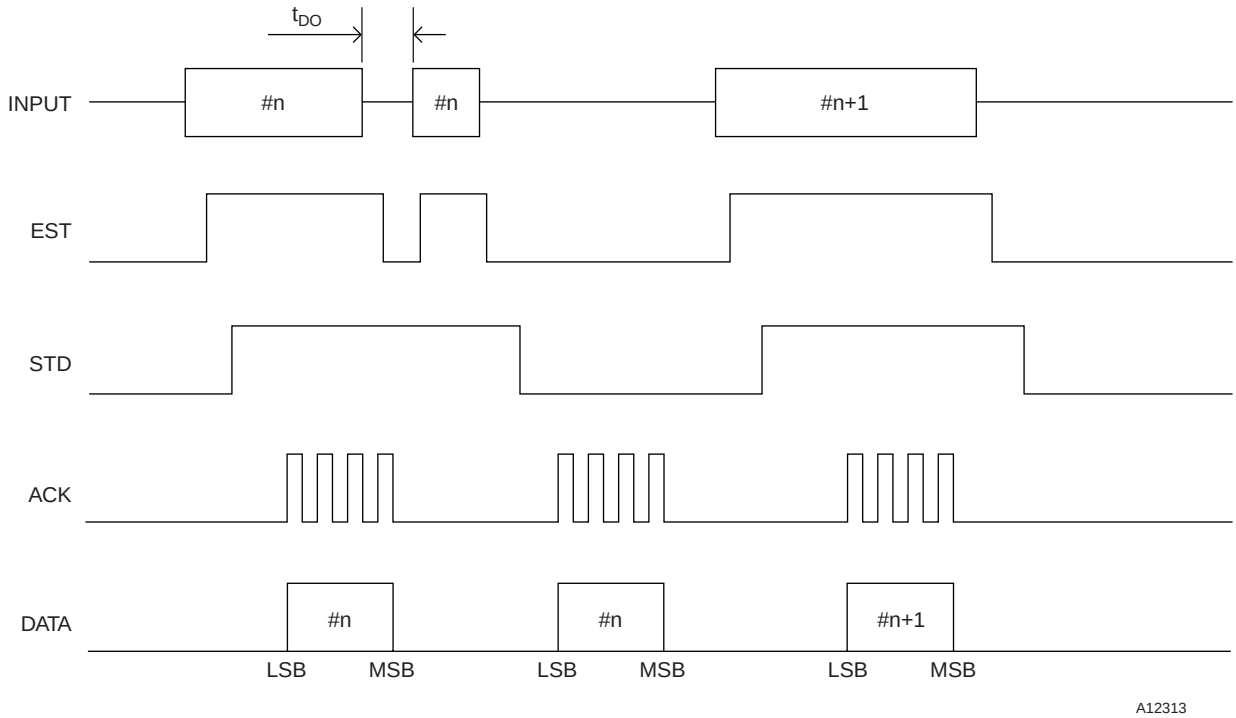


Timing Chart (DTMF mode)

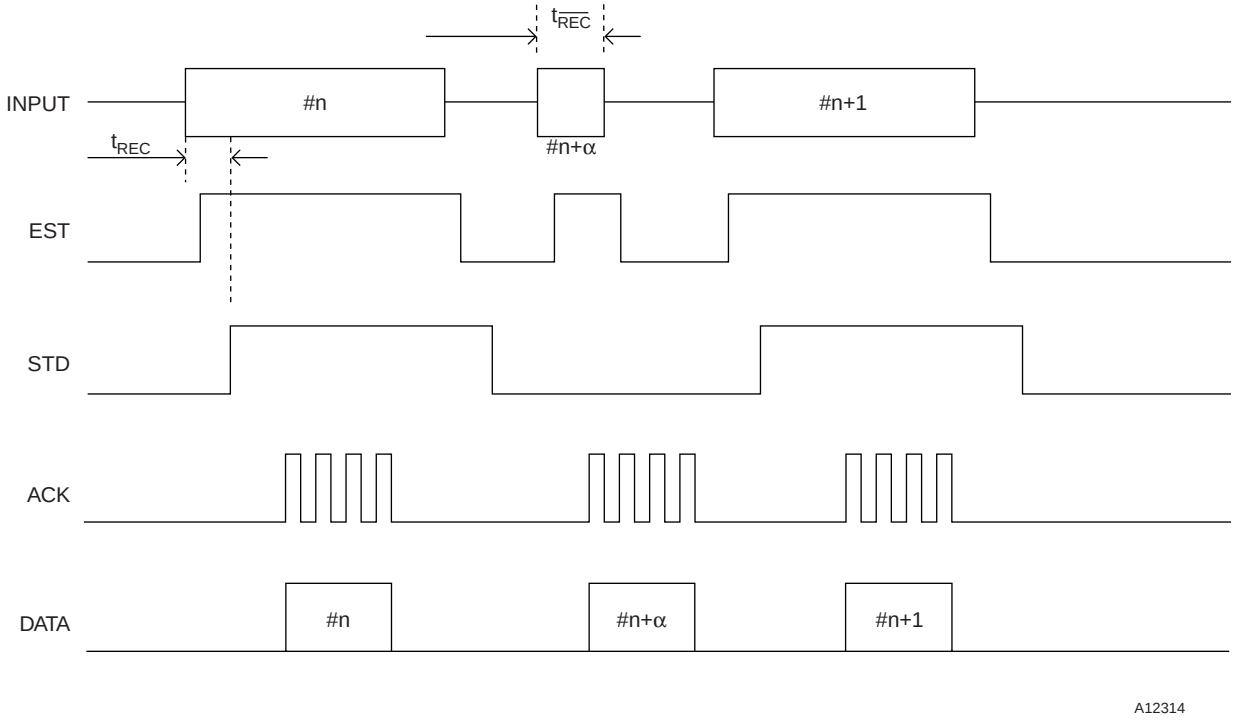
Timing chart for the normal state (when DTMF signal #n and #n+1 have been input.)



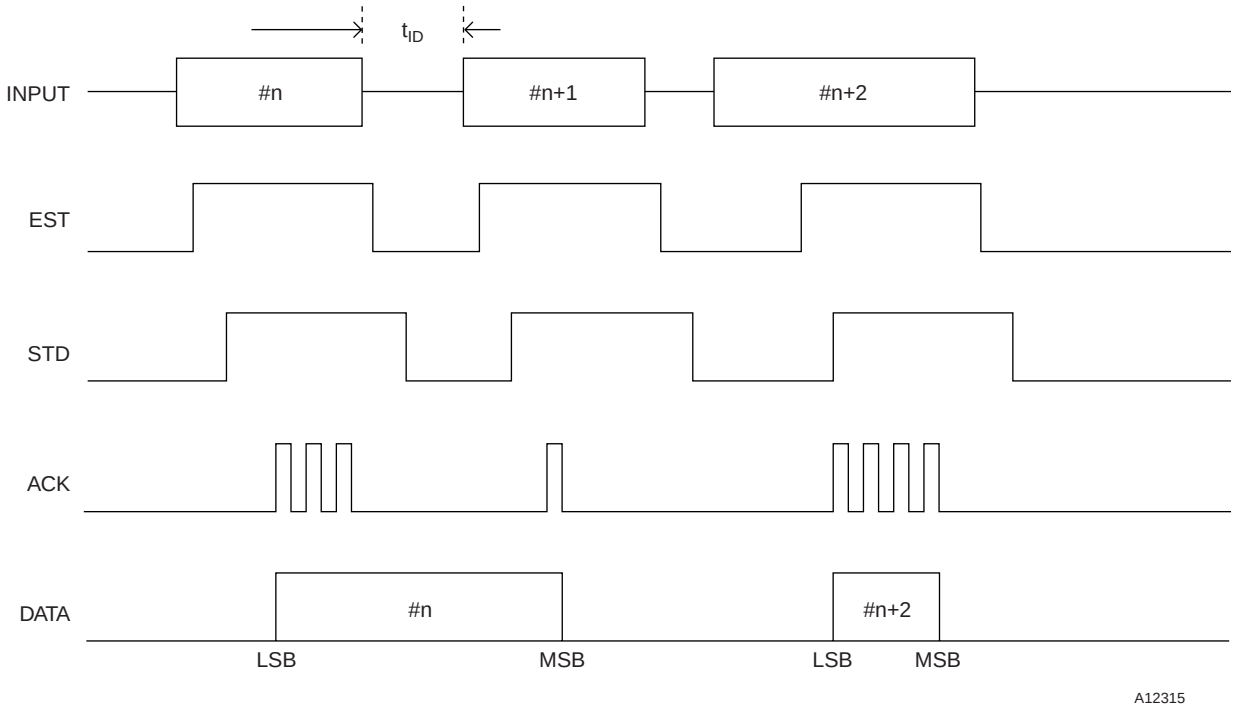
When a DTMF signal (#n) is separated into two events due to a burst waveform or other problem.



When a pseudo-DTMF signal consisting of noise (#n + α) is input.

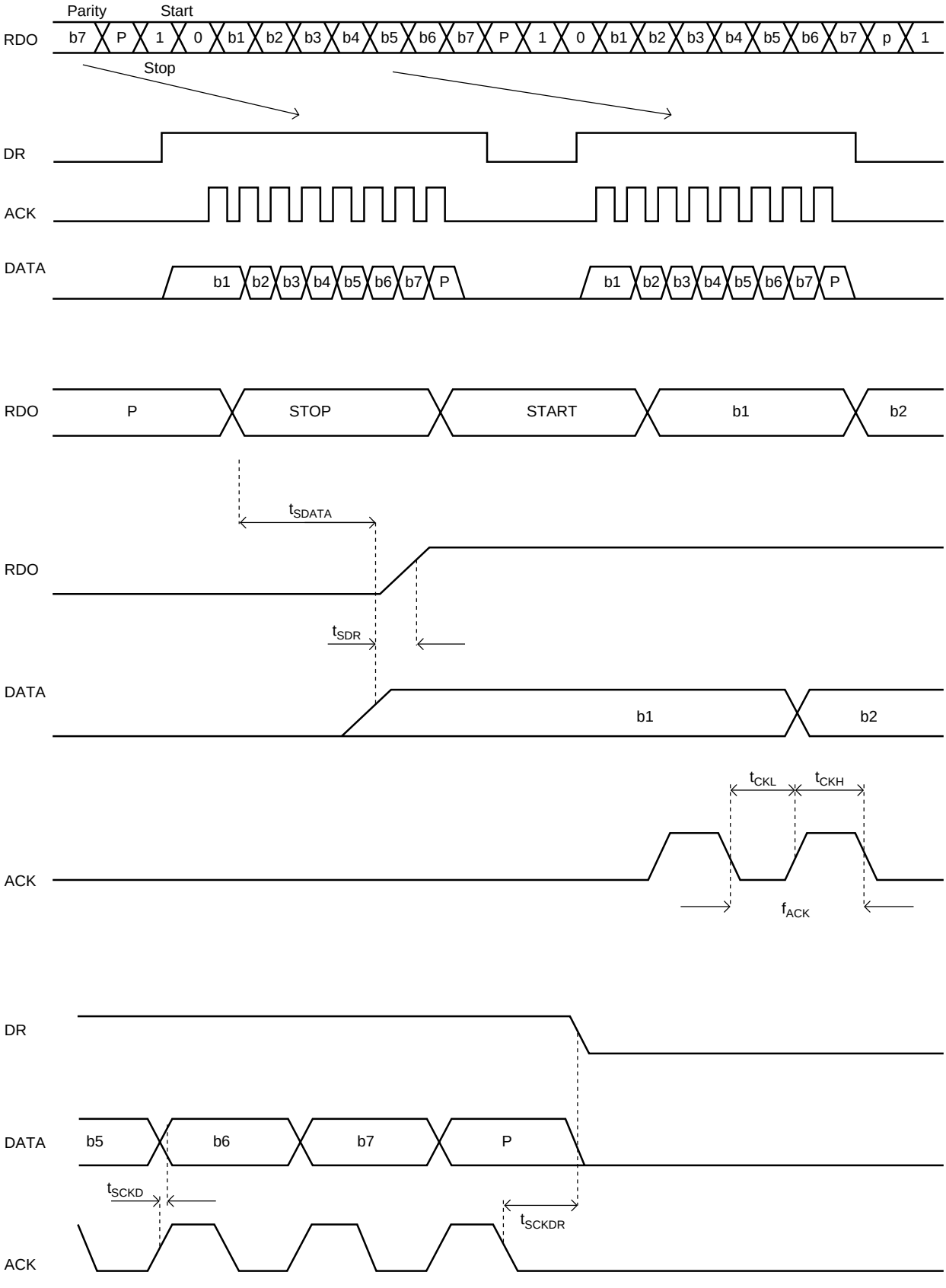


When the output data is incorrect due to displacement of the input clock

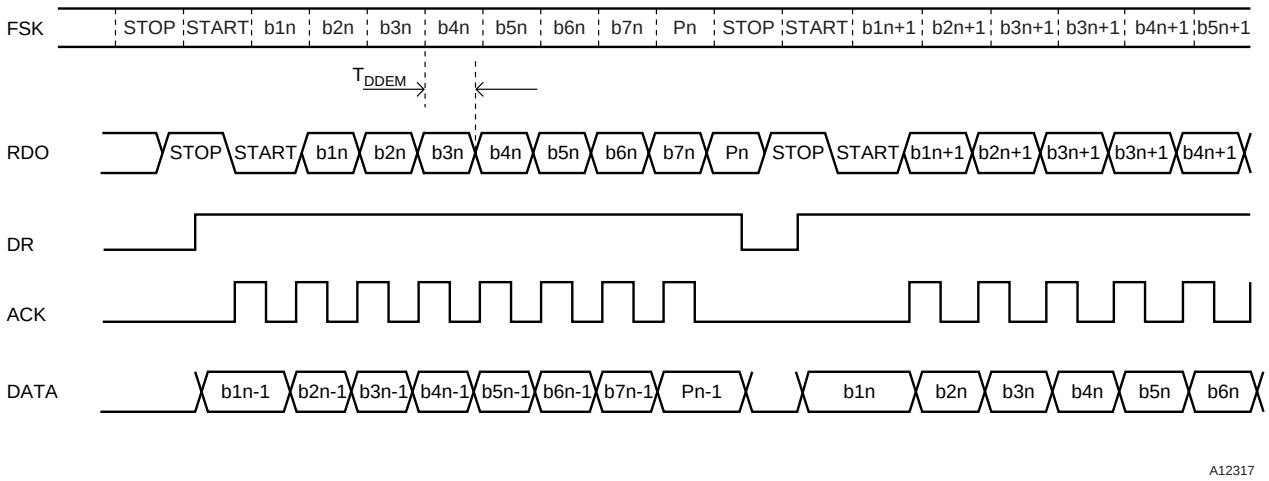


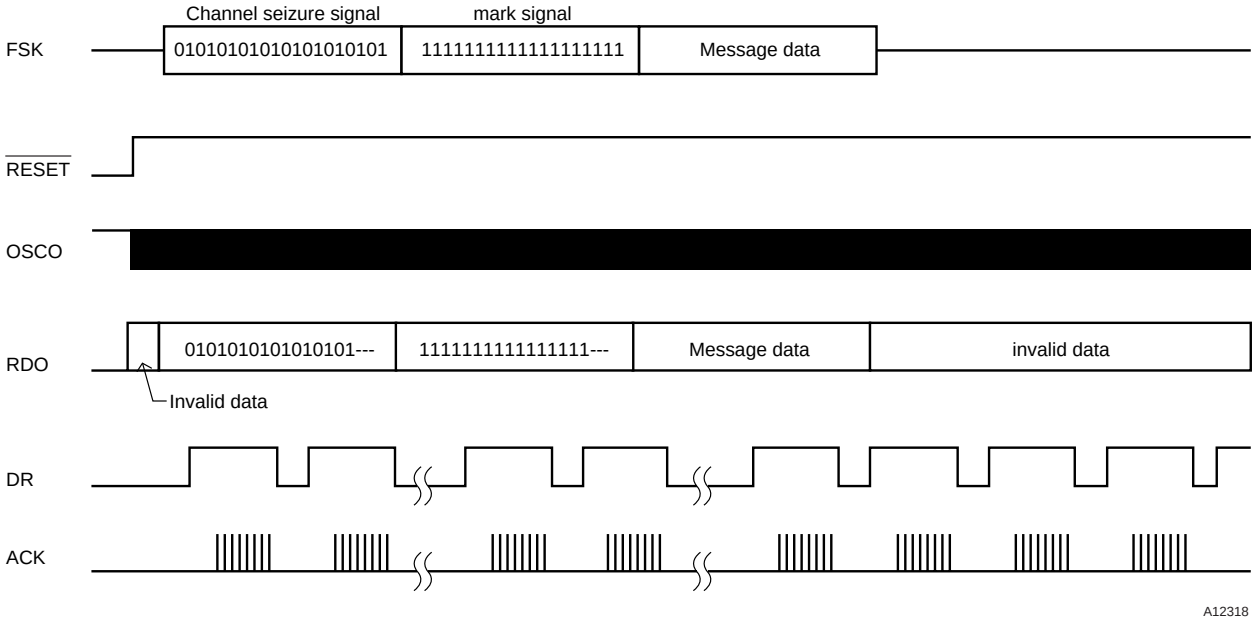
Note: The output data is output from the DATA pin in response to four pulses applied as a set to the ACK pin. The output data are composed of four ACK pulses.There must be a wait time of at least 20 μs between the last of these 4 ACK pulses and the next ACK pulse.

Timing Chart (FSK mode reception)

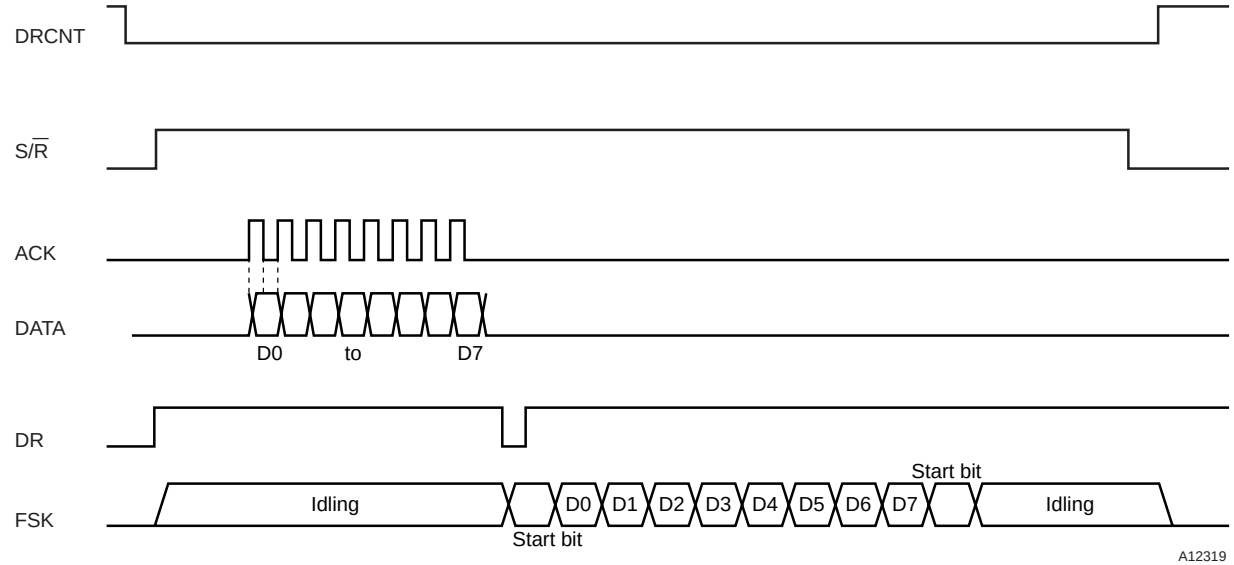


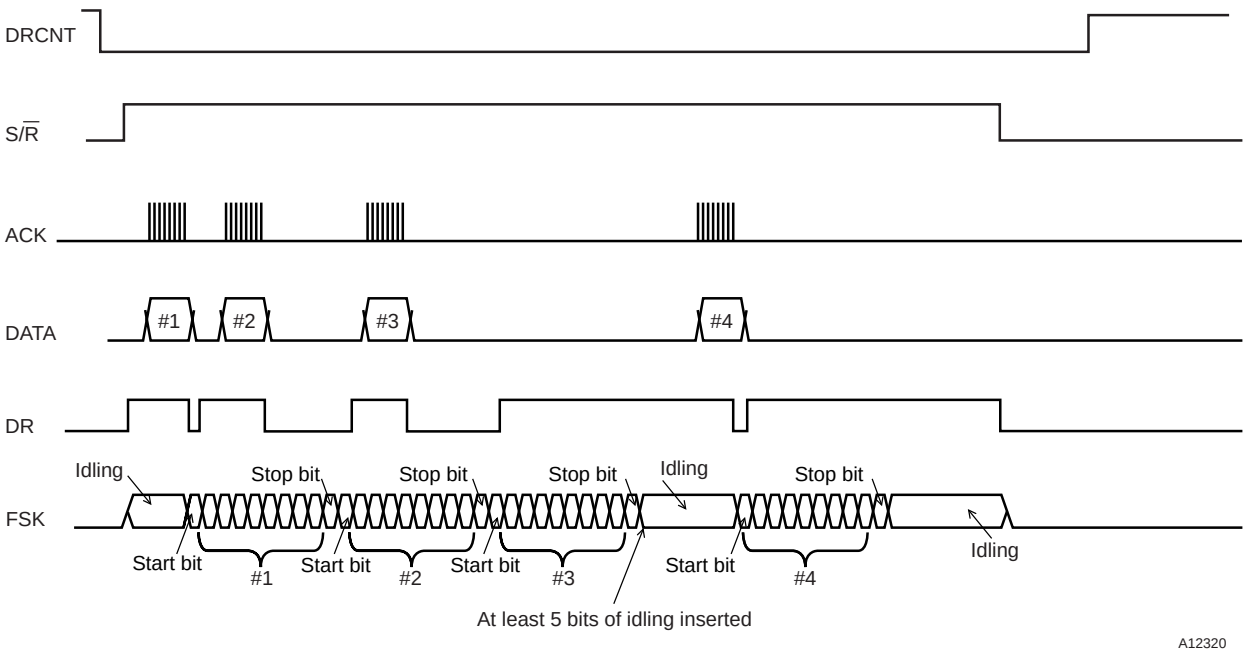
A12316

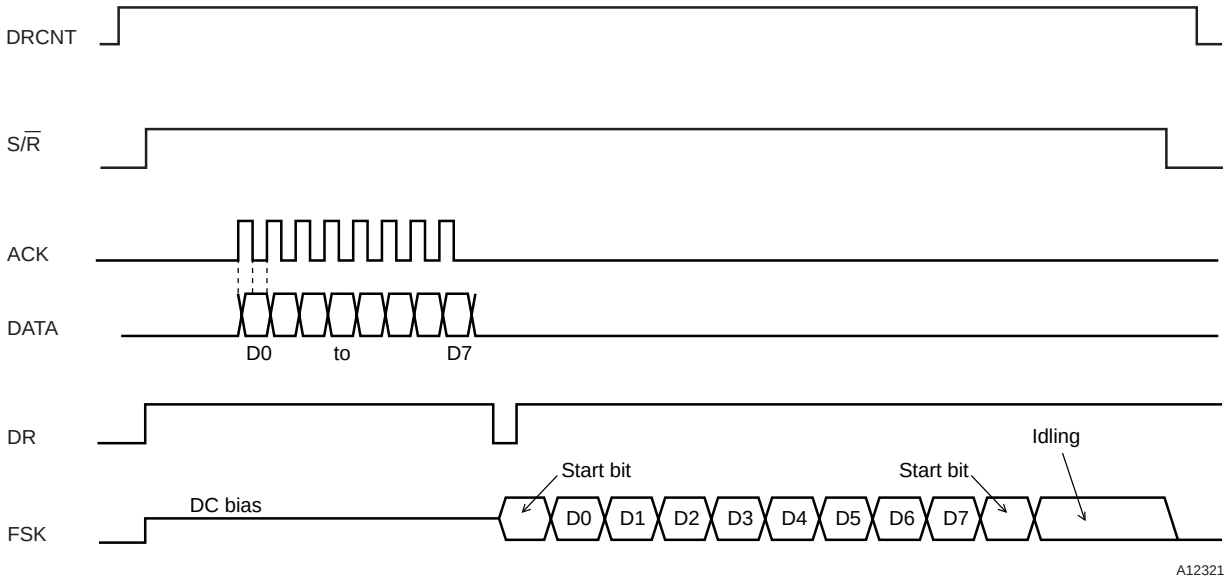

FSK
STOP START b1n b2n b3n b4n b5n b6n b7n Pn STOP START b1n+1 b2n+1 b3n+1 b3n+1 b4n+1 b5n+1
T_{DDEM}
RDO
STOP START b1n b2n b3n b4n b5n b6n b7n Pn STOP START b1n+1 b2n+1 b3n+1 b3n+1 b4n+1
DR
ACK
DATA
b1n-1 b2n-1 b3n-1 b4n-1 b5n-1 b6n-1 b7n-1 Pn-1 b1n b2n b3n b4n b5n b6n
A12317

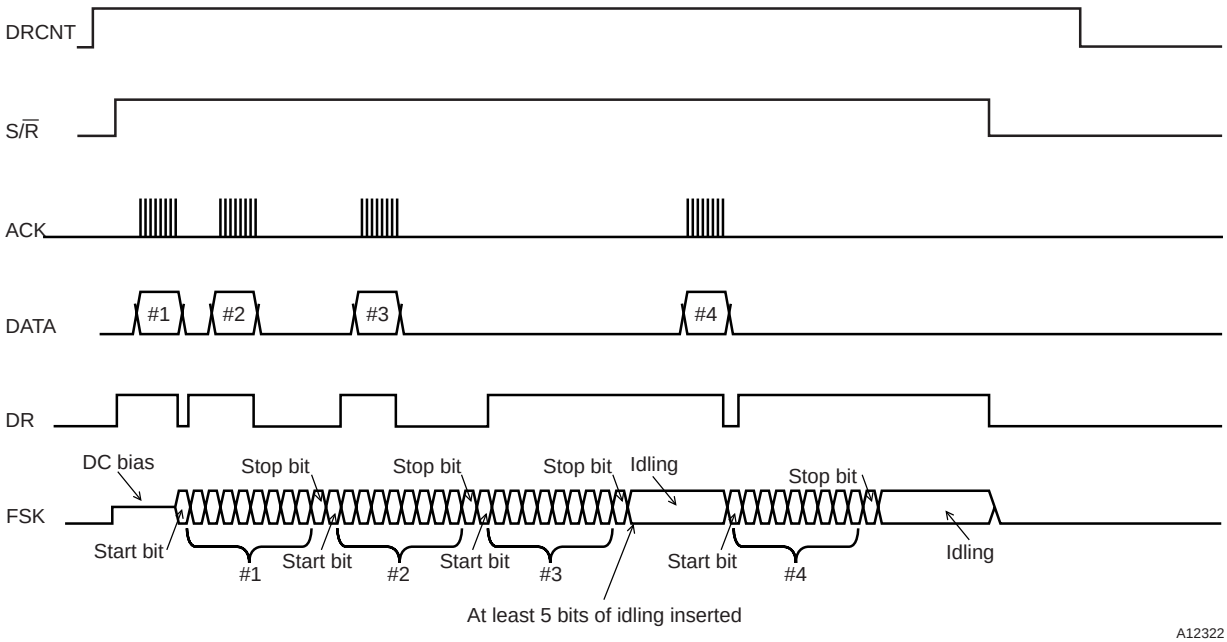

Channel seizure signal
mark signal
FSK
01010101010101010101
11111111111111111111
Message data
RESET
OSCO
RDO
0101010101010101---
1111111111111111---
Message data
invalid data
Invalid data
DR
ACK
A12318

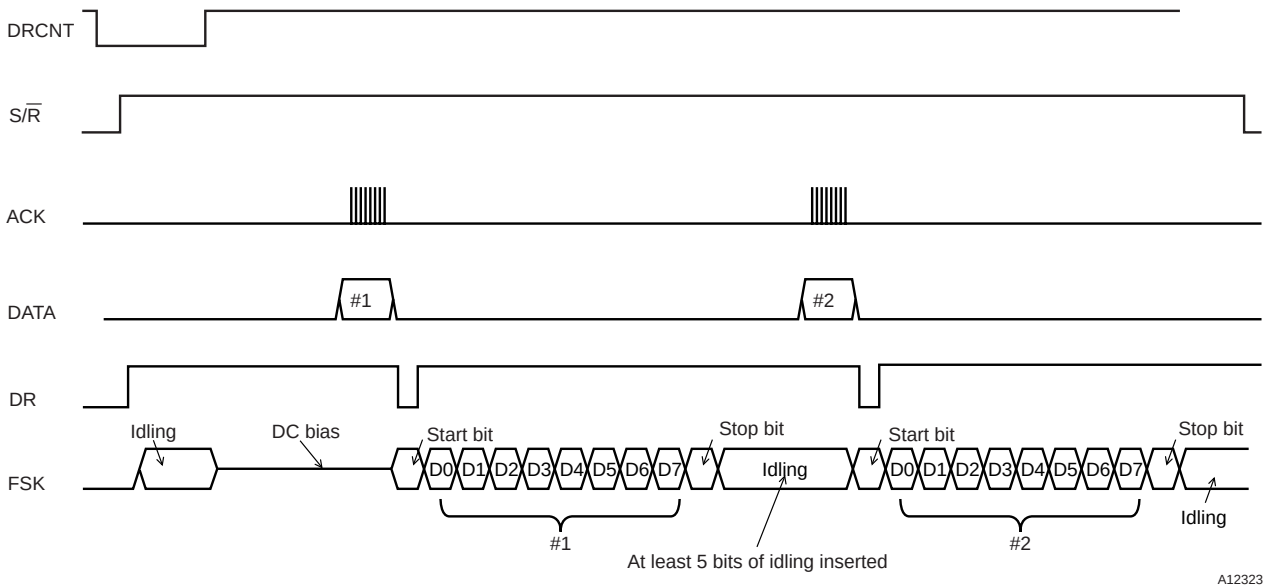
Timing Chart (FSK mode transmission)

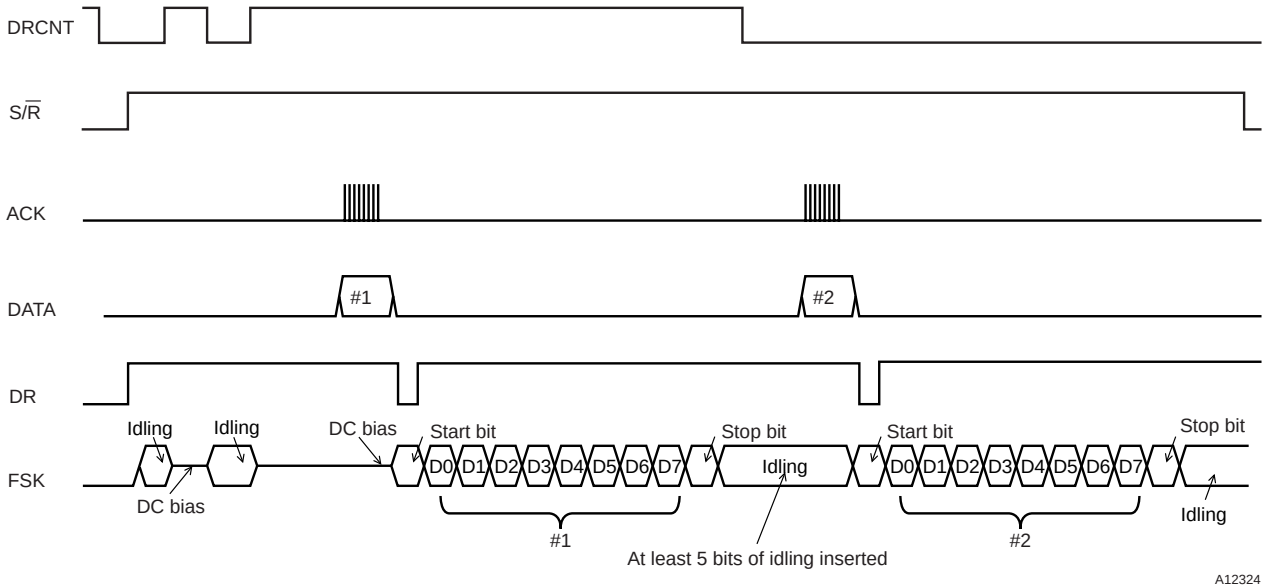




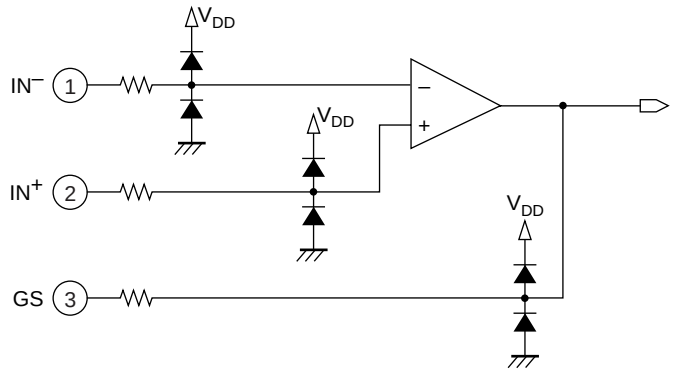
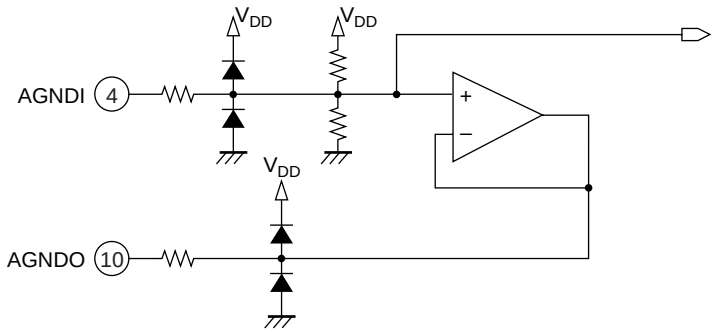
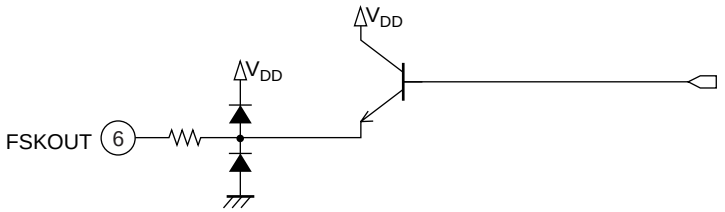
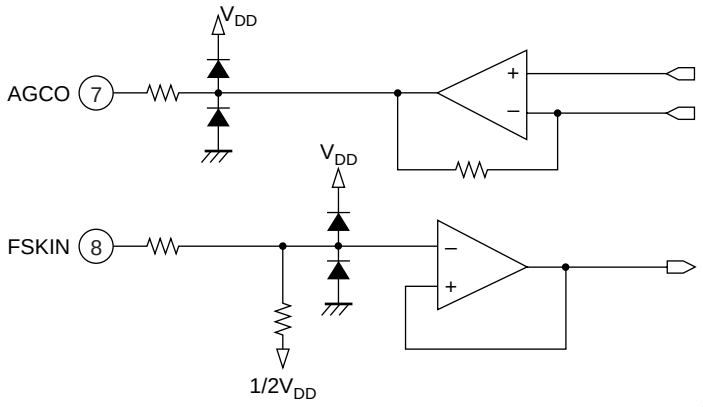
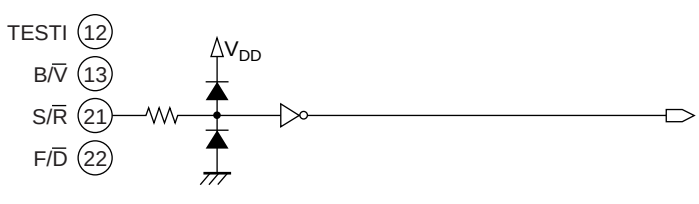

DRCNT
S/R
ACK
DATA
D0
to
D7
DR
Idling
Start bit
Start bit
DC bias
FSK
D0
D1
D2
D3
D4
D5
D6
D7
A12321


DRCNT
S/R
ACK
DATA
#1
#2
#3
#4
DR
DC bias
Stop bit
Stop bit
Stop bit
Idling
Stop bit
FSK
Start bit
#1
Start bit
#2
Start bit
#3
Start bit
#4
Idling
At least 5 bits of idling inserted
A12322


DRCNT
S/R
ACK
DATA
#1
#2
DR
Idling
DC bias
Start bit
Stop bit
Start bit
Stop bit
FSK
D0 D1 D2 D3 D4 D5 D6 D7
Idling
D0 D1 D2 D3 D4 D5 D6 D7
Idling
#1
#2
At least 5 bits of idling inserted
A12323


DRCNT
S/R
ACK
DATA
#1
#2
DR
Idling
Idling
DC bias
Start bit
Stop bit
Start bit
Stop bit
FSK
DC bias
D0 D1 D2 D3 D4 D5 D6 D7
Idling
D0 D1 D2 D3 D4 D5 D6 D7
Idling
#1
#2
At least 5 bits of idling inserted
A12324

Pin Internal Connection

Pin No.	Pin	Internal connection
1 2 3	IN^+ IN^- GS	
4 10	AGNDI AGNDO	
6	FSKOUT	
7 8	AGCO FSKIN	
12 13 21 22	TESTI B/$\overline{V}$ S/$\overline{R}$ F/$\overline{D}$	

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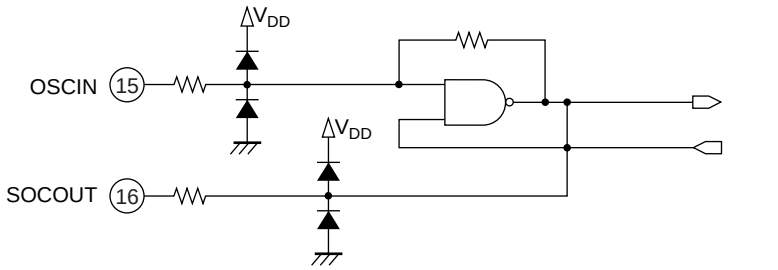
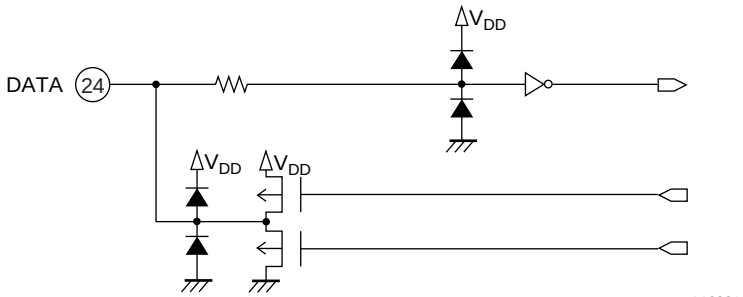
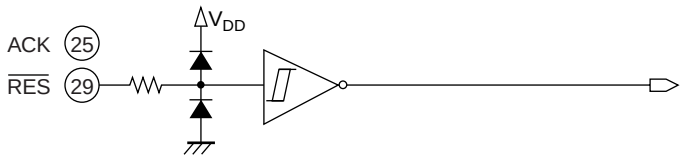
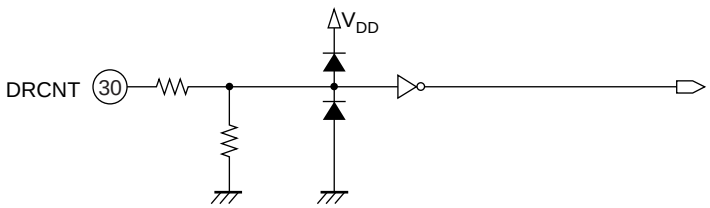
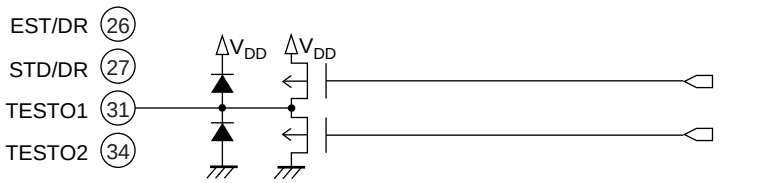
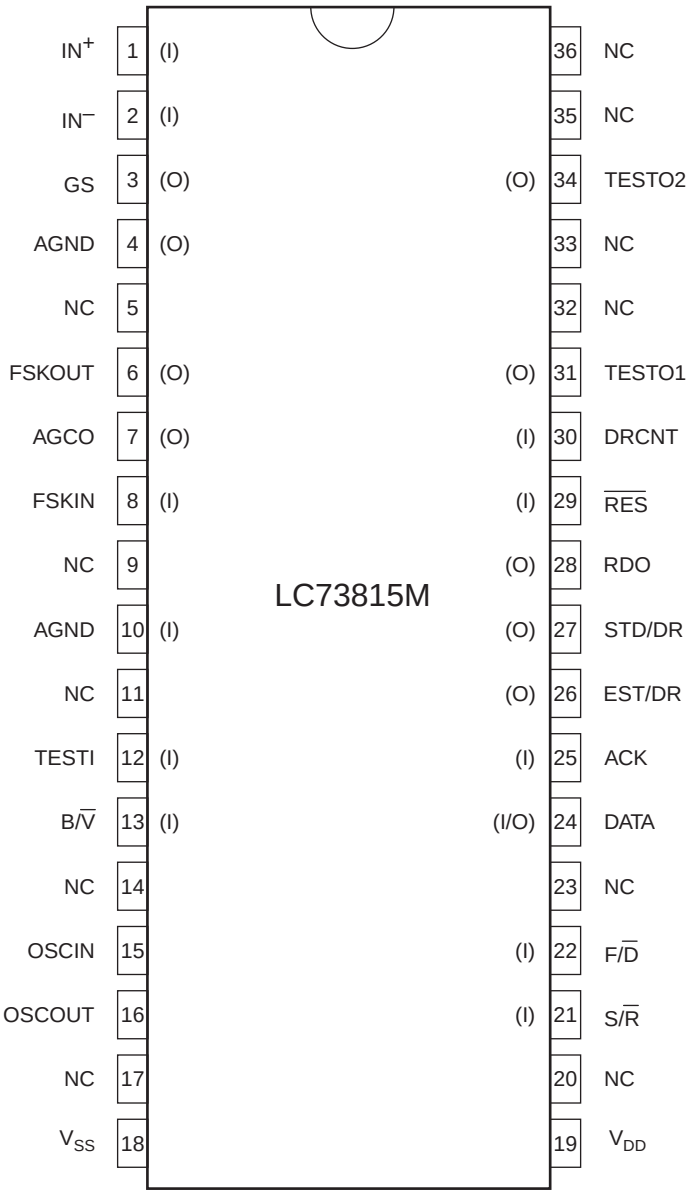
Pin No.	Pin	Internal connection
15 16	OSCIN OSCOUT	
24	DATA	
25 29	ACK $\overline{\text{RES}}$	
30	DRCNT	
26 27 31 34	EST/DR STD/DR TESTO1 TESTO2	

Pin Assignment

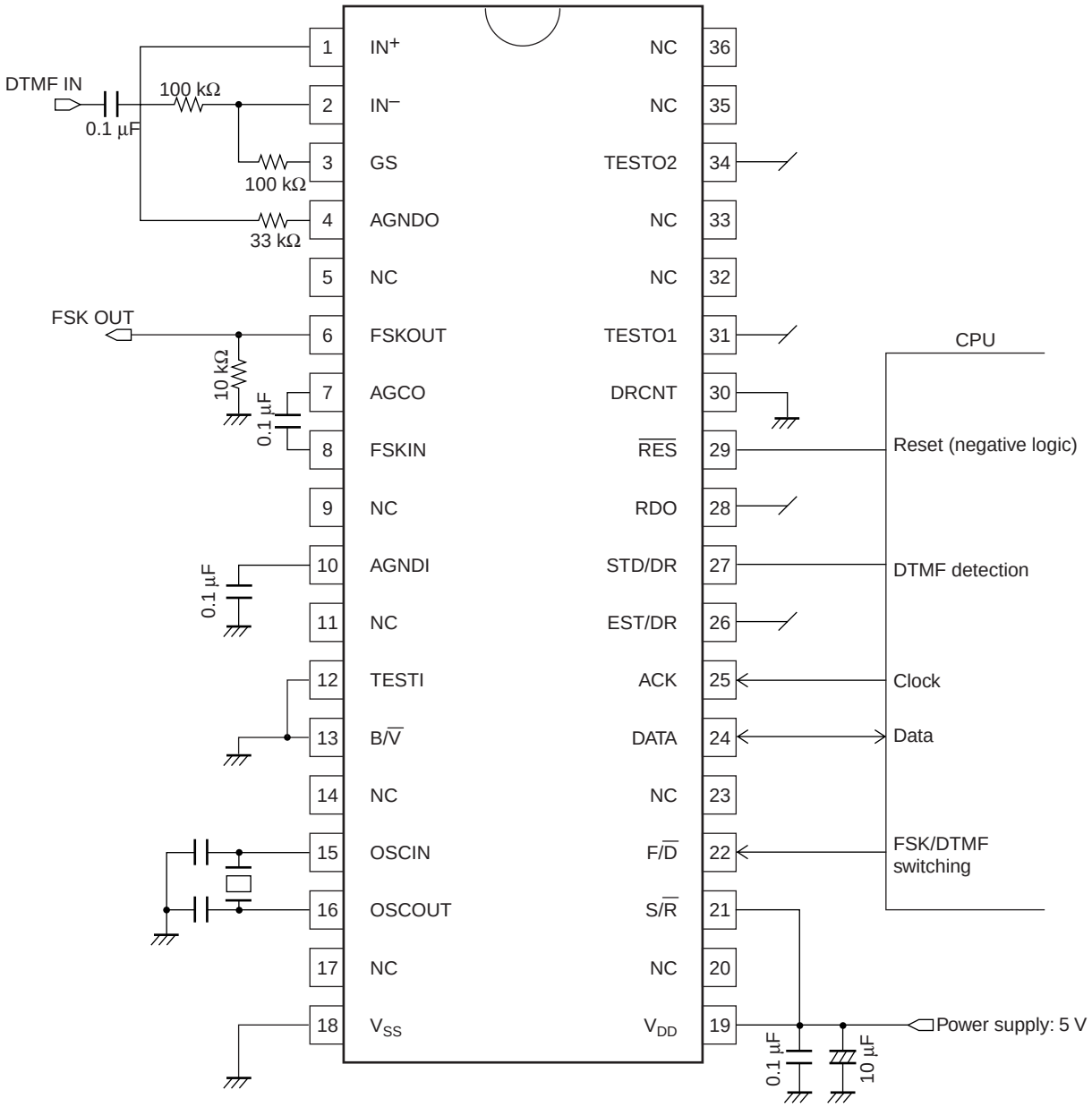


Top view

A12335

Sample Application Circuit

This example uses the DTMF receiver and the V.23 modulator, but does not use the FSK demodulator.



Top view

A12336