To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK2570

Silicon N-Channel MOS FET
Low Frequency Power Switching

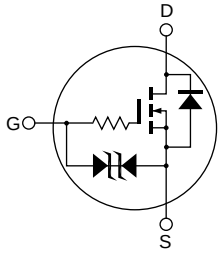
ADE-208-574 (Z)
1st. Edition
Aug. 1997

Features

- Low on-resistance
  $R_{DS(on)}$ = 0. 8Ω typ. (V_{GS} = 4 V, I_D = 100 mA)
- 2.5V gate drive devices.
- Small package (MPAK)

Outline

MPAK



1. Source
2. Gate
3. Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	20	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	0.2	A
Drain peak current	$I_{D(pulse)}$*[1]	0.4	A
Channel dissipation	Pch	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Note: 1. PW ≤ 10µs, duty cycle ≤ 1 %

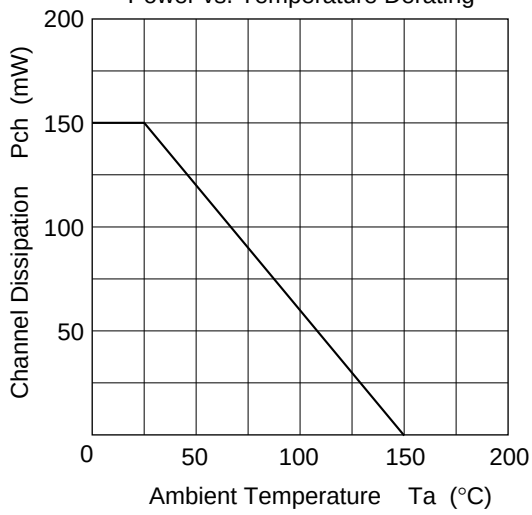
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	I_D = 10µA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±100µA, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	1.0	µA	V_{DS} = 20 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±5.0	µA	V_{GS} = ±6.5V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	I_D = 10µA, V_{DS} = 5V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.8	1.1	Ω	I_D = 100 mA V_{GS} = 4V*[1]
		—	1.3	2.2	Ω	I_D = 40 mA V_{GS} = 2.5V*[1]
Forward transfer admittance	$\|y_{fs}\|$	0.22	0.35	—	S	I_D = 100 mA V_{DS} = 10V*[1]
Input capacitance	Ciss	—	45	—	pF	V_{DS} = 10V
Output capacitance	Coss	—	33	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	9.6	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	V_{GS} = 5V, I_D = 100 mA
Rise time	t_r	—	60	—	ns	R_L = 100Ω
Turn-off delay time	$t_{d(off)}$	—	240	—	ns	
Fall time	t_f	—	140	—	ns	

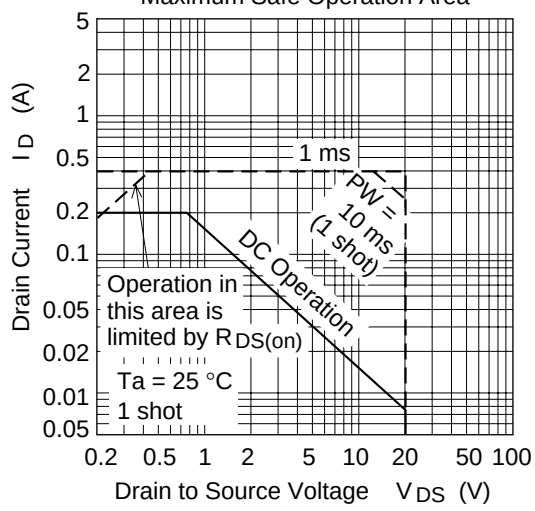
Notes: 1. Pulse test
2. Marking is “ZL–”

Main Characteristics

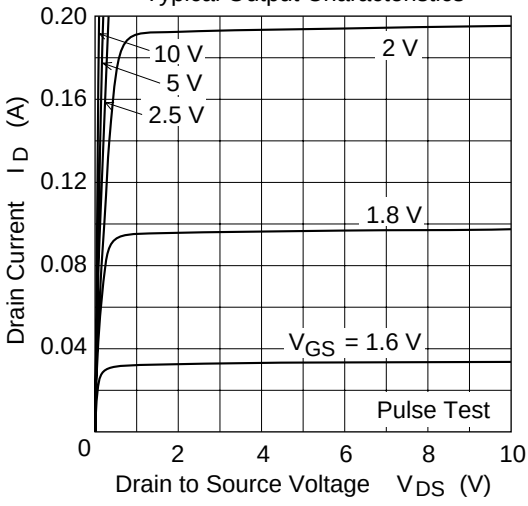
Power vs. Temperature Derating



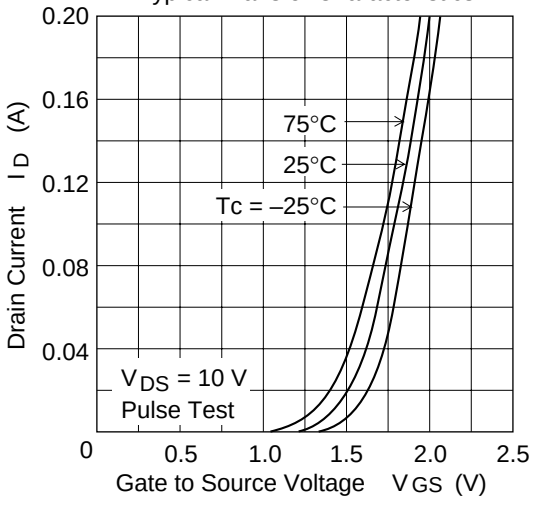
Maximum Safe Operation Area



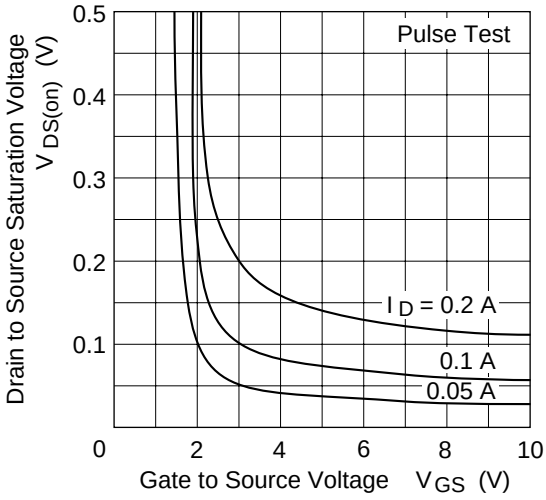
Typical Output Characteristics



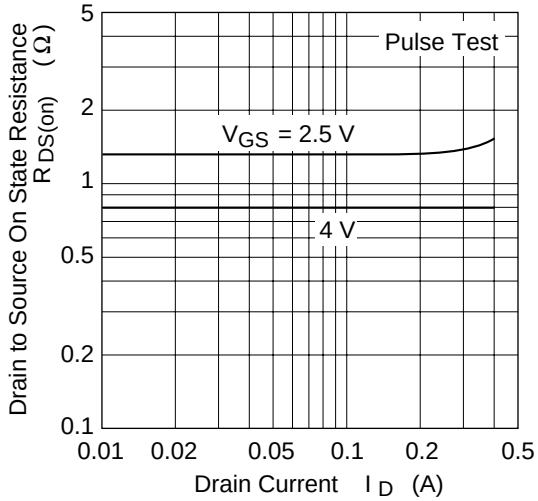
Typical Transfer Characteristics



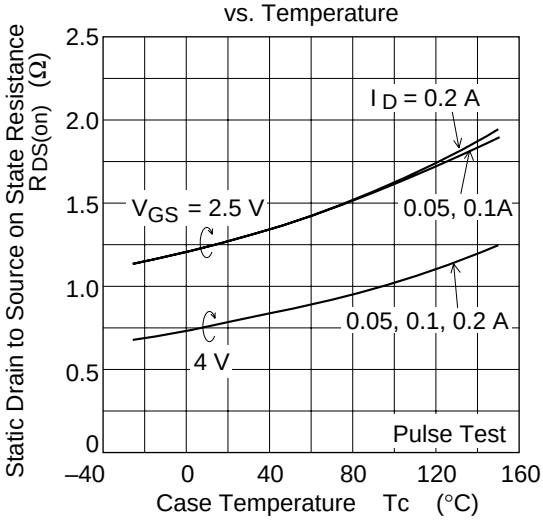
Drain to Source Saturation Voltage vs. Gate to Source Voltage



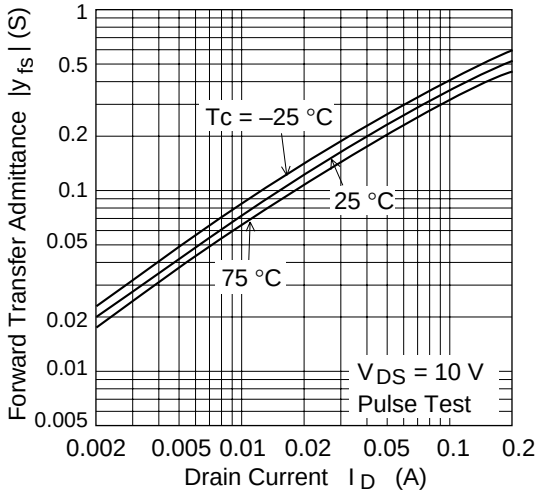
Static Drain to Source on State Resistance vs. Drain Current



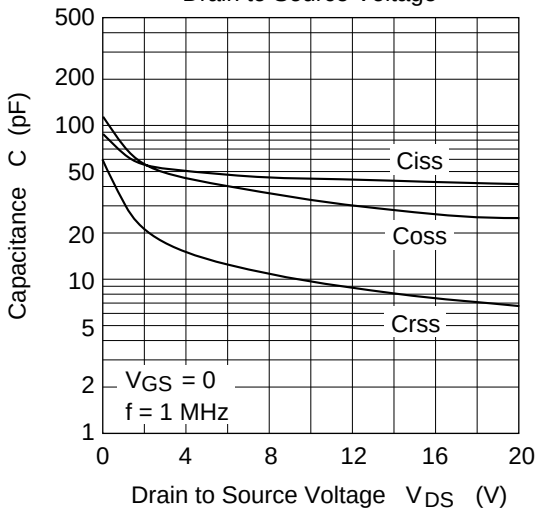
Static Drain to Source on State Resistance vs. Temperature



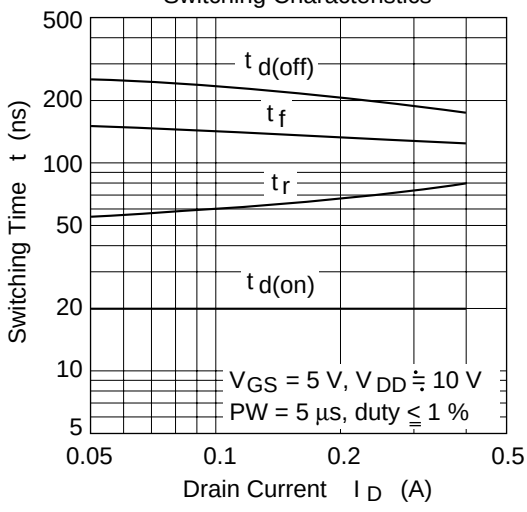
Forward Transfer Admittance vs. Drain Current



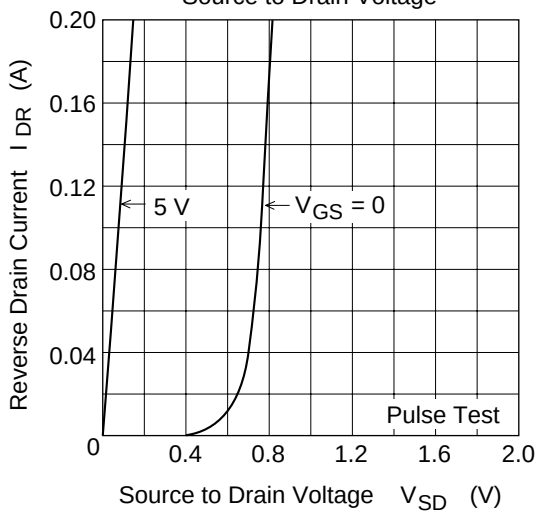
Typical Capacitance vs.
Drain to Source Voltage



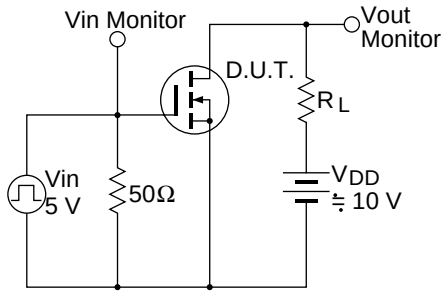
Switching Characteristics



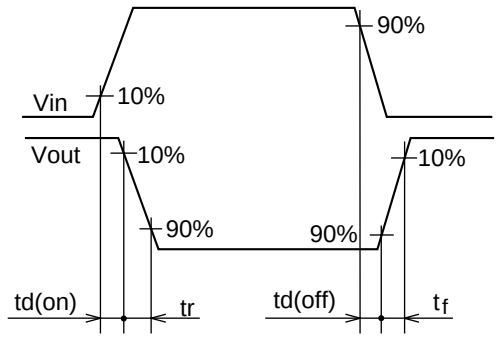
Reverse Drain Current vs.
Source to Drain Voltage



Switching Time Test Circuit



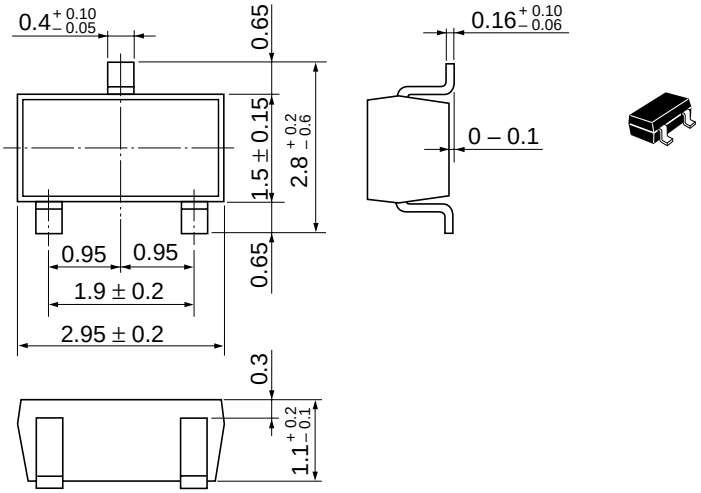
Waveform



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	MPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.011 g

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