DECT PLL / TX IC

Description

The U2786B is an RF IC for low-power DECT transmit applications. The IC includes a complete PLL with 1-GHz prescaler, on-chip frequency doubler, biasing for off-chip VCO, an integrated TX filter and a modulation-compensation circuit for advanced closed-loop modulation concept.

Electrostatic sensitive device.
Observe precautions for handling.

Features

- 1-GHz PLL, frequency doubler, TX data filter (13.824-MHz/ 27.648-MHz reference clock)
- Supply-voltage range: 2.7 V to 4.7 V
- Low current consumption
- Few external components
- No mechanical tuning necessary
- Switchable charge-pump current for enhanced switching time
- 1 operational amplifier for active loop filter
- Advanced closed-loop modulation (with 13.824-MHz/ 27.648-MHz reference clock) and open loop modulation supported

Block Diagram

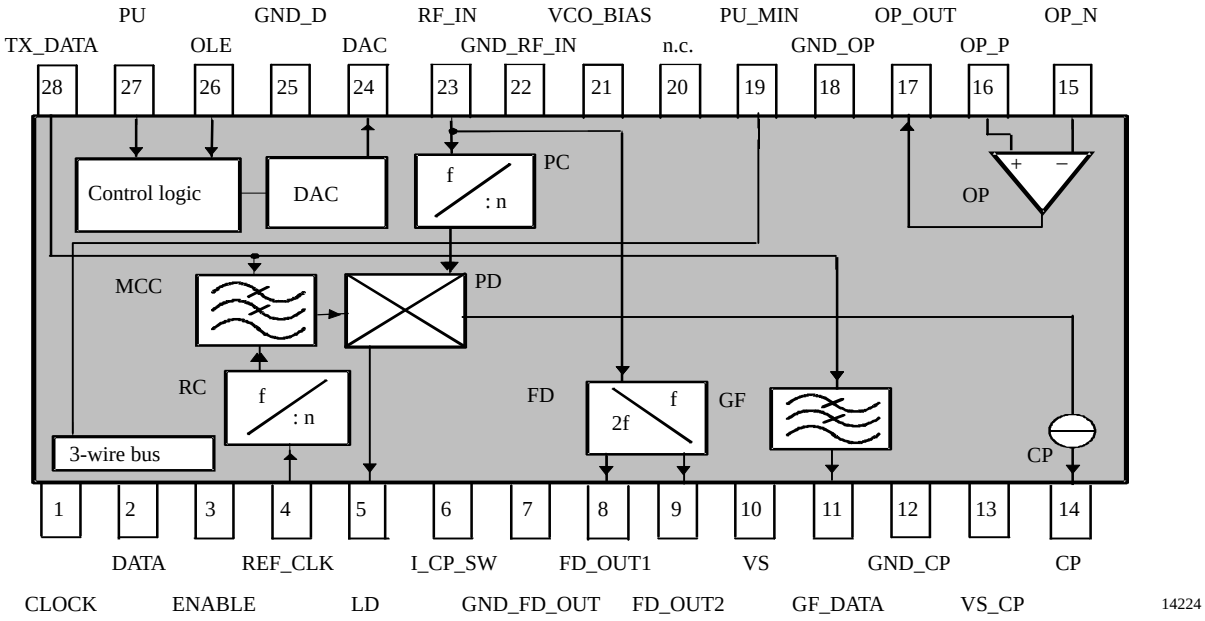


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U2786B-MFS	SSO28	Tube
U2786B-MFSG3	SSO28	Taped and reeled

Preliminary Information

Pin Description

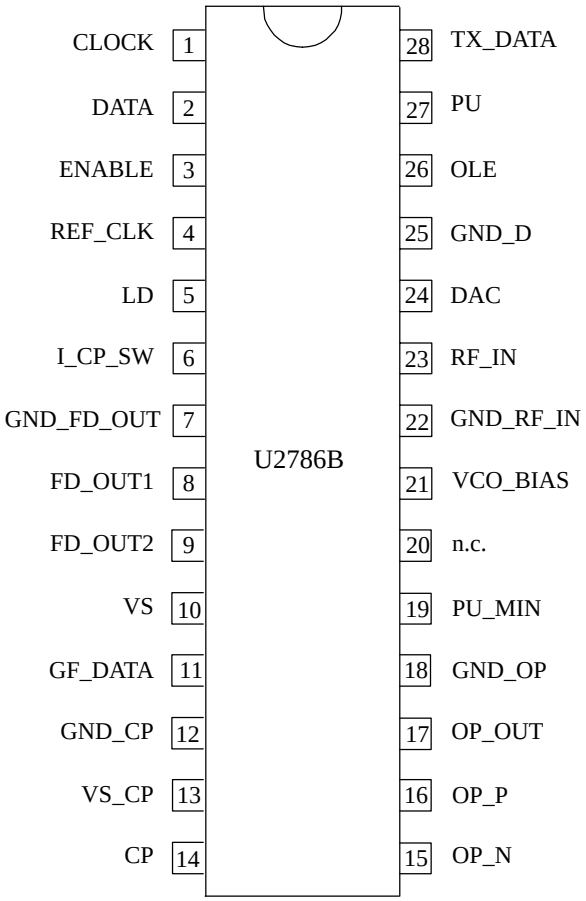
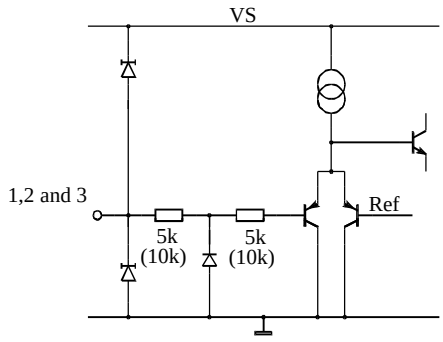
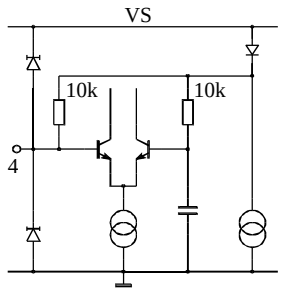
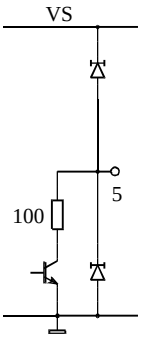
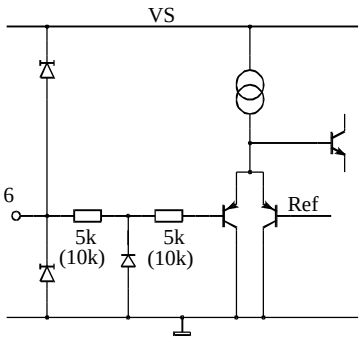
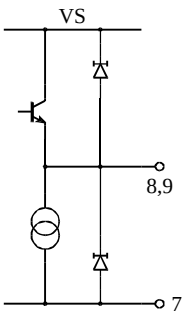


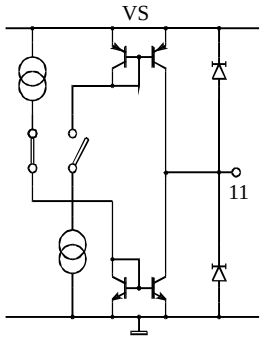
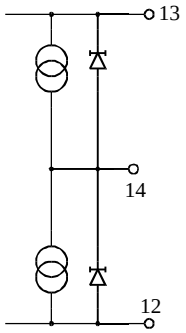
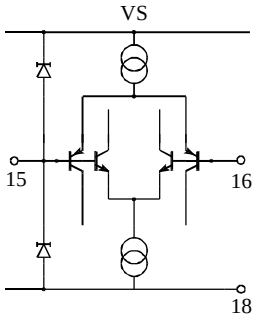
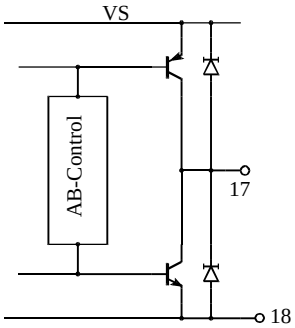
Figure 2. Pinning

Pin	Symbol	Function	Configuration
1	CLOCK	3-wire bus: Clock input	
2	DATA	3-wire bus: Data input	
3	ENABLE	3-wire bus: Enable input	

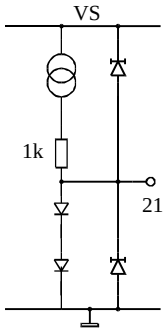
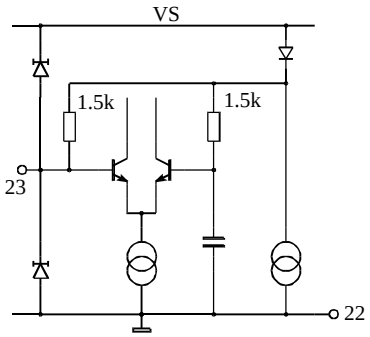
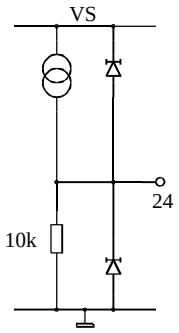
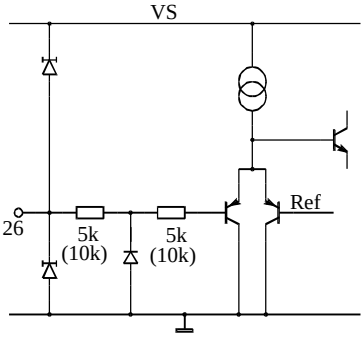
Pin Description (continued)

Pin	Symbol	Function	Configuration
4	REF_CLK	Reference frequency input	
5	LD	Lock detect output	
6	I_CP_SW	Charge-pump current switch	
7	GND_FD_OUT	Frequency-doubler buffer ground	
8	FD_OUT1	Frequency-doubler buffer output 1	
9	FD_OUT2	Frequency-doubler buffer output 2	
10	VS	Supply voltage	

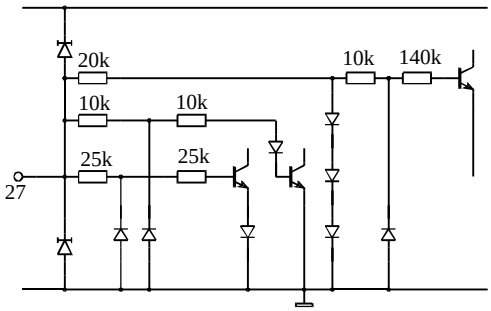
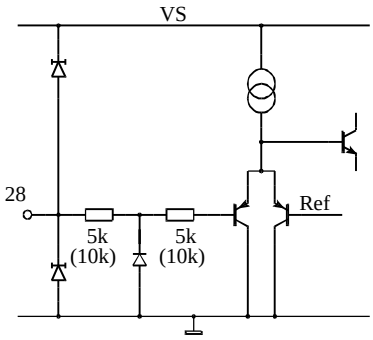
Pin Description (continued)

Pin	Symbol	Function	Configuration
11	GF_DATA	Modulation output (Gaussian filtered data signal)	
12	GND_CP	Charge-pump ground	
13	VS_CP	Charge-pump supply voltage	
14	CP	Charge-pump output	
15	OP_N	Operational-amplifier inverting input	
16	OP_P	Operational-amplifier non-inverting input	
17	OP_OUT	Operational-amplifier output	
18	GND_OP	Operational-amplifier ground	
19	PU_MIN	3-wire bus: Data-hold enable in power-down mode	

Pin Description (continued)

Pin	Symbol	Function	Configuration
20	n.c.	Not connected	
21	VCO_BIAS	VCO bias voltage output	
22	GND_RF_IN	RF input ground	
23	RF_IN	RF input from VCO to doubler and PLL	
24	DAC	DAC for VCO pretune	
25	GND_D	Digital ground	
26	OLE	Open-loop enable input	

Pin Description (continued)

Pin	Symbol	Function	Configuration
27	PU	Power-up input (active high)	
28	TX_DATA	Digital TX data input to Gaussian filter and modulation compensation circuit	

Functional Blocks

CP Charge pump
FD Frequency doubler
OP Amplifier for loop filter
MCC Modulation-compensation circuit
PD Phase detector
VCO Voltage-controlled oscillator
DAC DA converter for pretuning of VCO
GF Gaussian filter for transmit data
LF Loop filter
PC Programmable counter = MC (main counter) + SC (swallow counter)
RC Reference counter

Absolute Maximum Ratings

All voltages refer to GND (Pins 7, 12, 18, 22 and 25).

Parameter		Symbol	Min.	Max.	Unit
Supply voltage	Pins 10 and 13	V_S		5.0	V
Logic input voltage	Pins 1, 2, 3, 6, 26, 27 and 28	V_{IN}	– 0.3	5.0	V
Junction temperature		T_{jmax}		150	°C
Storage temperature		T_{stor}	–40	150	°C

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction ambient	R_{thJA}	130	K/W

Operating Range

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage Pins 10 and 13	V_S	2.7	3.0	4.7	V
Ambient temperature	T_{amb}	–25	+25	+85	°C

Electrical Characteristics

Test conditions (unless otherwise specified): V_S = 3 V, T_{amb} = 25°C

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power supply	**Pin 10**					
Standby current	V_{PU} = low level = '0'	$I_{S,OFF}$		1	10	µA
	RX (OLE = '1')	I_S		6		mA
	TX (OLE = '0')	I_S		11.5		mA
	TX, MCC on	I_S		13.2		mA
	TX, MCC, GF on	I_S		12.8		mA
	TX, MCC, GF, OP on	I_S		15		mA
	TX, MCC, GF, OP, FD on	I_S		25.8		mA
Supply current CP	V_{VS_CP} = 3 V, PLL in lock condition Pin 14	I_{CP}		1		µA
Frequency doubler f_{RF_IN} = 900 MHz (Pin 23) Pins 8 and 9 (differential)						
Output power	P_{RF_IN}= –10 dBm Z_{load} = 50 Ω (differential) Pins 8 and 9	P_{FD_OUT}	– 10	– 5	– 3	dBm
Harmonic suppression	2^{nd} + 3^{rd}; P_{RF_IN}= –10 dBm Pins 8 and 9	HS	– 20			dBc
Subharmonic suppression	P_{RF_IN}= –10 dBm Pins 8 and 9	SHS	– 20			dBc
PLL						
Input frequency	Pin 23	f_{RF_IN}	800		1000	MHz
Input voltage	f_{RF_IN} = 800 to 1000 MHz AC-coupled sinewave, Pin 23	V_{RF_IN}	20		200	mV_{RMS}
Scaling factor prescaler		S_{PSC}		32/33		
Scaling factor main counter		S_{MC}		31/32/33/34		
Scaling factor swallow counter		S_{SC}	0		31	
External reference input frequency	AC-coupled sinewave Pin4	f_{REF_CLK}	5		28	MHz
External reference input voltage	AC-coupled sinewave Pin4	V_{REF_CLK}	50		250	mV_{RMS}
Scaling factor reference counter	Pin4	S_{RC}		12/16/24/32		

Electrical Characteristics (continued)

Test conditions (unless otherwise specified): V_S = 3 V, T_{amb} = 25°C

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Charge pump active when RX, TX	**Pin 14**					
Output current	$V_{I\_CP\_SW}$ = '0' V_{CP} = V_{VS_CP} / 2	I_{CP_1}		±1		mA
	$V_{I\_CP\_SW}$ = '1' V_{CP} = V_{VS_CP} / 2	I_{CP_5}		±5		mA
Current scaling factor	See bus protocol D0...D2 I_{CP} = CPCS × I_{CP_TYP}	CPCS	60		130	%
Leakage current		I_L		± 100		pA
Operational amplifier						
Power-gain bandwidth	Pin 17	PGBW		10		MHz
Excess phase	R_{load} = 1 kΩ, C_{load} = 15 pF Pin 17	δ		80		degree
Input offset voltage	Pins 15 and 16	V_{offs}		± 1		mV
Open-loop gain	Pin 17	g		70		dB
Output voltage range	Pin 17	V_{out}	0.3		V_S – 0.3	V
Common-mode input voltage	Pins 15 and 16	V_{in}	0.3		V_S – 0.3	V
Modulation-compensation circuit @ max. DSV ≤ 64, MCC only for f_{REF_CLK} = 13.824MHz or 27.648 MHz						
Oversampling	f_{REF_CLK}= 13.824 MHz or 27.648 MHz	OVS		6		
Integration counter		MAC	– 511		511	
Current scaling factor	See bus protocol E3...E5	MCCS	60		130	%
Gaussian transmit filter (Gaussian shape B×T = 0.5) f_{REF_CLK} has to be chosen !						
Tx data filter clock	f_{REF_CLK} = 13.824 MHz, TX, 12 taps in filter	f_{TXFCLK}		6.912		MHz
	f_{REF_CLK} = 27.648 MHz, TX, 12 taps in filter	f_{TXFCLK}		6.912		MHz
Maximum output current	Polarity see bus protocol D13 Pin 11	$\|I_{GF\_DATA}\|$		8.5		µA
Current scaling factor	See bus protocol D6...D8 I_{GF_DATA} = GFCS × I_{GF_TYP} Pin 11	GFCS	60		130	%
VCO biasing	**Pin 21**					
Bias voltage		V_{VCO}		1.5		V
	Standby, PU = '0'	V_{VCO}		0	10	mV
Temperature coefficient		TC		– 3.3		mV/K

Electrical Characteristics (continued)

Test conditions (unless otherwise specified): V_S = 3 V, T_{amb} = 25°C

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
DAC for VCO PRETUNE 3-bit programming, see BUS protocol D3....D5 Pin 24						
DAC low level	I_{load} = 1 µA	V_{DAC_min}		0.3		V
DAC step level	Nonlinear (see D3...D5)	V_{DAC_step}				V
DAC high level	I_{load} = 1 µA	V_{DAC_max}		2.25		V
Output impedance		R_{DAC_out}		10		kΩ
Lock-detect output						
Lock-detect output, test-mode output	locked = '1', unlocked = '0' test modes see bus protocol E0....E2 Pin 5	LD				
Leakage current	V_{OH} = 4.5 V Pin5	I_L			5	µA
Saturation voltage	I_{OL} = 0.5 mA Pin 5	V_{SL}			0.4	V
3-wire bus						
Clock	Pin 1	f_{clock}		1.152		MHz
Logic input levels (CLOCK, DATA, ENABLE, I_CP_SW, OLE, GF_DATA) Pins 1, 2, 3, 6, 26 and 28						
High input level	='1'	V_{iH}	1.5			V
Low input level	='0'	V_{iL}			0.5	V
High input current	='1'	I_{iH}	–5		5	µA
Low input current	='0'	I_{iL}	–5		5	µA
Standby control						
Power up High input level	PU = '1' Pin 27	V_{PU}	2.0			V
Low input level	PU = '0' Pin 27	$V_{PU,OFF}$			0.7	V
DATA hold enable High input level	PU_MIN = '1' Pin 19	V_{PU_MIN}	2.0			V
Low input level	PU_MIN = '0' Pin 19	V_{PU_MIN}			0.7	V
Power up High input current	PU = '1' V_{PU} = 3 V V_{PU} = 4.5 V Pin 27	I_{PU}	100 220	125 300	150 420	µA µA
Standby High input current	PU = '0', PU_MIN = '1' V_{PU_MIN} = 3 V Pin 19	$I_{PU\_MIN,ON}$		21		µA
Standby Low input current	PU = '0' , PU_MIN = '0' V_{PU} = 0 V Pin 27 V_{PU_MIN} = 0.5 V Pin 19	$I_{PU,OFF}$ $I_{PU\_MIN,OFF}$			0.1 1	µA µA
Settling time: VS = 0 → active operation	Switched from VS = 0 to VS = 3 V	t_{soa}		< 10		µs
Settling time: standby → active operation	Switched from standby to PU = '1'	t_{ssa}		< 10		µs
Settling time: active operation → standby	Switched from PU = '1' to standby	t_{sas}		< 2		µs

PLL Principle

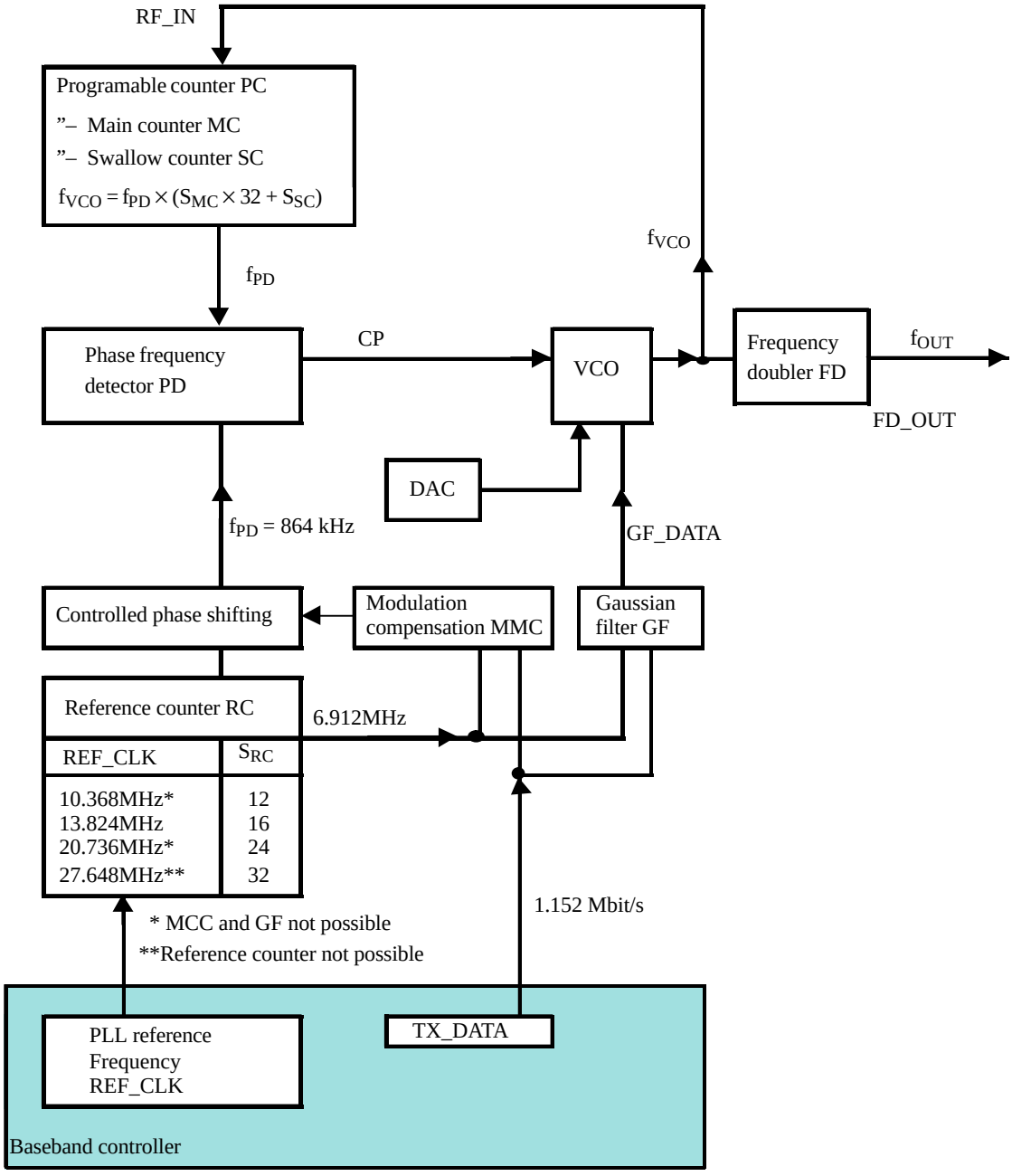


Figure 3. PLL principle

The following table shows the LO frequencies for RX and TX for the DECT band plus additional channels for an optional DECT band extension. Intermediate frequencies of 110.592 and 112.32 MHz are supported.

Table 1 LO frequencies

Mode	f_{IF}/MHz	Channel	f_{ANT}/MHz	f_{LO}/MHz	$2f_{LO}$/MHz	S_{MC}	S_{SC}
TX		C0	1897,344	948,672	1897,344	34	10
		C1	1895,616	947,808	1895,616	34	9
		C2	1893,888	946,944	1893,888	34	8
		C3	1892,16	946,08	1892,16	34	7
		C4	1890,432	945,216	1890,432	34	6
		C5	1888,704	944,352	1888,704	34	5
		C6	1886,976	943,488	1886,976	34	4
		C7	1885,248	942,624	1885,248	34	3
		C8	1883,52	941,76	1883,52	34	2
		C9	1881,792	940,896	1881,792	34	1
RX	110,592	C0	1897,344	893,376	1786,752	32	10
		C1	1895,616	892,512	1785,024	32	9
		C2	1893,888	891,648	1783,296	32	8
		C3	1892,16	890,784	1781,568	32	7
		C4	1890,432	889,92	1779,84	32	6
		C5	1888,704	889,056	1778,112	32	5
		C6	1886,976	888,192	1776,384	32	4
		C7	1885,248	887,328	1774,656	32	3
		C8	1883,52	886,464	1772,928	32	2
		C9	1881,792	885,6	1771,2	32	1
	112,32	C0	1897,344	892,512	1785,024	32	9
		C1	1895,616	891,648	1783,296	32	8
		C2	1893,888	890,784	1781,568	32	7
		C3	1892,16	889,92	1779,84	32	6
		C4	1890,432	889,056	1778,112	32	5
		C5	1888,704	888,192	1776,384	32	4
		C6	1886,976	887,328	1774,656	32	3
		C7	1885,248	886,464	1772,928	32	2
		C8	1883,52	885,6	1771,2	32	1
		C9	1881,792	884,736	1769,472	32	0

Table 2 Limits

Mode	f_{IF}/MHz		f_{ANT}/MHz	f_{LO}/MHz	$2f_{LO}$/MHz	S_{MC}	S_{SC}
TX		fmin	1714,176	857,088	1714,176	31	0
RX	110,592		1824,768	857,088	1714,176	31	0
	112,32		1826,496	857,088	1714,176	31	0
TX		fmax	1933,632	966,816	1933,632	34	31
RX	110,592		2044,224	966,816	1933,632	34	31
	112,32		2045,952	966,816	1933,632	34	31

Formula

$f_{ANT\,C1} - f_{ANT\,C2} = 1{,}728MHz$
for TX $f_{LO} = f_{ANT} / 2$
for RX $f_{LO} = (f_{ANT} - f_{IF}) / 2$

S_{MC} = integer (f_{LO} / 0,864 MHz / 32)
S_{SC} = MOD ((f_{LO} / 0,864 MHz) / 32)

Control Signals

		Standard Settings
I_CP_SW	Input for switching charge-pump current by factor 5	0
LD	Output, which is active after PLL is locked and testmode output (according to programmed testmode)	
OLE	Enable input for open-loop modulation	0
DAC	DAC for VCO band switch	
PU	Hardware power up / standby of complete PLL / TX – IC	1
PU_MIN	Data-hold enable of 3-wire bus in power-down mode	1

Serial Programming Bus

Reference and programmable counters can be programmed by the 3-wire bus (CLOCK, DATA and ENABLE). Beside this information additional control bits as phase detector polarity and scaling of charge-pump currents as well as internal currents for Gaussian lowpass filter and modulation compensation circuit can be transferred.

After setting ENABLE signal to low condition, the data status is transferred bit by bit on the rising edge of the CLOCK signal into the shift register, starting with the MSB-bit. After ENABLE returning to high condition the programmed information is loaded into the addressed latches, according to the addressbit condition (last bit). Additional leading bits are ignored and there is no check made how many pulses have arrived during ENABLE-low condition. The bus then returns to a low current standby mode until the ENABLE signal changes to low again.

During standby of the PLL the information in the registers of the PLL is maintained.

In powerdown mode of complete PLL/TX–IC (PU is set to 0) there are two possible states of the 3-wire bus.

3. PU_MIN = 1: the informations in the registers of 3-wire bus are maintained
4. PU_MIN = 0: the informations in the registers of 3-wire bus are lost

MSB																							LSB
Data bits																							Address bit
D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A0
RC		SC					MC		Phase			GF	MCC	GFCS			DAC			CPCS			1
0	1	0	1	1	1	1	0	0	0	1	0	1	1	1	0	0	1	0	0	1	0	0	1

Standard bit setting: Word 1 Word 2 →

Data bits								Address bit
E7	E6	E5	E4	E3	E2	E1	E0	A0
FD	OP	MCCS			TEST			0
1	1	1	0	0	0	0	0	0

PLL Settings

RC (Reference Counter)		
D22	D21	S_{RC}
0	0	32
0	1	12
1	0	16
1	1	24

MC (Main Counter)		
D15	D14	S_{MC}
0	0	31
0	1	32
1	0	33
1	1	34

SC (Swallow Counter)					
D20	D19	D18	D17	D16	S_{SC} *
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
					. . .
1	1	1	1	0	30
1	1	1	1	1	31

* $S_{SC} = [D16] \times 2^0 + [D17] \times 2^1 + ... [D20] \times 2^4$
$S_{PGD} = 32 \times S_{MC} + S_{SC}$

Phase Settings

Phase of GFDATA	
D13	GFDATA
0	Source
1	Sink

Phase of MCC Internal Connection	
D12	MCC Data
0	Inverted
1	Normal

Phase of CP (Charge Pump)			
D11	$f_R > f_P$	$f_R < f_P$	$f_R = f_P$
0	I_{Sink}	I_{Source}	High imp
1	I_{Source}	I_{Sink}	High imp

Current Saving Power up/down Settings

D10	GF (Gaussian Filter)
0	OFF (RX)
1	ON (TX)

E7	FD (Frequency Doubler)
0	OFF
1	ON

D9	MCC (Modulation Compensation Circuit)
0	OFF (RX or OLE = ‘1’)
1	ON (TX)

E6	OP (OpAmp)
0	OFF
1	ON

Current Gain Settings

GFCS (Gaussian Filtered Current Settings)			
D8	D7	D6	GFCS
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

MCCS (Modulation Compensation Settings)			
E5	E4	E3	MCCS
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

CPCS (Charge-Pump Current Settings)			
D2	D1	D0	CPCS
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

Pretune DAC Voltage Settings

Pretune DAC Voltage			
D5	D4	D3	DAC / V
0	0	0	0.33
0	0	1	0.43
0	1	0	0.60
0	1	1	0.79
1	0	0	1.02
1	0	1	1.38
1	1	0	1.73
1	1	1	2.24

Test Mode Settings

Test Output Pin (Lock Detect)					
D11	E2	E1	E0	Signal at Lock Detect and PLL Mode	CP Mode
x	0	0	0	Lock detect mode	Active
0	0	0	1	RC out and CP active	Active
1	0	1	0	PC out and CP active (phase changed)	Active
x	0	1	1	MCCTEST (RC out divided by 2048 or 4096)	Active
x	1	0	0	CP tristate only	High impedance
0	1	0	1	RC out and CP high impedance	High impedance
1	1	1	0	PC out and CP high impedance	High impedance
x	1	1	1	GFTEST (RC out divided by 4 or 8)	High impedance

3-Wire Bus Protocol Pulse Diagram

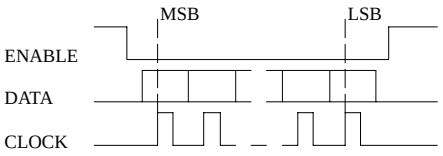


Figure 4. Pulse diagram

3-Wire Bus Protocol Timing Diagram

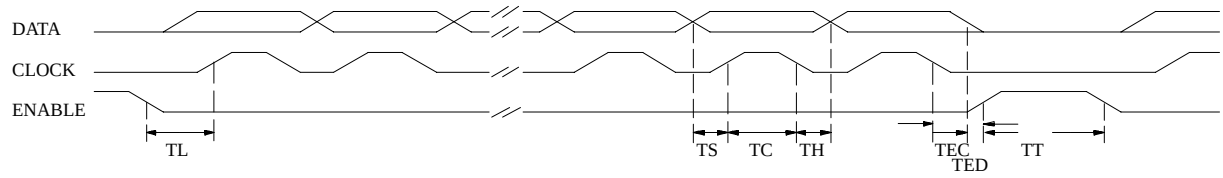


Figure 5. Timing diagram

Description	Symbol	Min. Value	Unit
Set time DATA to CLOCK	TS	434	ns
Hold time DATA to CLOCK	TH	0	ns
CLOCK pulse width	TC	434	ns
Set time ENABLE to CLOCK	TL	217	ns
Hold time ENABLE to CLOCK	TEC	0	ns
Hold time ENABLE to DATA	TED	0	ns
Time between two protocols	TT	868	ns

Typical Application Circuit

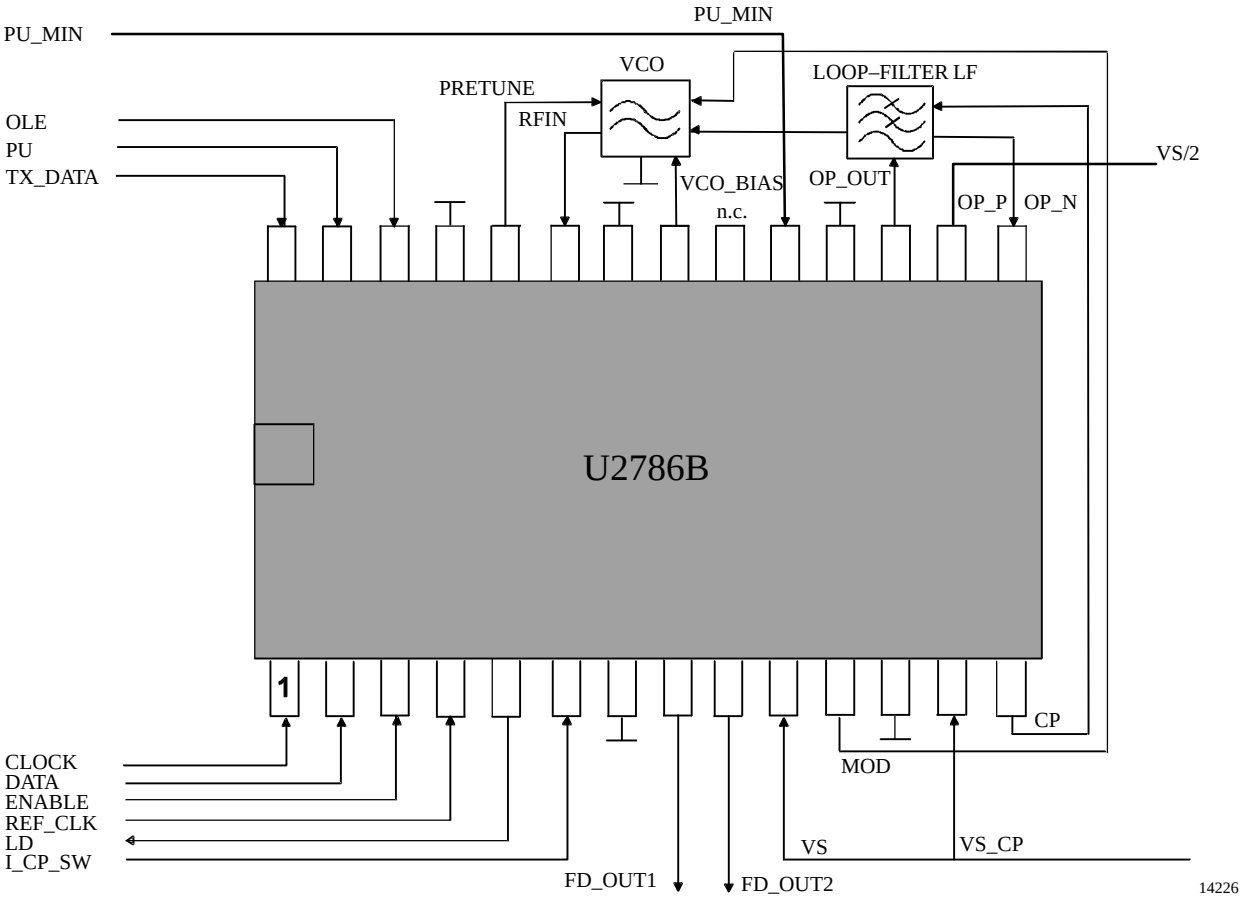
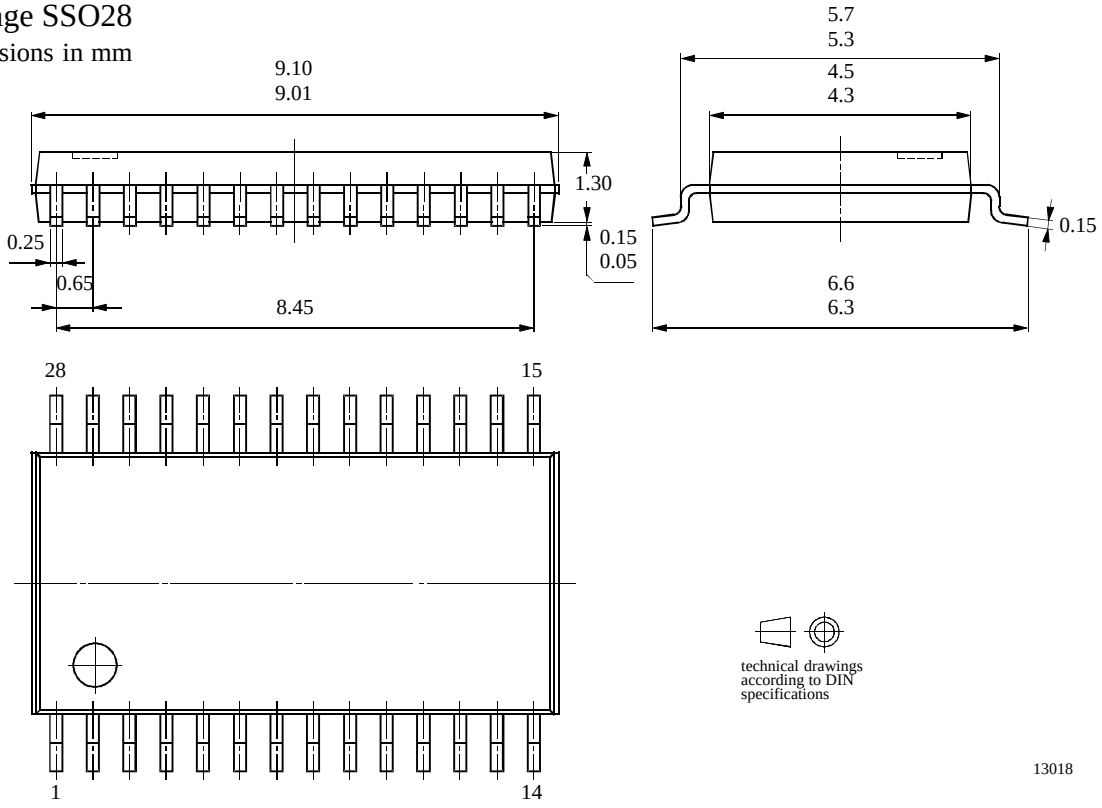


Figure 6. Application circuit

Package Information

Package SSO28
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Data sheets can also be retrieved from the Internet: http://www.temic–semi.com

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