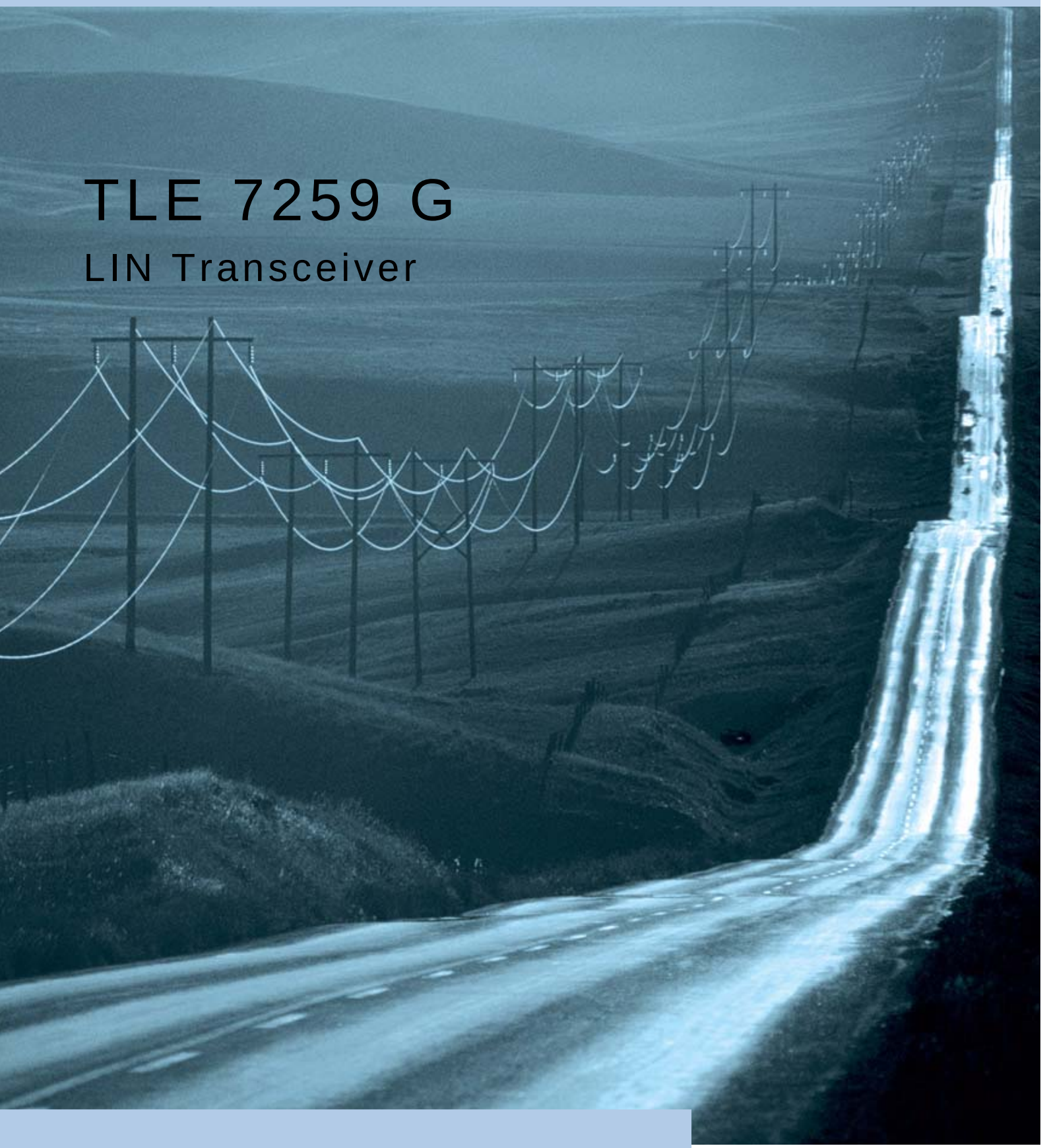

TLE 7259 G

LIN Transceiver

Automotive Power

Never stop thinking.

Edition 2004-12-13

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
81669 München, Germany

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Features

- Transmission rate up to 20 kBaud
- Compatible to LIN specification 1.2, 1.3 and 2.0
- Support of K-line function
- Very low current consumption in sleep mode
- Very low leakage current in unpowered state
- Control output for voltage regulator
- Wake up source recognition (local/remote)
- For 3.3 V and 5 V µC I/O
- Suitable for 12V and 24V boardnet
- Bus short to V_{BAT} protection
- Bus short to GND handling
- Overtemperature protection

P-DSO-8-3, -6, -7, -8, -9

Description

The TLE 7259 G is a monolithic integrated circuit in a P-DSO-8-3 package. It works as an interface between the protocol controller and the physical bus. The TLE 7259 G is especially suitable to drive the bus line in LIN systems in automotive and industrial applications.

In order to reduce the current consumption, the TLE 7259 G offers a sleep operation mode. In this mode the voltage regulator can be switched off by the TLE 7259 G to minimize the current consumption of the whole application. A wake-up caused by a message on the bus or a signal at the wake (WK) pin, enables the voltage regulator and sets the device to standby operation mode. The TLE 7259 G has a BUS short to GND feature implemented, to avoid a battery discharge.

The TLE 7259 G offers a very good EMC performance within a broad frequency range independent from battery voltage. This is achieved by implementing a slope control mechanism based on a constant slew rate. The TLE 7259 G can also be used with 3.3 V and 5 V micro controllers.

Type	Ordering Code	Package
TLE 7259 G	Q67006-A9694	P-DSO-8-3

The IC is based on the Smart Power Technology SPT® which allows bipolar and CMOS control circuitry in accordance with DMOS power devices existing on the same monolithic circuit. The TLE 7259 G is designed to withstand the severe conditions of automotive applications.

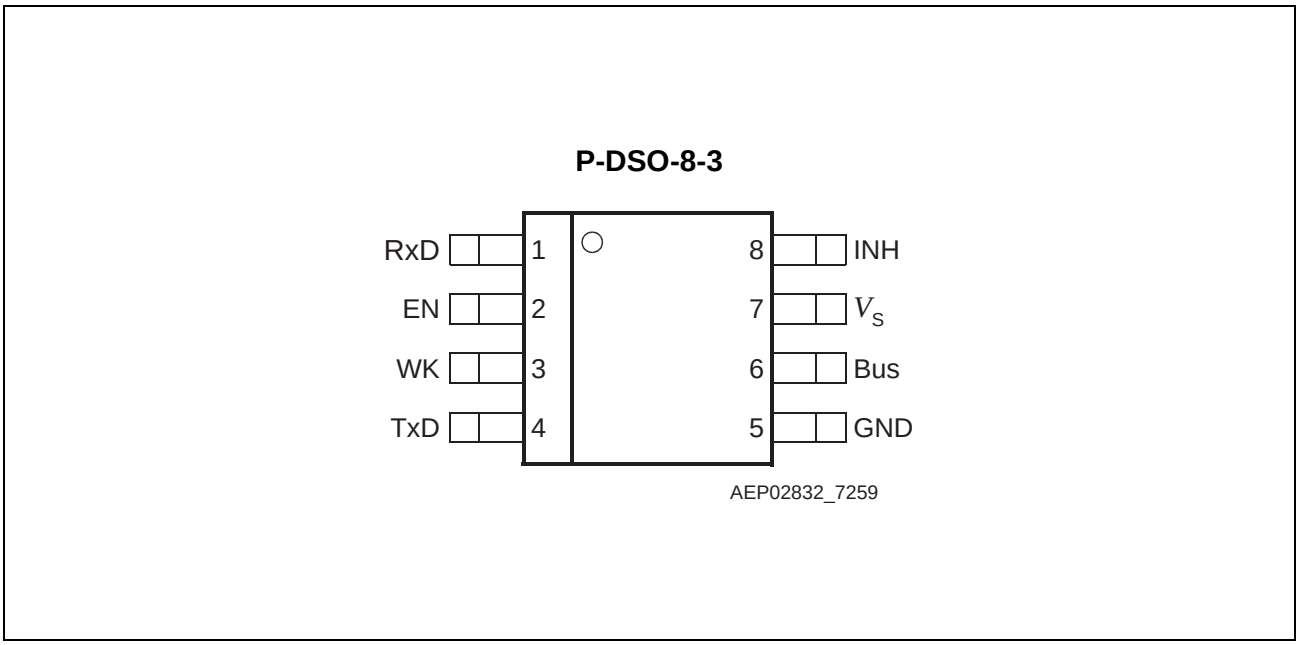


Figure 1 **Pin Configuration** (top view)

Table 1 **Pin Definitions and Functions**

Pin No.	Symbol	Function
1	RxD	**Receive data output;** external pull-up used, LOW in dominant state, active LOW after a wake-up event
2	EN	**Enable input;** integrated 30 kΩ pull-down, transceiver in normal operation mode when HIGH
3	WK	**Wake input;** active LOW, negative edge triggered, internal pull-up
4	TxD	**Transmit data input;** integrated pull-down, LOW in dominant state; active LOW after wake-up via WK pin
5	GND	**Ground**
6	Bus	**Bus output/input;** internal 30 kΩ pull-up, LOW in dominant state
7	V_S	**Battery supply input**
8	INH	**Inhibit output;** to control a voltage regulator, becomes HIGH (V_S), when wake-up via LIN bus or WK pin occurs

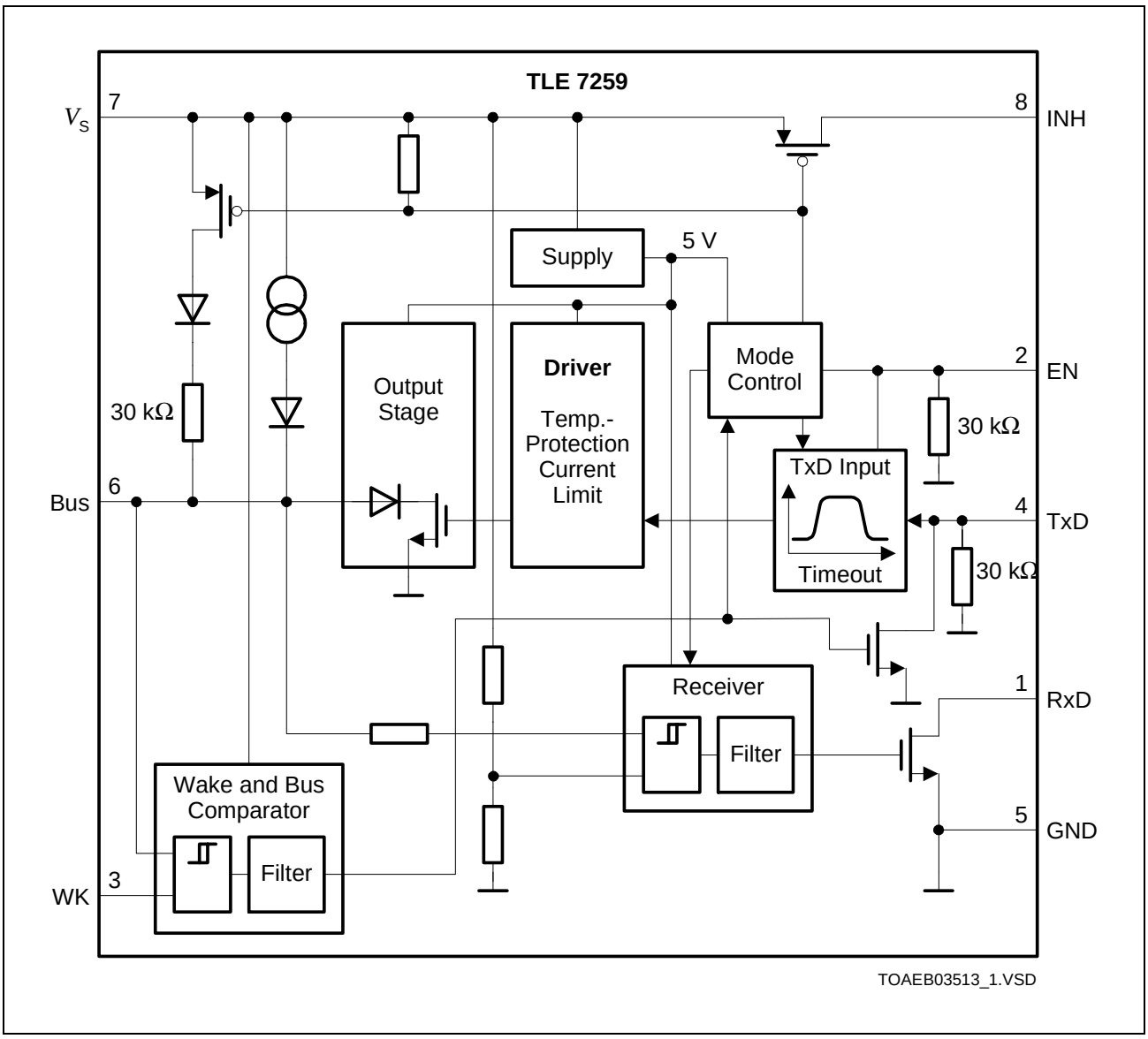


Figure 2 Functional Block Diagram

Operation Modes

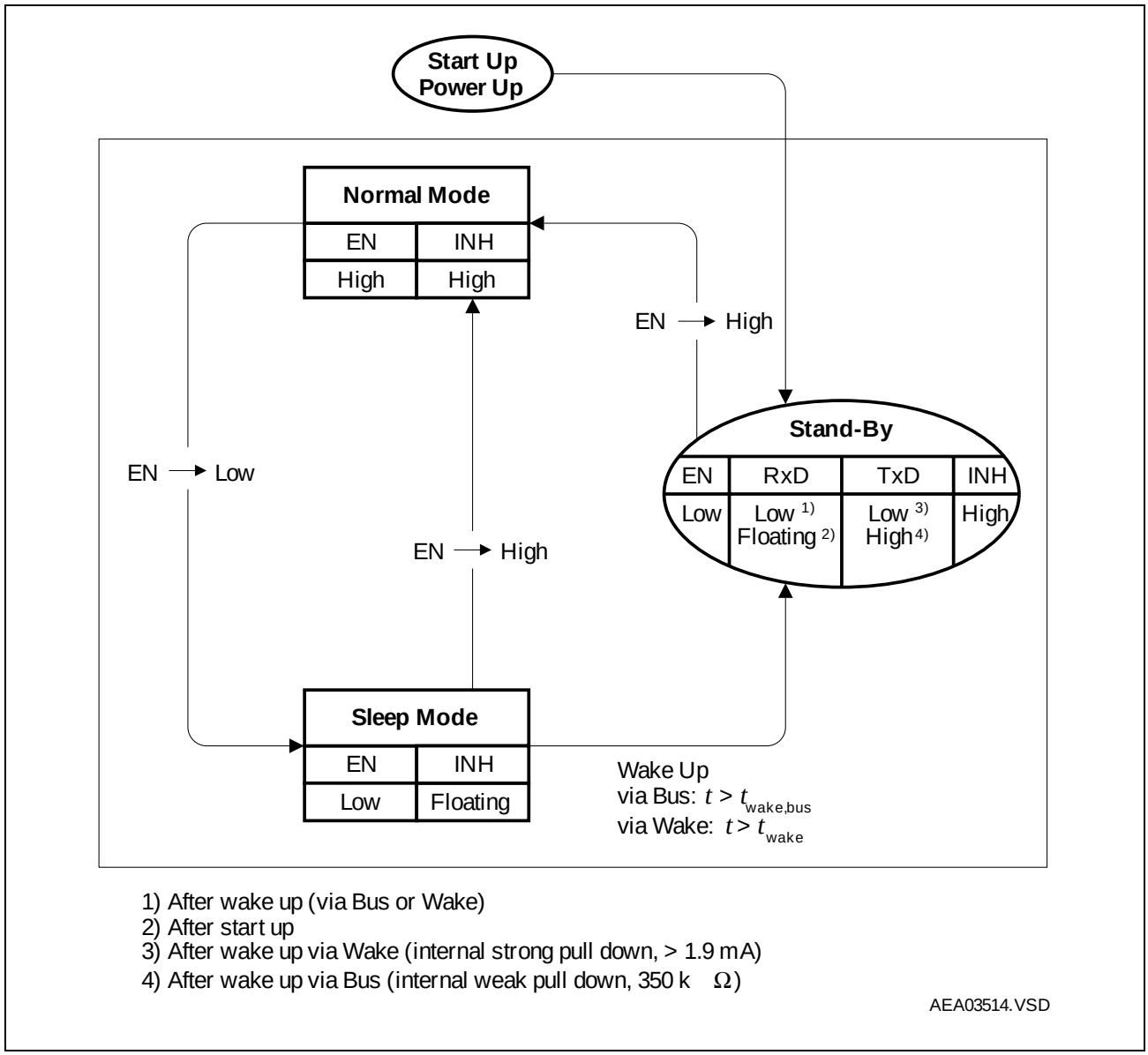


Figure 3 Operation Mode State Diagram

Standby Mode

After a power up, wake-up or low supply condition, the TLE 7259 G is automatically transferred to the standby mode (see **Figure 3**). This is realized, by setting EN = low due to a pull-down. The INH output is automatically switching to high level (= V_S), to turn on the system voltage regulator. In the standby mode, no communication on the bus is possible. The bus driver is disabled.

In the standby mode, the µC can detect if a wake-up from sleep mode is caused by the WK pin or a bus message. This is realized by monitoring the RxD and TxD pin (see **Figure 3**).

Normal Mode

The TLE 7259 G is entering the normal mode after the µC is setting EN = high (see **Figure 3**). In this mode it is possible to transmit and receive messages on the bus.

Sleep Mode

In order to reduce the current consumption the TLE 7259 G offers a sleep operation mode. This mode is selected by switching the enable input EN low from the normal mode (see **Figure 3**). In the sleep mode, a voltage regulator will be switched off via the INH output in order to minimize the current consumption of the whole application. A wake-up caused by a message on the communication bus (for $t > t_{WK,bus}$) or the WK pin (for $t > t_{WK}$), automatically enables the voltage regulator by switching the INH output high.

In parallel the wake-up is indicated by setting the RxD output LOW. The TxD input automatically is set to LOW if the source of the wake-up was the WK-pin, otherwise TxD is HIGH. So, the RxD pin can be used as a flag to indicate a wake-up from sleep mode and the TxD flag can be used as an indicator for the wake-up source (see **Figure 3**).

When entering the normal mode these wake-up flags are reset and the RxD output and TxD input is released to receive/transmit the bus data.

In case the voltage regulator control input is not connected to INH output or the microcontroller is active respectively, the TLE 7259 G can be set in normal operation mode without a wake-up via the communication bus.

Application Information

Master Termination

To achieve the required timings for the dominant to recessive transition of the bus signal an additional external termination resistor of 1 kΩ is mandatory. It is recommended to place this resistor at the master node. To avoid reverse currents from the bus line into the battery supply line it is recommended to place a diode in series to the external pull-up. For small systems (low bus capacitance) the EMC performance of the system is supported by an additional capacitor of at least 1 nF in the master node (see **Figure 6** and **Figure 7**, application circuit).

BUS short to GND Feature

The TLE 7259 G has a feature implemented to protect the battery from running out of charge in the case of BUS short to GND.

In this failure case a normal master termination connection like described above, 1 kΩ resistor and diode between bus and V_S, would cause a constantly drawn current even in sleep mode. The resulting resistance of this short to GND is lower than 1 kΩ. To avoid this current during a generator off state, like a parked car, the sleep mode has a bus short to GND feature implemented in the TLE 7259 G. This feature is only applicable, if the

master termination is connected with the INH pin, instead of the V_S (see **Figure 6** and **Figure 7**). Internally, the 30 kΩ path is also switched off from supply (see **Figure 2**).

External Capacitors

A capacitor of 22 µF at the supply voltage input V_S buffers the input voltage. In combination with the required reverse polarity diode this prevents the device from detecting power down conditions in case of negative transients on the supply line.

The 100 nF capacitors close to the V_S pins of the TLE 7259 G and the voltage regulator help to improve the EMC behavior of the system.

Oscillator Tolerance

According to the LIN Calculation table, an oscillator clock tolerance < 2% is possible with TLE 7259 G.

3.3 V and 5 V Logic Capability

The TLE 7259 G can be used for 3.3 V and 5 V micro controllers. The inputs and the outputs are capable to operate with both voltage levels. The inputs (TxD, EN) take the reference voltage from the connected µC pins. The RxD output must have an external pull-up resistance to the µC supply, to define the output voltage level.

LIN Specifications 1.2, 1.3 and 2.0

The difference between LIN specification 1.2 and 1.3 is mainly the physical layer specification. The reason was to improve the compatibility between the nodes.

The difference between LIN specification 1.3 and 2.0 is that the 2.0 version is a superset of the 1.3 version. The 2.0 version offers some new features. However, it is possible to use the LIN 1.3 slave node in a 2.0 node cluster, as long as the new features are not used. Vice versa it is possible to use a LIN 2.0 node in the 1.3 cluster without using the new features.

LIN 2.0 is the latest version of the LIN specification, released in September 2003.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Voltages					
Battery supply voltage	V_S	-0.3	40	V	(LIN Spec 1.3(2.0); Line 10.1.3 (3.1.3))
Bus input voltage versus GND versus V_S	 $V_{BUS,G}$ $V_{BUS,Vs}$	 -40 -40	 40 40	 V V	t < 1 s
Wake input versus GND Wake input versus V_S	$V_{WK,G}$ $V_{WK,Vs}$	-40 -40	40 40	V V	–
Logic voltages at EN, TxD, RxD	V_{IO}	-0.3	5.5	V	–
Inhibit Voltage versus GND Versus V_S	 $V_{INH,G}$ $V_{INH, Vs}$	 -0,3 -40	 40 0,3	 V V	
Output current at INH	I_{INH}	-150	80	mA	pos. output current is internally limited
Electrostatic discharge voltage at V_S, Bus, Wk versus GND	V_{ESD}	-4	4	kV	human body model (100 pF via 1.5 kΩ)
Electrostatic discharge voltage Jedec Norm	V_{ESD}	-2	2	kV	human body model (100 pF via 1.5 kΩ)
Temperatures					
Junction temperature	T_j	-40	150	°C	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Supply Voltage range V_S	V_S	5	40	V	(LIN Spec 1.3 (2.0); Line 10.1.2 (3.1.2))
Junction temperature	T_j	-40	150	°C	–
Thermal Resistances					
Junction ambient	$R_{thj\text{-}a}$	–	185	K/W	–
Thermal Shutdown (Junction Temperature)					
Thermal shutdown temp.	T_{jSD}	150	170	190	°C
Thermal shutdown hyst.	ΔT	–	10	–	K

Table 4 Electrical Characteristics

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Current Consumption						
Current consumption at V_S	I_S	–	0.8	1.5	mA	recessive state, without R_L; V_{TxD} = V_{CC}
		–	1.3	2.5	mA	dominant state, without R_L; V_{TxD} = 0 V
Current consumption in sleep mode	I_S	–	–	14	µA	sleep mode, V_{WK} = V_S; V_{BUS} = V_S
Current consumption in stand-by mode	I_S	–	–	1.5	mA	stand-by mode, V_{WK} = V_S; V_{BUS} = V_S
Receiver Output RxD						
HIGH level leakage current	$I_{RD,H}$	-5	0	+5	µA	V_{RxD} = 5 V; V_{BUS} = V_S
LOW level output current	$I_{RD,L}$	1.9	–	–	mA	V_{RxD} = 0.9 V; V_{BUS} = 0 V
Transmission Input TxD						
HIGH level input voltage threshold	$V_{TD,H}$	–	–	0.7 × V_{EN}	V	recessive state
TxD input hysteresis	$V_{TD,hys}$	–	0.12× V_{EN}	–	mV	–
LOW level input voltage threshold	$V_{TD,L}$	0.3 × V_{EN}	–	–	V	dominant state
TxD pull-down resistance	R_{TD}	100	350	800	kΩ	V_{TxD} = 5 V
TxD low level leakage current	I_{TD}	–	–	10	µA	V_{EN} = 0 V; V_{TxD} = 0 V
TxD dominant current Wake = 0 V; V_S = 12 V; standby mode	$I_{TD,L}$	1.5	3	–	mA	V_{TxD} = 0.9 V

Table 4 Electrical Characteristics (cont'd)

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Enable Input EN						
HIGH level input voltage threshold	$V_{EN,on}$	–	–	2	V	normal mode
LOW level input voltage threshold	$V_{EN,off}$	0.8	–	–	V	low power mode
EN input hysteresis	$V_{EN,hys}$	150	300	450	mV	–
EN pull-down resistance	R_{EN}	15	30	60	kΩ	–
Enable inhibit high current	$I_{EN,\ hc}$	50	–	400	µA	V_{EN} = 5 V, 3 V
Inhibit Output INH						
Inhibit R_{on} resistance	$R_{INH,on}$	–	36	50	Ω	I_{INH} = -15 mA
Maximum INH output current	I_{INH}	40	–	150	mA	V_{INH} = 0 V
Leakage current	$I_{INH,lk}$	-5.0	–	5.0	µA	sleep mode; V_{INH} = 0 V
Wake Input WK						
High level input voltage	$V_{WK,H}$	V_S - 1	–	V_S + 3	V	–
Low level input voltage	$V_{WK,L}$	-0.3	–	V_S - 3.3 V	V	–
Pull-up current	$I_{WK,PU}$	-60	-30	-3	µA	–
High level leakage current	$I_{WK,L}$	-5	–	5	µA	V_S = 0 V; V_{WK} = 40 V
Dominant time for wake-up	t_{WK}	30	–	150	µs	–

Table 4 Electrical Characteristics (cont'd)

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Bus Receiver						
Receiver threshold voltage, recessive to dominant edge	$V_{BUS,rd}$	0.42× V_S	0.48× V_S	–	V	–
Receiver dominant state	$V_{BUS,dom}$	–	–	0.42× V_S	V	(LIN Spec 1.3 (2.0); Line 10.1.9 (3.1.9))
Receiver threshold voltage, dominant to recessive edge	$V_{BUS,dr}$	–	0.52× V_S	0.58× V_S	V	$V_{BUS,rec}$ < V_{BUS} < 27 V
Receiver recessive state	$V_{BUS,rec}$	0.58× V_S	–	–	V	(LIN Spec 1.3 (2.0); Line 10.1.10 (3.1.10)
Receiver center voltage	$V_{BUS,c}$	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	(LIN Spec 1.3 (2.0); Line 10.1.11 (3.1.11)
Receiver hysteresis	$V_{BUS,hys}$	0.02× V_S	0.04× V_S	0.1 × V_S	V	$V_{BUS,hys}$ = $V_{BUS,rec}$ - $V_{BUS,dom}$ (LIN Spec 1.3 (2.0); Line 10.1.12 (3.1.12))
Wake-up threshold voltage	$V_{BUS,wk}$	0.40× V_S	0.5 × V_S	0.6 × V_S	V	–
Dominant time for bus wake-up	$t_{WK,bus}$	30	–	150	µs	–

Table 4 Electrical Characteristics (cont'd)

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Bus Transmitter						
Bus recessive output voltage	$V_{BUS,ro}$	0.8 × V_S	–	V_S	V	V_{TxD} = high Level
Bus dominant output voltage	$V_{BUS,do}$	–	–	1.2	V	V_{TxD} = 0 V; V_S = 5 V; R_L = 500 Ω; (LIN Spec 1.3; Line 10.1.13)
		–	–	2.0	V	V_S = 18 V; R_L = 500 Ω; (LIN Spec 1.3; Line 10.1.14)
Bus short circuit current	$I_{BUS,sc}$	40	100	150	mA	V_{BUS} = 13.5 V; (LIN Spec 1.3 (2.0); Line 10.1.4 (3.1.4))
Leakage current	$I_{BUS,lk}$	-500	-70	–	µA	V_S = 0 V; V_{BUS} = -8 V; (LIN Spec 1.3 (2.0); Line 10.1.7 (3.1.7))
		–	10	20	µA	V_S = 0 V; V_{BUS} = 18 V; (LIN Spec 1.3 (2.0); Line 10.1.8 (3.1.8))
		-1	–	–	mA	V_S = 18 V; V_{BUS} = 0 V; (LIN Spec 1.3 (2.0); Line 10.1.5 (3.1.5))
		–	–	20	µA	V_S = 8 V; V_{BUS} = 18 V; (LIN Spec 1.3 (2.0); Line 10.1.6 (3.1.6))
Bus pull-up resistance	R_{BUS}	20	30	47	kΩ	Normal mode (LIN Spec 1.3 (2.0); Line 10.2.2 (3.2.2))
LIN output current	I_{BUS}	5	30	60	µA	Sleep mode

Table 4 Electrical Characteristics (cont'd)

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Dynamic Transceiver Characteristics						
Slew rate falling edge	t_{fslope}	-3	–	-1	V/µs	[1] 60% > V_{bus} > 40%; 1 µs < ($\tau = R_L \times C_{BUS}$) < 5 µs; V_S = 13.5 V; normal mode; (LIN Spec 1.3; Line 10.3.1)
Slew rate rising edge	t_{rslope}	1	–	3	V/µs	[1] 40% < V_{bus} < 60%; 1 µs < ($\tau = R_L \times C_{BUS}$) < 5 µs; V_S = 13.5 V; normal mode; (LIN Spec 1.3; Line 10.3.1)
Slope symmetry	$t_{slopesym}$	-5	–	5	µs	t_{fslope} - t_{rslope}; V_S = 13.5 V; (LIN Spec 1.3; Line 10.3.2)
Propagation delay TxD LOW to bus	$t_{d(L),T}$	–	1	4	µs	V_{EN} = 5 V; (LIN Spec 1.3; Line 10.3.6)
Propagation delay TxD HIGH to bus	$t_{d(H),T}$	–	1	4	µs	V_{EN} = 5 V; (LIN Spec 1.3; Line 10.3.6)
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	–	1	6	µs	V_{CC} = 5 V; C_{RxD} = 20 pF; R_{RxD} = 2.4 kΩ; (LIN Spec 1.3; Line 10.3.7)
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	–	1	6	µs	V_{CC} = 5 V; C_{RxD} = 20 pF; R_{RxD} = 2.4 kΩ; (LIN Spec 1.3; Line 10.3.7)

Table 4 Electrical Characteristics (cont'd)

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$; (LIN Spec 1.3; Line 10.3.7)
Transmitter delay symmetry	$t_{sym,T}$	-2	–	2	µs	$t_{sym,T} = t_{d(L),T} - t_{d(H),T}$; (LIN Spec 1.3; Line 10.3.8)
Wake-up delay time	t_{wake}	30	100	150	µs	$T_j \leq 125$ °C
Delay time for change sleep/stand by mode - normal mode	t_{snorm}	–	–	10	µs	–
Delay time for change normal mode - sleep mode	t_{nsleep}	–	–	10	µs	–
TxD dominant time out	$t_{timeout}$	6	12	20	ms	V_{TxD} = 0 V
TxD dominant time out recovery time	t_{torec}	–	10	–	µs	–

Table 4 Electrical Characteristics (cont'd)

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Duty cycle D1 (for worst case at 20 kBit/s)	t_{duty1}	0.396	–	–		duty cycle 1[1)] TH_{Rec}(max) = 0.744 × $V_{S;}$ TH_{Dom}(max) = 0.581 × V_S; V_S = 7.0 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus\_rec(min)}$/2 t_{bit}; (LIN Spec 2.0; line 3.3.1)
Duty cycle D2 (for worst case at 20 kBit/s)	t_{duty2}	–	–	0.581		duty cycle 2[1)] TH_{Rec}(max) = 0.422 × V_S; TH_{Dom}(max) = 0.284 × V_S V_S = 7.6 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus\_rec(max)}$/2 t_{bit}; (LIN Spec 2.0; line 3.3.2)

1) Bus load conditions concerning LIN spec 2.0 C_{bus}, R_{bus} = 1 nF, 1 kΩ / 6.8 nF, 660 Ω / 10 nF, 500 Ω

Diagrams

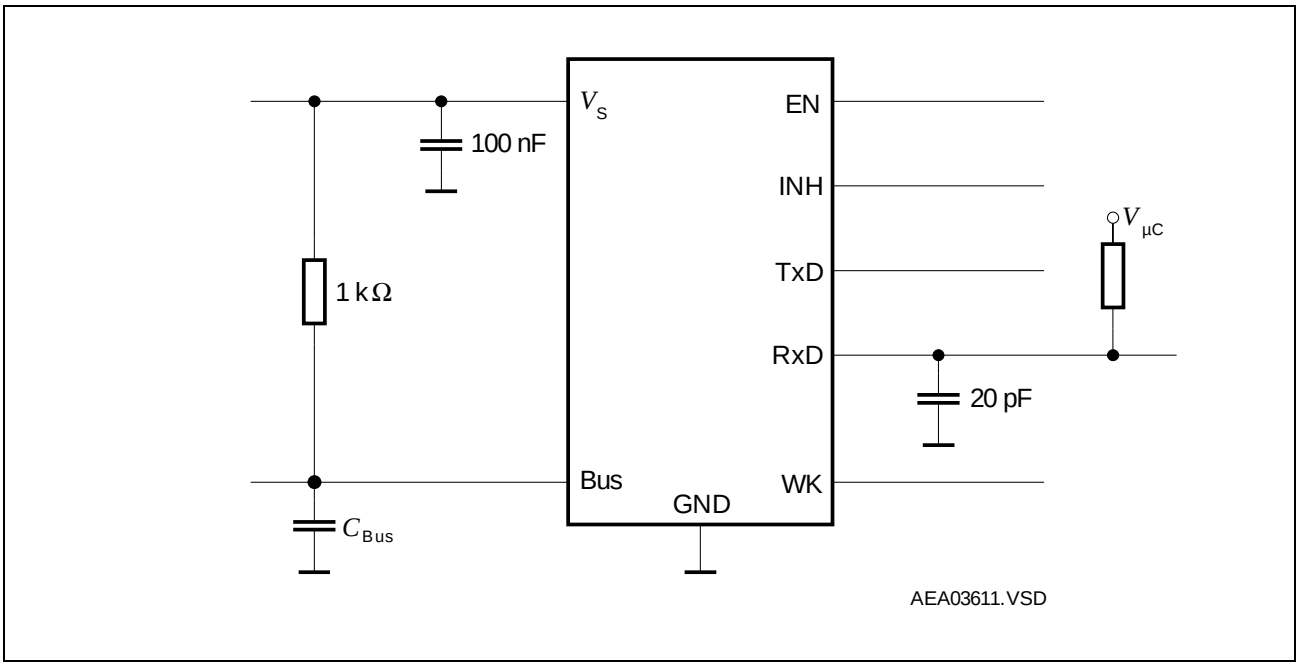


Figure 4 Test Circuits

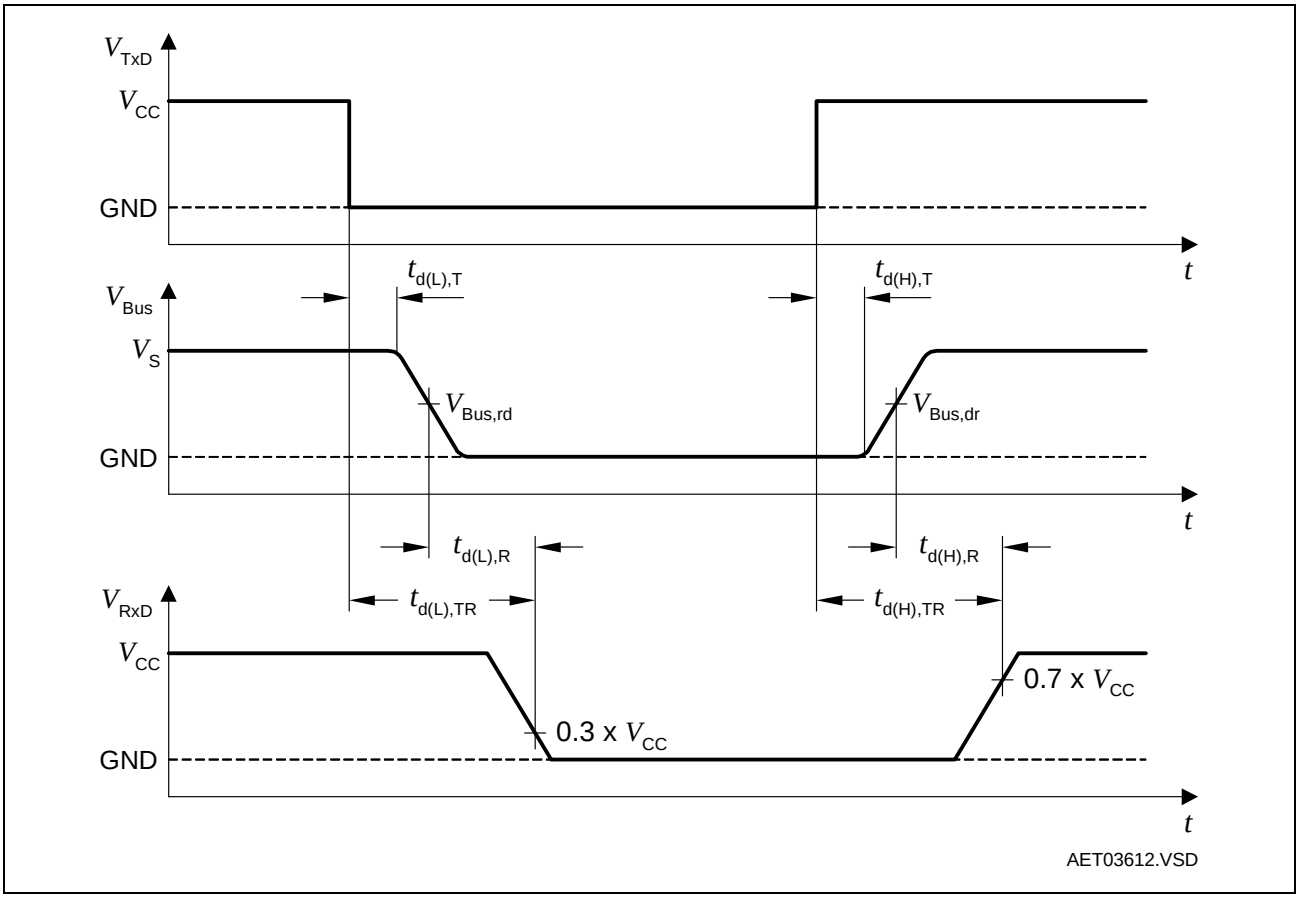


Figure 5 Timing Diagrams for Dynamic Characteristics

Application

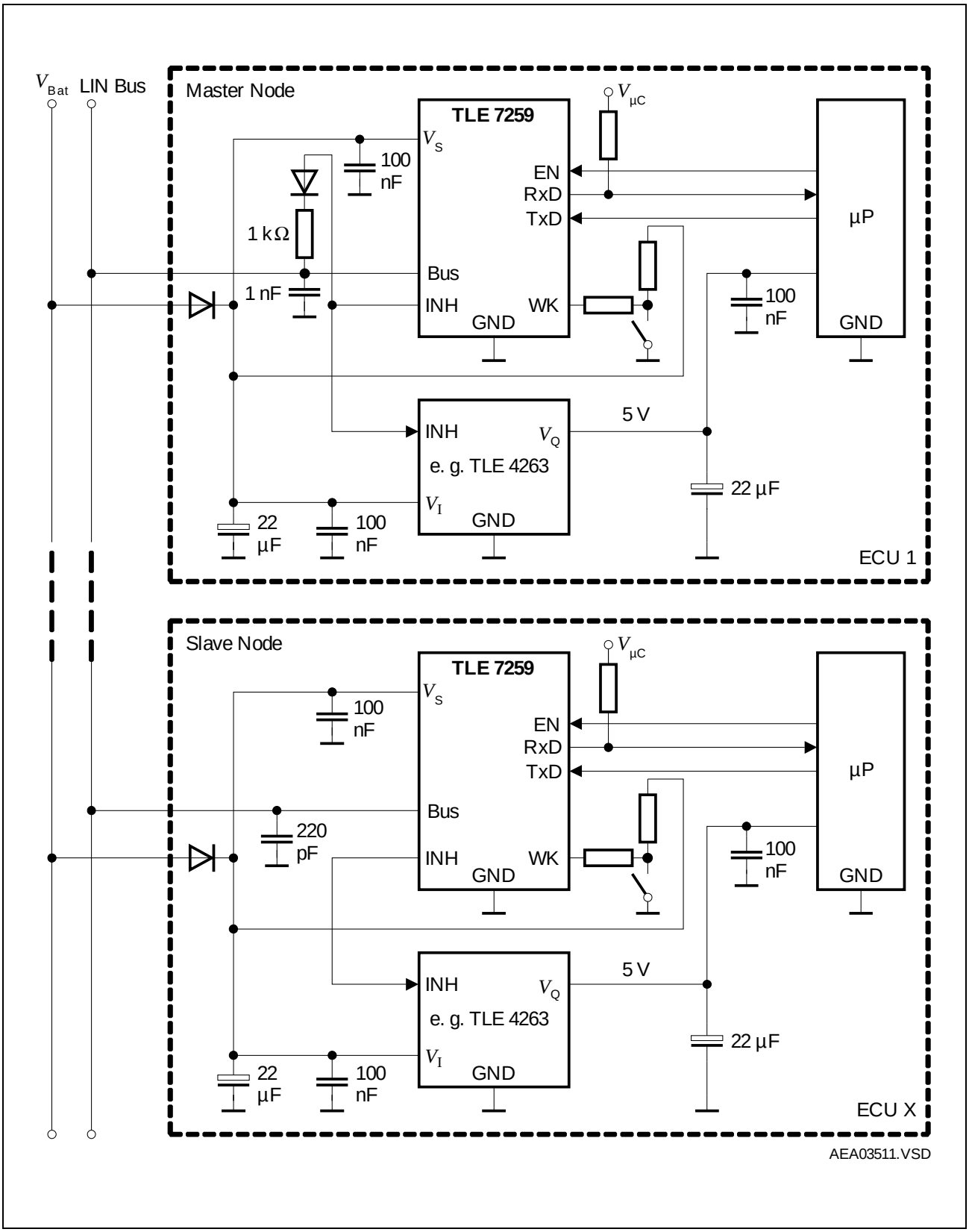


Figure 6 Application Circuit with Bus Short to GND Feature Applied

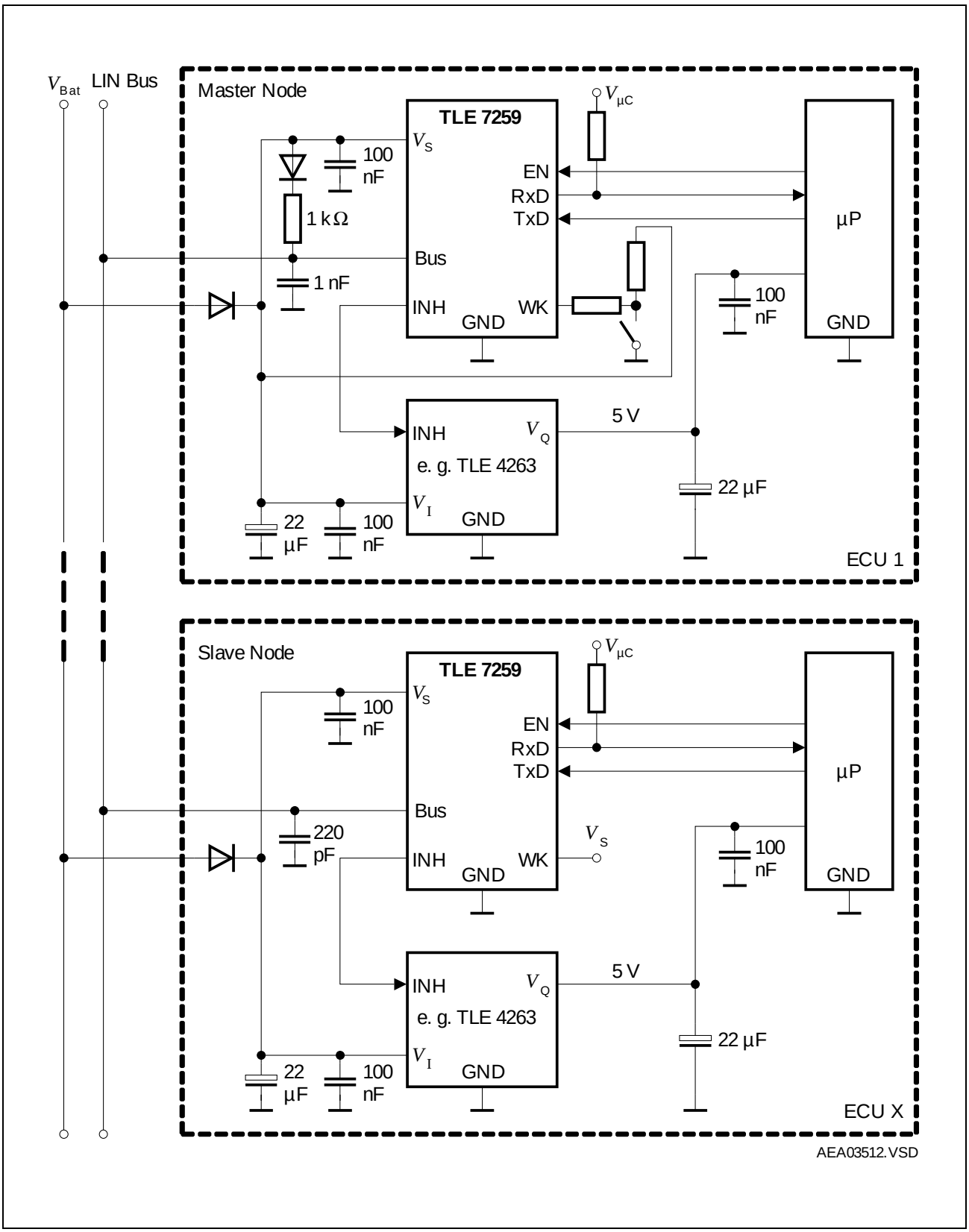
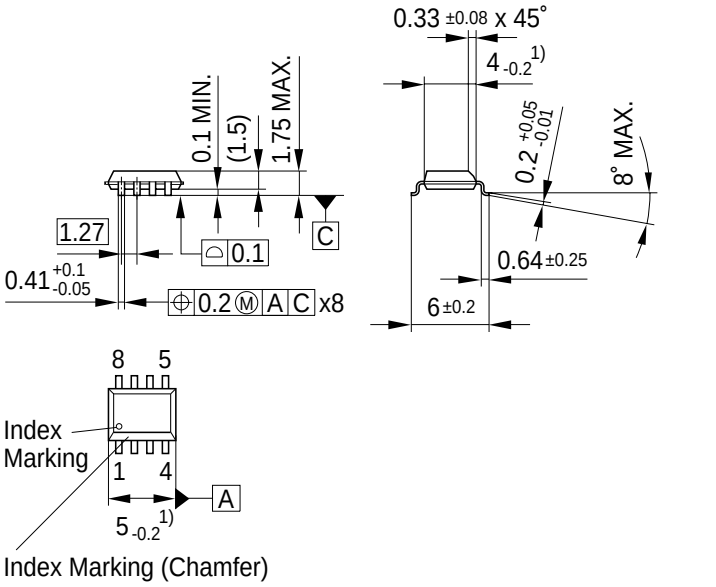


Figure 7 Application Circuit without Bus Short to GND Feature

Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS09032

Figure 8 **P-DSO-8-3** (Plastic Dual Small Outline)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

TLE 7259 G

Revision History:	**2004-12-13**	Rev. 1.3
Previous Version:	Rev.1.2	

Page	Subjects (major changes since last revision)
3	List of *features* change
3	*Description* changed
7	Description changed for the *BUS short to GND Feature*
9	**Table 2** *Output current at INH* deleted
9	$\mathbf{V_{INH,G}}$ *Inhibit Voltage* values changed
11	$\mathbf{I_S}$ Current consumption in stand-by mode added
11	**Table 4** voltage range changed to 7.0 V < V_S < 27 V
15	$\mathbf{t_{slopesym}}$ Slope symmetry updated
17	Duty cycle D3 (for worst case at 10.4 kBit/s) deleted
17	Duty cycle D4 (for worst case at 10.4 kBit/s) deleted
15	$\mathbf{t_{fslope}}$ *Slew rate falling edge* updated according to LIN 1.3 / 2.0
15	$\mathbf{t_{d(L),T}}$Propagation delay TxD LOW to bus (max: 4µs)
15	$\mathbf{t_{d(H),T}}$Propagation delay TxD HIGH to bus (max: 4µs)
	References to LIN 2.0 added