

Si6923DQ

P-Channel 2.5V Specified PowerTrench® MOSFET with Schottky Diode

General Description

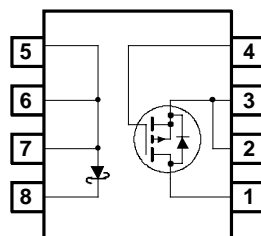
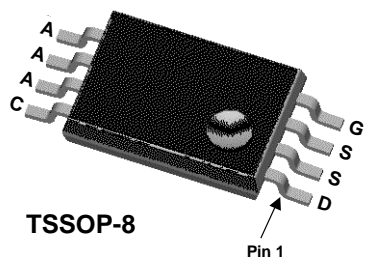
This P-Channel 2.5V specified MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It is combined with a low forward drop Schottky diode which is isolated from the MOSFET, providing a compact power solution for asynchronous DC/DC converter applications.

Applications

- DC/DC conversion

Features

- -3.5 A, -20 V. $R_{DS(ON)} = 0.045 \Omega @ V_{GS} = -4.5 V$
 $R_{DS(ON)} = 0.075 \Omega @ V_{GS} = -2.5 V$
- $V_F < 0.55 V @ 1 A$
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low profile TSSOP-8 package



MOSFET Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	-20	V
V_{GSS}	Gate-Source Voltage	± 12	V
I_D	Drain Current – Continuous (Note 1)	-3.5	A
	– Pulsed	-30	
P_D	MOSFET Power Dissipation (minimum pad) (Note 1)	1.2	W
	Schottky Power Dissipation (minimum pad) (Note 1)	1.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

Schottky Maximum Ratings

V_{RRM}	Repetitive Peak Reverse Voltage	20	V
I_F	Average Forward Current	1.5	A
I_{FM}	Peak Forward Current	30	A

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (minimum pad) (Note 1)	MOSFET: 115 Schottky: 130	$^\circ C/W$
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Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
6923	Si6923DQ	13"	16mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		-16		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.6	-1.0	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -4.5\text{ V}, I_D = -3.5\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -2.7\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -3.5\text{ A}, T_J = 125^\circ\text{C}$		36 56 49	45 75 72	m Ω
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-15			A
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -3.5\text{ A}$		13.2		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}$		1015		pF
C_{oss}	Output Capacitance	$f = 1.0\text{ MHz}$		446		pF
C_{riss}	Reverse Transfer Capacitance			118		pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -5\text{ V}, I_D = -1\text{ A}$		11	20	ns
t_r	Turn–On Rise Time	$V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		18	32	ns
$t_{d(off)}$	Turn–Off Delay Time			34	55	ns
t_f	Turn–Off Fall Time			34	55	ns
Q_g	Total Gate Charge	$V_{DS} = -5\text{ V}, I_D = -3.5\text{ A}$		9.7	16	nC
Q_{gs}	Gate–Source Charge	$V_{GS} = -4.5\text{ V}$		2.2		nC
Q_{gd}	Gate–Drain Charge			2.4		nC

Drain–Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain–Source Diode Forward Current				-1.25	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -1.25\text{ A}$ (Note 2)	-0.6		-1.2	V
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			100	nA

Schottky Diode Characteristics

I_R	Reverse Leakage	$V_R = 20\text{ V}$	$T_J = 25^\circ\text{C}$	0.6	50	μA
			$T_J = 125^\circ\text{C}$	1	8	mA
V_F	Forward Voltage	$I_F = 1\text{ A}$	$T_J = 25^\circ\text{C}$	0.48	0.55	V
			$T_J = 125^\circ\text{C}$	0.42	0.50	V
C_T	Junction Capacitance	$V_R = 10\text{ V}$		50		pF

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$R_{\theta JA}$ is 115 $^\circ\text{C}/\text{W}$ for the MOSFET and 130 $^\circ\text{C}/\text{W}$ for the Schottky Diode when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

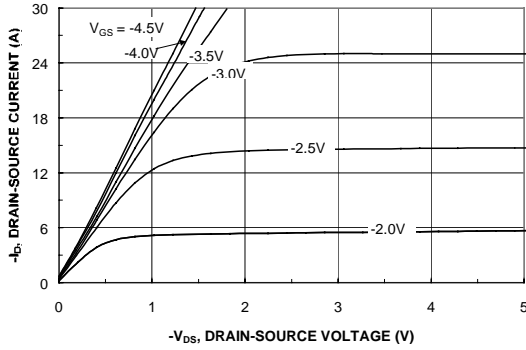


Figure 1. On-Region Characteristics.

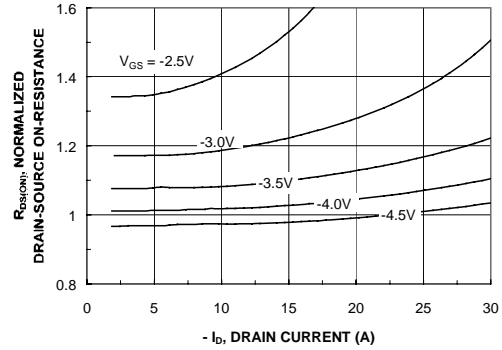


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

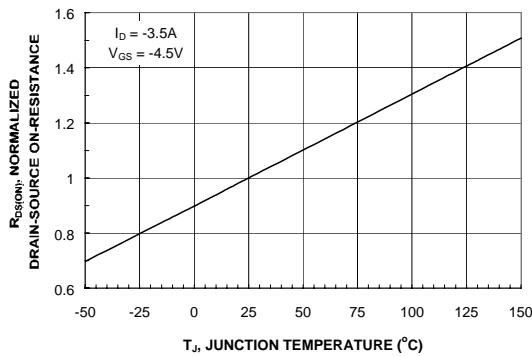


Figure 3. On-Resistance Variation with Temperature.

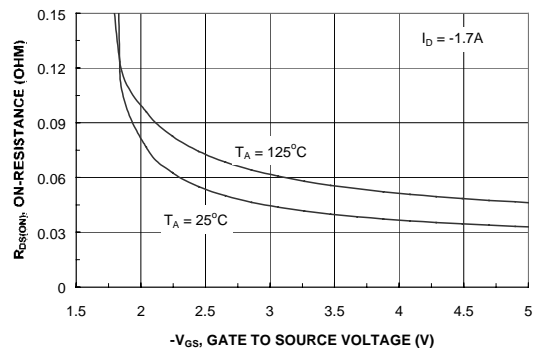


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

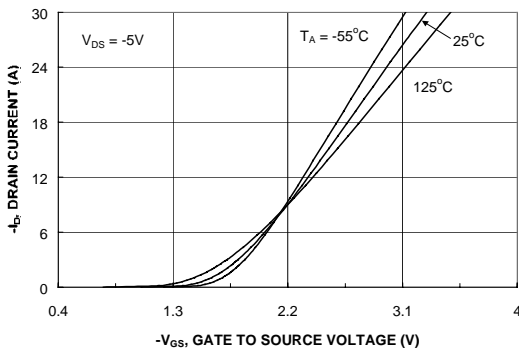


Figure 5. Transfer Characteristics.

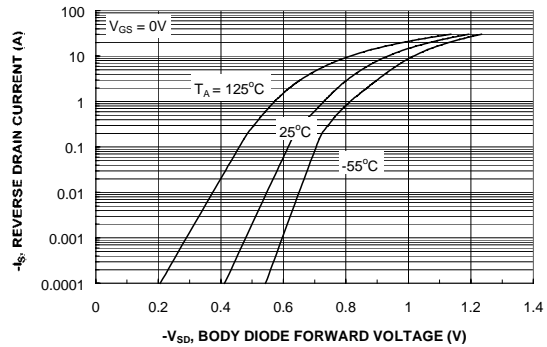


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

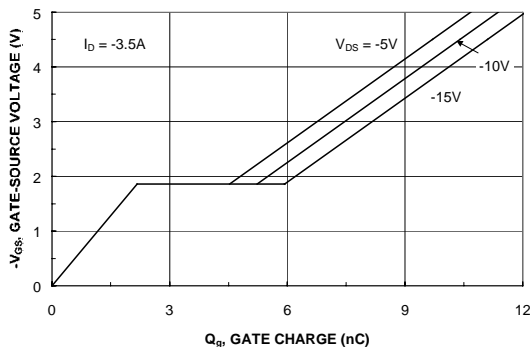


Figure 7. Gate Charge Characteristics.

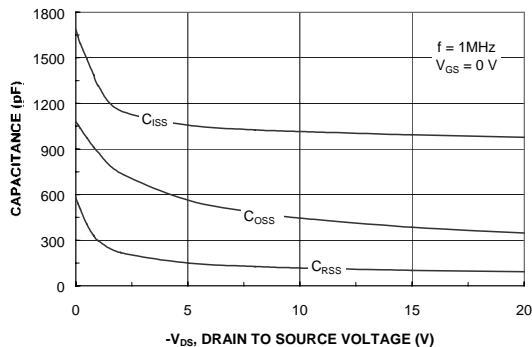


Figure 8. Capacitance Characteristics.

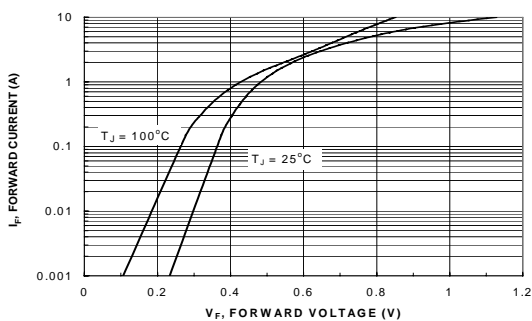


Figure 9. Schottky Diode Forward Voltage.

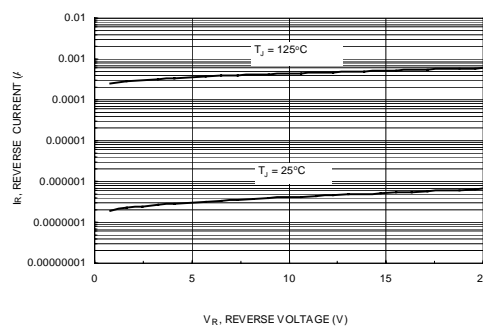


Figure 10. Schottky Diode Reverse Current.

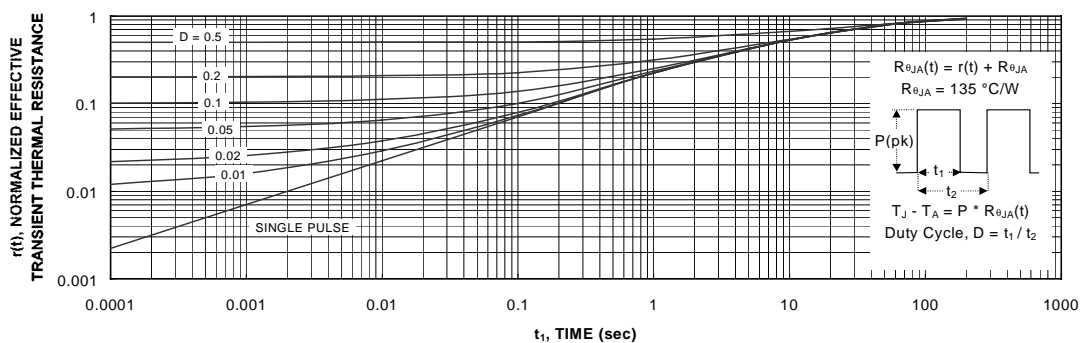


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1.
 Transient thermal response will change depending on the circuit board design.

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