

# 1GB – 2x64Mx64, SDRAM UNBUFFERED

## FEATURES

- PC100 and PC133 compatible
- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- Available with "WP" write protect on pin 81 option
  - W3DG63126V-D2
- 3.3V ± 0.3V Power Supply
- 168 Pin DIMM JEDEC
  - PCB: 30.50mm (1.20in)

## DESCRIPTION

The W3DG64126V is a 2x64Mx64 synchronous DRAM module which consists of sixteen 64Mx8 SDRAM components in TSOP II package and one 2K EEPROM in an 8 Pin TSSOP package for Serial Presence Detect which are mounted on a 168 Pin DIMM multilayer FR4 Substrate.

\* This product is subject to change without notice.

NOTE: Consult factory for availability of:

- Lead-free products
- Vendor source control option
- Industrial temperature option

## PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V <sub>SS</sub>	29	DQM1	57	DQ18	85	V <sub>SS</sub>	113	DQM5	141	DQ50
2	DQ0	30	CS0#	58	DQ19	86	DQ32	114	CS1#	142	DQ51
3	DQ1	31	DNU	59	V <sub>CC</sub>	87	DQ33	115	RAS#	143	V <sub>CC</sub>
4	DQ2	32	V <sub>SS</sub>	60	DQ20	88	DQ34	116	V <sub>SS</sub>	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	V <sub>CC</sub>	34	A2	62	*V <sub>REF</sub>	90	V <sub>CC</sub>	118	A3	146	*V <sub>REF</sub>
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	DNU
8	DQ5	36	A6	64	V <sub>SS</sub>	92	DQ37	120	A7	148	V <sub>SS</sub>
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	V <sub>SS</sub>	40	V <sub>CC</sub>	68	V <sub>SS</sub>	96	V <sub>SS</sub>	124	V <sub>CC</sub>	152	V <sub>SS</sub>
13	DQ9	41	V <sub>CC</sub>	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	V <sub>SS</sub>	71	DQ26	99	DQ43	127	V <sub>SS</sub>	155	DQ58
16	DQ12	44	DNU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2#	73	V <sub>CC</sub>	101	DQ45	129	CS3#	157	V <sub>CC</sub>
18	V <sub>CC</sub>	46	DQM2	74	DQ28	102	V <sub>CC</sub>	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DNU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CBO	49	V <sub>CC</sub>	77	DQ31	105	*CB4	133	V <sub>CC</sub>	161	DQ63
22	*CB1	50	NC	78	V <sub>SS</sub>	106	*CB5	134	NC	162	V <sub>SS</sub>
23	V <sub>SS</sub>	51	NC	79	CK2	107	V <sub>SS</sub>	135	NC	163	CK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	***WP	109	NC	137	*CB7	165	**SA0
26	V <sub>CC</sub>	54	V <sub>SS</sub>	82	**SDA	110	V <sub>CC</sub>	138	V <sub>SS</sub>	166	**SA1
27	WE#	55	DQ16	83	**SCL	111	CAS#	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	V <sub>CC</sub>	112	DQM4	140	DQ49	168	V <sub>CC</sub>

## PIN NAMES

A0 – A12	Address input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CK0-CK3	Clock input
CKE0, CKE1	Clock Enable input
CS0# - CS3#	Chip select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-7	DQM
V <sub>CC</sub>	Power Supply
V <sub>SS</sub>	Ground
SDA	Serial data I/O
SCL	Serial clock
DNU	Do not use
NC	No Connect
WP	Write Protect

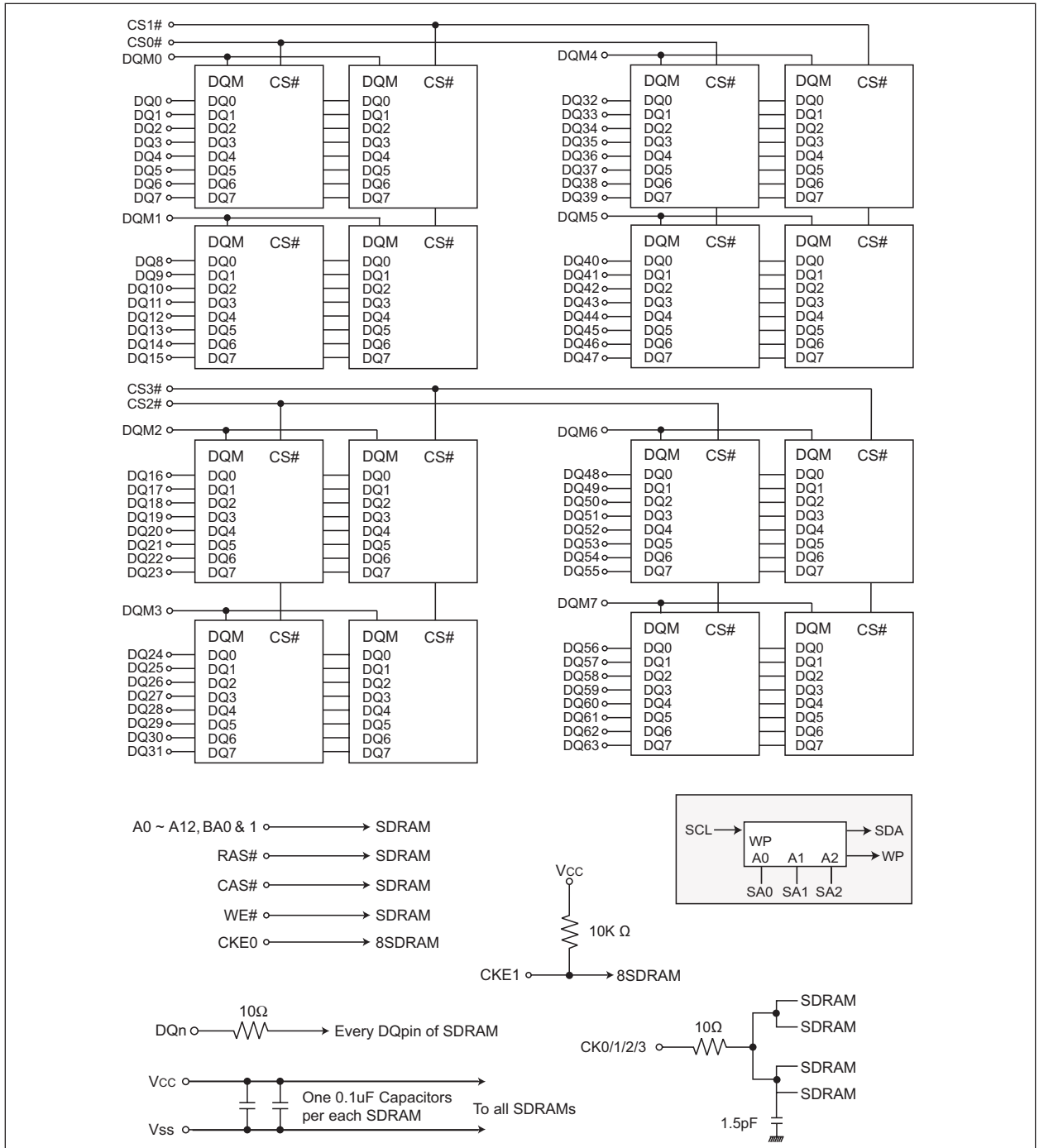
\* These pins are not used in this module.

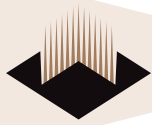
\*\* These pins should be NC in the system which does not support SPD.

\*\*\* WP available on the W3DG63126V-D2 only.



FUNCTIONAL BLOCK DIAGRAM





**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Units
Voltage on any pin relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-1.0 ~ 4.6	V
Voltage on V <sub>CC</sub> supply relative to V <sub>SS</sub>	V <sub>CC</sub> , V <sub>CCA</sub>	-1.0 ~ 4.6	V
Storage Temperature	TSTG	-55 ~ +150	°C
Power Dissipation	PD	8	W
Short Circuit Current	IOS	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.  
 Functional operation should be restricted to recommended operating condition.  
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

Voltage Referenced to: V<sub>SS</sub> = 0V, 0°C ≤ T<sub>A</sub> ≤ +70°C

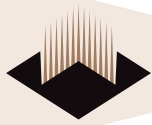
Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V	
Input High Voltage	V <sub>IH</sub>	2.0	3.0	V <sub>CCA</sub> +0.3	V	1
Input Low Voltage	V <sub>IL</sub>	-0.3	—	0.8	V	2
Output High Voltage	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -2mA
Output Low Voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = -2mA
Input Leakage Current	I <sub>LI</sub>	-10	—	10	µA	3

Note:  
 1. V<sub>IH</sub> (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.  
 2. V<sub>IL</sub> (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.  
 3. Any input 0V ≤ V<sub>IN</sub> ≤ V<sub>CC</sub>  
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

**CAPACITANCE**

T<sub>A</sub> = 25°C, f = 1MHz, V<sub>CC</sub> = 3.3V, V<sub>REF</sub>=1.4V ± 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C <sub>IN1</sub>	66	pF
Input Capacitance (RAS#,CAS#,WE#)	C <sub>IN2</sub>	66	pF
Input Capacitance (CKE0-CKE1)	C <sub>IN3</sub>	66	pF
Input Capacitance (CK0-CK3)	C <sub>IN4</sub>	16	pF
Input Capacitance (CS0#-CS3#)	C <sub>IN5</sub>	21	pF
Input Capacitance (DQM0-DQM7)	C <sub>IN6</sub>	15	pF
Input Capacitance (BA0-BA1)	C <sub>IN7</sub>	66	pF
Data input/output capacitance (DQ0-DQ63)	C <sub>OUT</sub>	15	pF



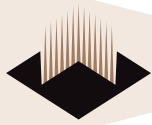
## I<sub>DD</sub> SPECIFICATIONS AND CONDITIONS

V<sub>CC</sub>, V<sub>CCQ</sub> = +3.3V ±0.3V; SDRAM component values only

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES	
		7	7.5	10			
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; t <sub>RC</sub> = t <sub>RC</sub> (MIN)	I <sub>DD1</sub>	1,920	1,760	1,760	mA	1	
STANDBY CURRENT: Power-Down Mode; All device devicebanks idle; CKE = LOW	I <sub>DD2</sub>	56	56	56	mA		
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; All device banks active after t <sub>RCD</sub> met; No accesses in progress	I <sub>DD3</sub>	720	720	720	mA		
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All device banks active	I <sub>DD4</sub>	2,000	1,840	1,840	mA	1	
AUTO REFRESH CURRENT	t <sub>RFC</sub> = t <sub>RFC</sub> (MIN)	I <sub>DD5</sub>	3,920	3,920	3,920	mA	2
CKE = HIGH; CS# = HIGH	t <sub>RFC</sub> = 7.8125μs	I <sub>DD6</sub>	96	96	96	mA	
SELF REFRESH CURRENT: CKE < 0.2V	I <sub>DD7</sub>	96	96	96	mA		

Notes:

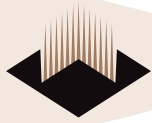
1. Measured with outputs open.
2. Refresh period is 64ms.



**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

V<sub>CC</sub>, V<sub>CCQ</sub> = +3.3V ±0.3V

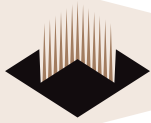
AC CHARACTERISTICS		SYMBOL	7		7.5		10		UNITS	NOTE
PARAMETER			MIN	MAX	MIN	MAX	MIN	MAX		
Access time from CLK (pos. edge)	CL = 3	t <sub>AC(3)</sub>		5.4		5.4		6	ns	27
	CL = 2	t <sub>AC(2)</sub>		5.4		6		6	ns	
Address hold time		t <sub>AH</sub>	0.8		0.8		1		ns	
Address setup time		t <sub>AS</sub>	1.5		1.5		2		ns	
CLK high-level width		t <sub>CH</sub>	2.5		2.5		3		ns	
CLK low-level width		t <sub>CL</sub>	2.5		2.5		3		ns	
Clock cycle time	CL = 3	t <sub>CK(3)</sub>	7		7.5		8		ns	23
	CL = 2	t <sub>CK(2)</sub>	7.5		10		10		ns	23
CKE hold time		t <sub>CKH</sub>	0.8		0.8		1		ns	
CKE setup time		t <sub>CKS</sub>	1.5		1.5		2		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		t <sub>CMH</sub>	0.8		0.8		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		t <sub>CMS</sub>	1.5		1.5		2		ns	
Data-in hold time		t <sub>DH</sub>	0.8		0.8		1		ns	
Data-in setup time		t <sub>DS</sub>	1.5		1.5		2		ns	
Data-out high-impedance time	CL = 3	t <sub>HZ(3)</sub>		5.4		5.4		6	ns	10
	CL = 2	t <sub>HZ(2)</sub>		5.4		6		6	ns	10
Data-out low-impedance time		t <sub>LZ</sub>	1		1		1		ns	
Data-out hold time (load)		t <sub>OH</sub>	2.7		2.7		2.7		ns	
Data-out hold time (no load)		t <sub>OHN</sub>	1.8		1.8		1.8		ns	28
ACTIVE to PRECHARGE command		t <sub>RAS</sub>	37	120,000	44	120,000	50	120,000	ns	
ACTIVE to ACTIVE command period		t <sub>RC</sub>	60		66		66		ns	
ACTIVE to READ or WRITE delay		t <sub>RCD</sub>	15		20		20		ns	
Refresh period		t <sub>REF</sub>	64		64		64		ms	
AUTOREFRESH period		t <sub>RFC</sub>	66		66		66		ns	
PRECHARGE command period		t <sub>RP</sub>	15		20		20		ns	
ACTIVE bank a to ACTIVE bank b command		t <sub>RRD</sub>	14		15		15		ns	
Transition time		t <sub>T</sub>	0.3	1.2	0.3	1.2	0.3	1.2	ns	7
WRITE recovery time		t <sub>WR</sub>	1 CLK + 7ns		1 CLK + 7.5ns		1 CLK + 7.5ns			24
			14		15		15		ns	25
Exit SELF REFRESH to ACTIVE command		t <sub>XSR</sub>	67		75		80		ns	20



**AC FUNCTIONAL CHARACTERISTICS**

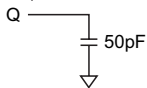
V<sub>CC</sub>, V<sub>CCQ</sub> = +3.3V ±0.3V

PARAMETER	SYMBOL	7	7.5	10	UNITS	NOTES
READ/WRITE command to READ/WRITE command	t <sub>CCD</sub>	1	1	1	t <sub>CK</sub>	17
CKE to clock disable or power-down entry mode	t <sub>CKED</sub>	1	1	1	t <sub>CK</sub>	14
CKE to clock enable or power-down exit setup mode	t <sub>PED</sub>	1	1	1	t <sub>CK</sub>	14
DQM to input data delay	t <sub>DQD</sub>	0	0	0	t <sub>CK</sub>	17
DQM to data mask during WRITES	t <sub>DQM</sub>	0	0	0	t <sub>CK</sub>	17
DQMto data high-impedance during READs	t <sub>DQZ</sub>	2	2	2	t <sub>CK</sub>	17
WRITE command to input data delay	t <sub>DWD</sub>	0	0	0	t <sub>CK</sub>	17
Data-into ACTIVE command	t <sub>DAL</sub>	4	5	5	t <sub>CK</sub>	15, 21
Data-into PRECHARGE command	t <sub>DPL</sub>	2	2	2	t <sub>CK</sub>	16, 21
Last data-in to burst STOP command	t <sub>BDL</sub>	1	1	1	t <sub>CK</sub>	17
Last data-in to new READ/WRITE command	t <sub>CDL</sub>	1	1	1	t <sub>CK</sub>	17
Lastdata-into PRECHARGE command	t <sub>RDL</sub>	2	2	2	t <sub>CK</sub>	16, 21
LOADMODEREGISTER command to ACTIVE or REFRESH command	t <sub>MRD</sub>	2	2	2	t <sub>CK</sub>	26
Data-out to high-impedance from PRECHARGE command	CL = 3	t <sub>ROH(3)</sub>	3	3	t <sub>CK</sub>	17
	CL = 2	t <sub>ROH(2)</sub>	2	2	t <sub>CK</sub>	17



## Notes

1. All voltages referenced to  $V_{SS}$ .
2. This parameter is sampled.  $V_{CC}$ ,  $V_{CCQ} = +3.3V$ ;  $T_A = 25^\circ C$ ; pin under test biased at 1.4V;  $f = 1$  MHz.
3.  $I_{DD}$  is dependent on output loading and cycle rates. Specified values are obtained with mini-mum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100 $\mu s$  is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. ( $V_{CC}$  and  $V_{CCQ}$  must be powered up simultaneously.  $V_{SS}$  and  $V_{SSQ}$  must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the tREF refresh requirement is exceeded.
7. AC characteristics assume  $t_r = 1$  ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a mono-tonic manner.
9. Outputs measured at 1.5V with equivalent load:



10.  $t_{HZ}$  defines the time at which the output achieves the open circuit condition; it is not a reference to  $V_{OH}$  or  $V_{OL}$ . The last valid data element will meet  $t_{OH}$  before going High-Z.
11. AC timing and  $I_{DD}$  tests have  $V_{IL} = 0V$  and  $V_{IH} = 3V$  with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) and no longer at the 1.5V crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are other-wise at valid  $V_{IH}$  or  $V_{IL}$  levels.
13.  $I_{DD}$  specifications are tested after the device is properly initialized.
14. Timing actually specified by  $t_{CKS}$ ; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by  $t_{WR}$  plus  $t_{RP}$ ; clock(s) specified as a reference only at minimum cycle rate.

16. Timing actually specified by  $t_{WR}$ .
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The  $I_{DD}$  current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on  $t_{CK} = 10$ ns for 10, and  $t_{CK} = 7.5$ ns for 7 and 7.5.
22.  $V_{IH}$  overshoot:  $V_{IH}$  (MAX) =  $V_{CCQ} + 2V$  for a pulse width  $\leq 3$ ns, and the pulse width cannot be greater than one third of the cycle rate.  $V_{IL}$  under-shoot:  $V_{IL}$  (MIN) =  $-2V$  for a pulse width  $\leq 3$ ns.
23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including  $t_{WR}$ , and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget ( $t_{RP}$ ) begins 7ns for 7; 7.5ns for 7.5 and 7.5ns for 10 after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
25. Precharge mode only.
26. JEDEC and PC133, PC100 specify three clocks.
27.  $t_{AC}$  for 7/7.5 at  $CL = 3$  with no load is 4.6ns and is guaranteed by design.
28. Parameter guaranteed by design.







### Document Title

1GB - 2x64Mx64, SDRAM UNBUFFERED

### Revision History

Rev #	History	Release Date	Status
Rev A	Created	5-3-02	Advanced
Rev B	Corrected mechanical drawing	5-21-02	Advanced
Rev 0	0.1 Update CAP and I <sub>DD</sub> specs 0.2 Moved from Advanced to Preliminary	12-04	Preliminary
Rev 1	1.1 Added lead-free and RoHS notes 1.2 Added source control notes 1.3 Added industrial temperature options 1.4 Moved Preliminary to Final	1-05	Final