

IRF740AS/LPbF
HEXFET® Power MOSFET

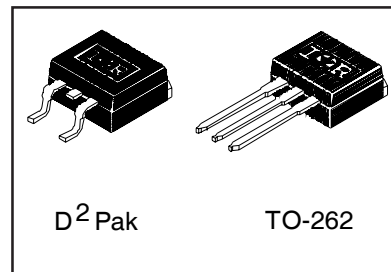
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High speed power switching
- Lead-Free

V _{DSS}	R _{ds(on)} max	I _D
400V	0.55Ω	10A

Benefits

- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss specified (See AN 1001)



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V [ⓐ]	10	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V [ⓐ]	6.3	
I _{DM}	Pulsed Drain Current [ⓑ]	40	
P _D @ T _A = 25°C	Power Dissipation	3.1	W
P _D @ T _C = 25°C	Power Dissipation	125	
	Linear Derating Factor	1.0	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt [ⓒ]	5.9	V/ns
T _J	Operating Junction and	-55 to + 150	
T _{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Typical SMPS Topologies:

- Single transistor Flyback Xfmr. Reset
- Single Transistor Forward Xfmr. Reset
(Both for US Line Input only)

Notes [ⓐ] through [ⓔ] are on page 10

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	400	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.48	—		$V/^\circ\text{C}$ Reference to $25^\circ\text{C}, I_D = 1mA$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.55	Ω	$V_{GS} = 10V, I_D = 6.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 400V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 320V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	4.9	—	—	S	$V_{DS} = 50V, I_D = 6.0A$ ⑥
Q_g	Total Gate Charge	—	—	36	nC	$I_D = 10A$ $V_{DS} = 320V$ $V_{GS} = 10V$, See Fig. 6 and 13 ④ ⑥
Q_{gs}	Gate-to-Source Charge	—	—	9.9		
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	16		
$t_{d(on)}$	Turn-On Delay Time	—	10	—		
t_r	Rise Time	—	35	—	ns	$V_{DD} = 200V$ $I_D = 10A$ $R_G = 10\Omega$ $R_D = 19.5\Omega$, See Fig. 10 ④ ⑥
$t_{d(off)}$	Turn-Off Delay Time	—	24	—		
t_f	Fall Time	—	22	—		
C_{iss}	Input Capacitance	—	1030	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0MHz$, See Fig. 5 ⑥
C_{oss}	Output Capacitance	—	170	—		
C_{riss}	Reverse Transfer Capacitance	—	7.7	—		
C_{oss}	Output Capacitance	—	1490	—		
C_{oss}	Output Capacitance	—	52	—		
$C_{oss\ eff.}$	Effective Output Capacitance	—	61	—		

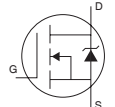
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ② ⑥	—	630	mJ
I_{AR}	Avalanche Current ①	—	10	A
E_{AR}	Repetitive Avalanche Energy ①	—	12.5	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.0	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)*	—	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	10	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	40		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	$T_J = 25^\circ\text{C}, I_S = 10A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	240	360	ns	$T_J = 25^\circ\text{C}, I_F = 10A$
Q_{rr}	Reverse Recovery Charge	—	1.9	2.9	μC	$di/dt = 100A/\mu\text{s}$ ④ ⑥
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

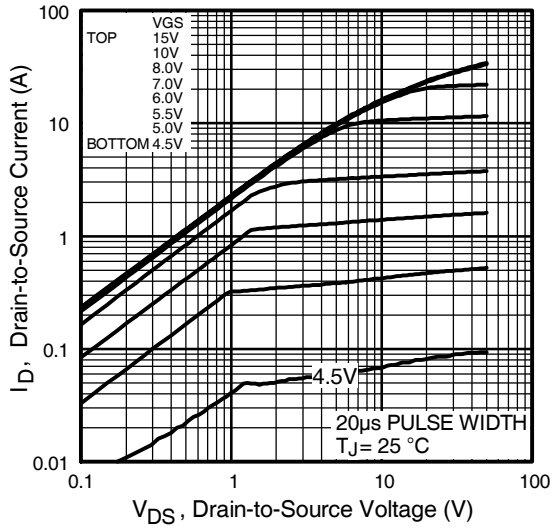


Fig 1. Typical Output Characteristics

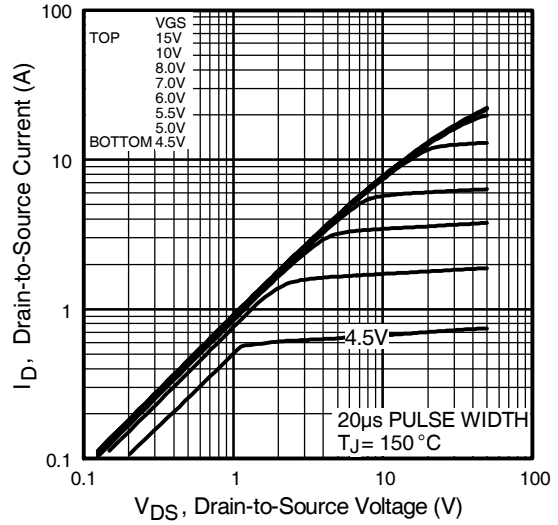


Fig 2. Typical Output Characteristics

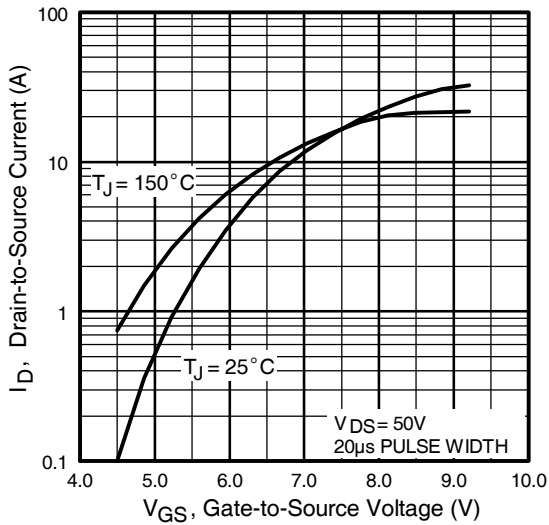


Fig 3. Typical Transfer Characteristics

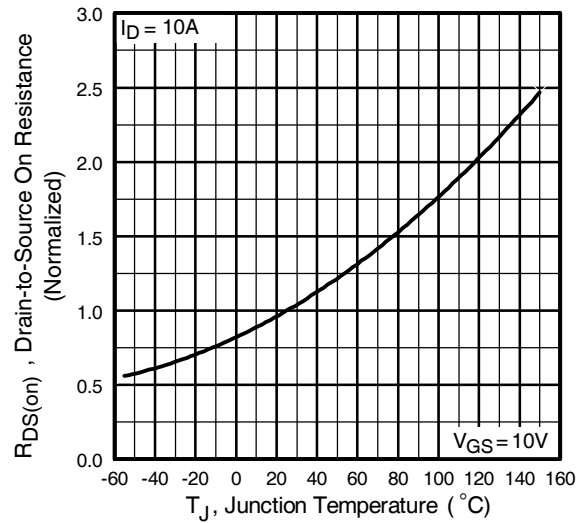


Fig 4. Normalized On-Resistance Vs. Temperature

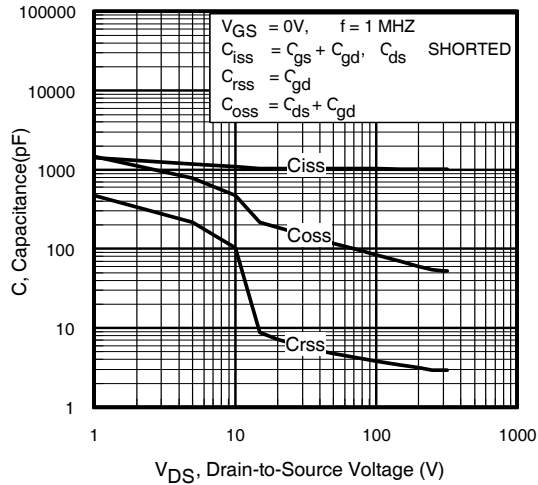


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

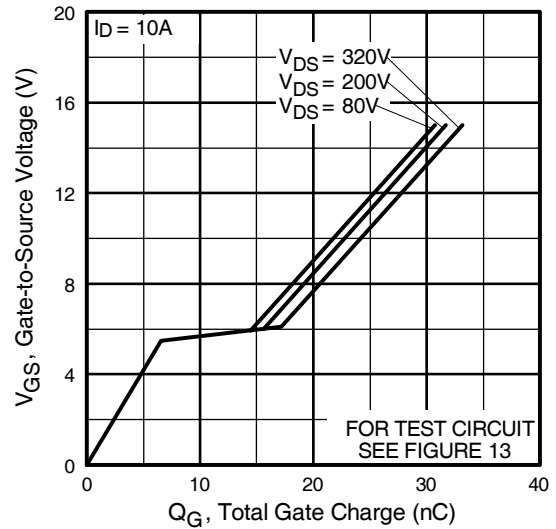


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

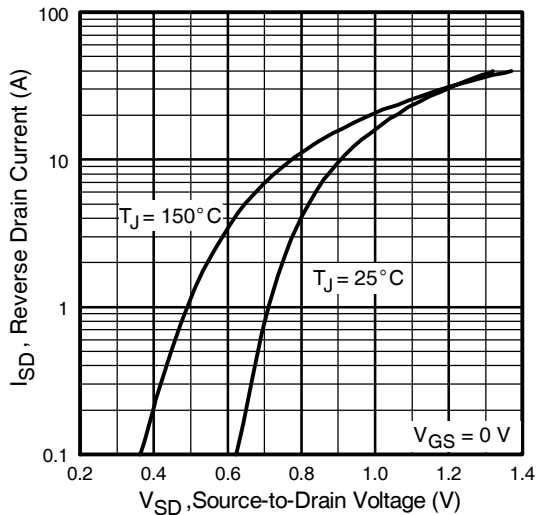


Fig 7. Typical Source-Drain Diode Forward Voltage

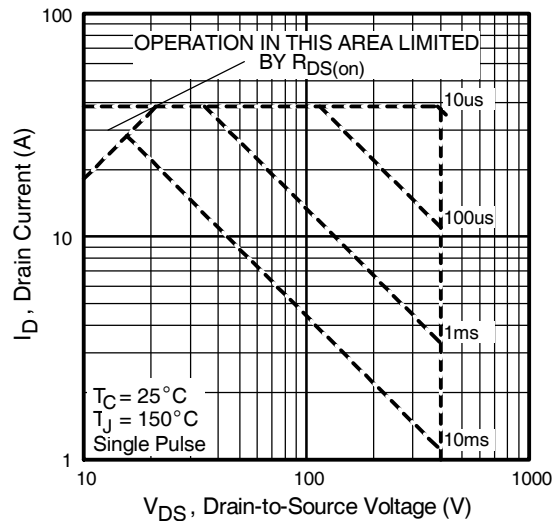


Fig 8. Maximum Safe Operating Area

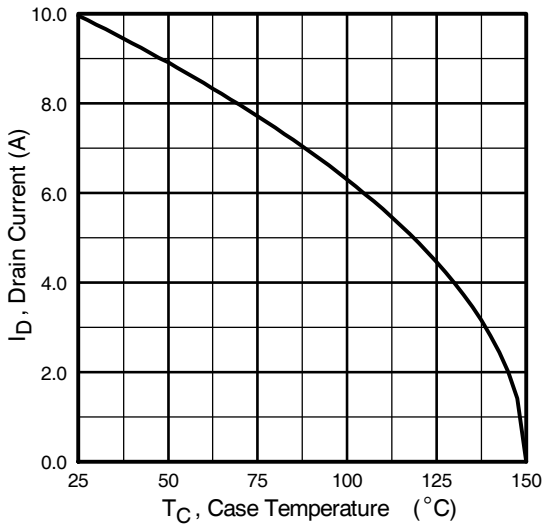


Fig 9. Maximum Drain Current Vs. Case Temperature



Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

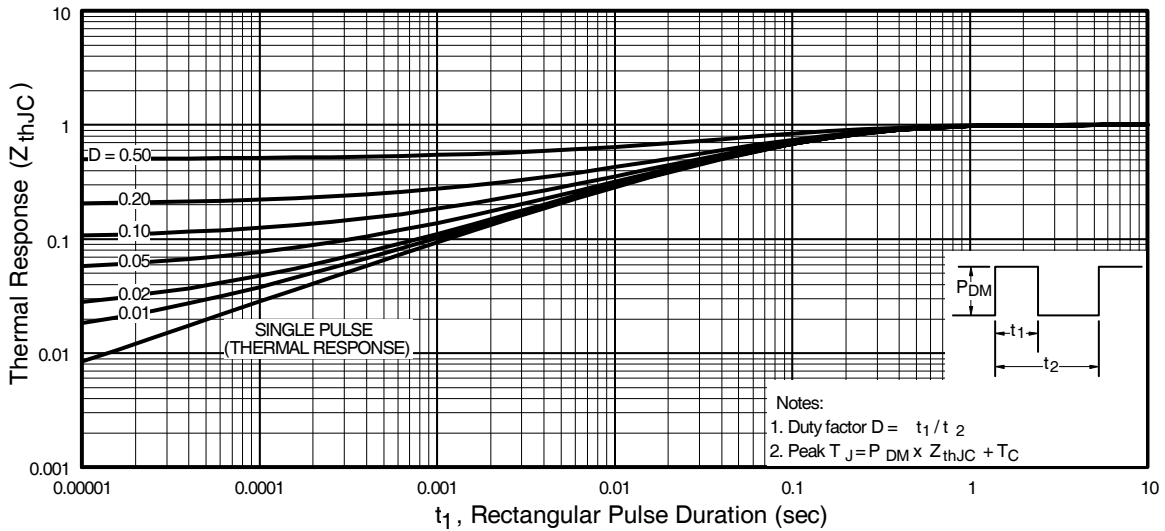


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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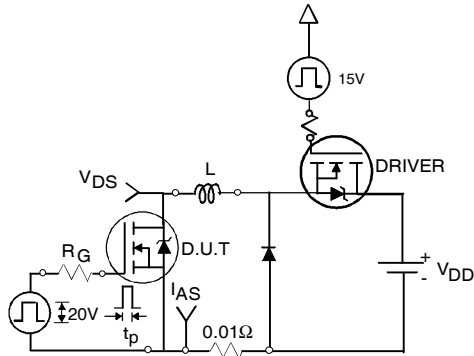


Fig 12a. Unclamped Inductive Test Circuit

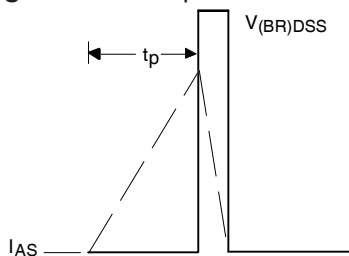


Fig 12b. Unclamped Inductive Waveforms

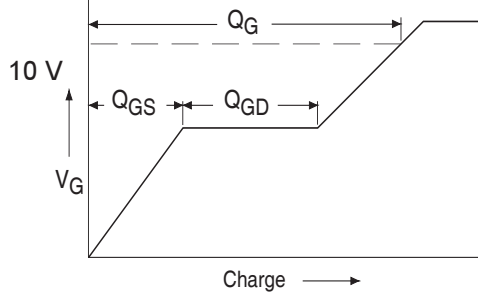


Fig 13a. Basic Gate Charge Waveform

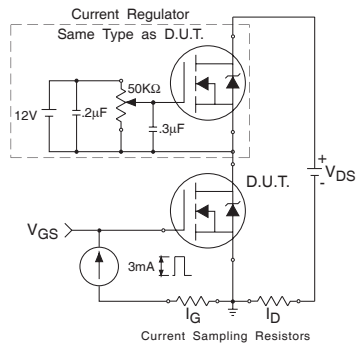


Fig 13b. Gate Charge Test Circuit

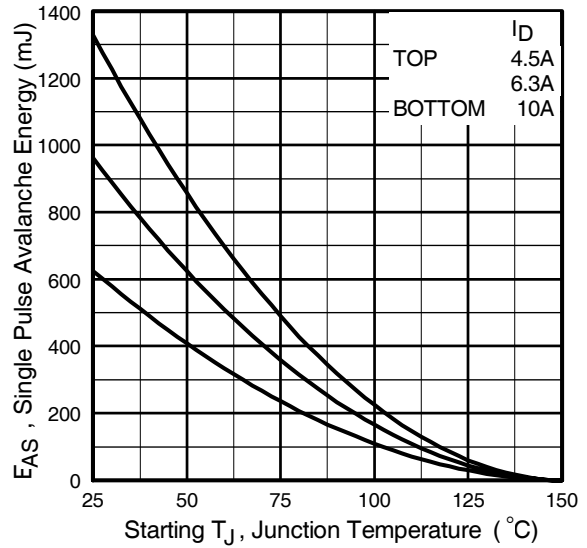


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

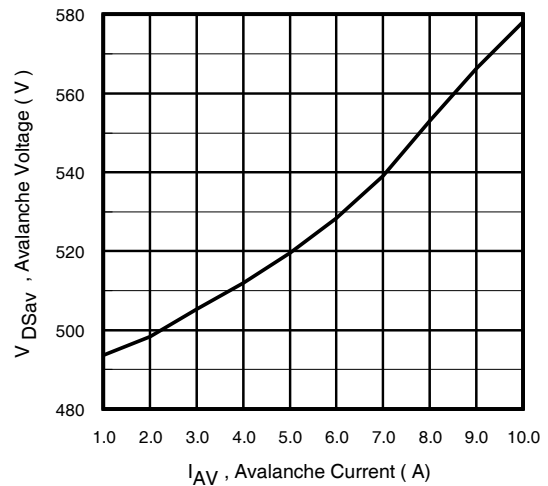
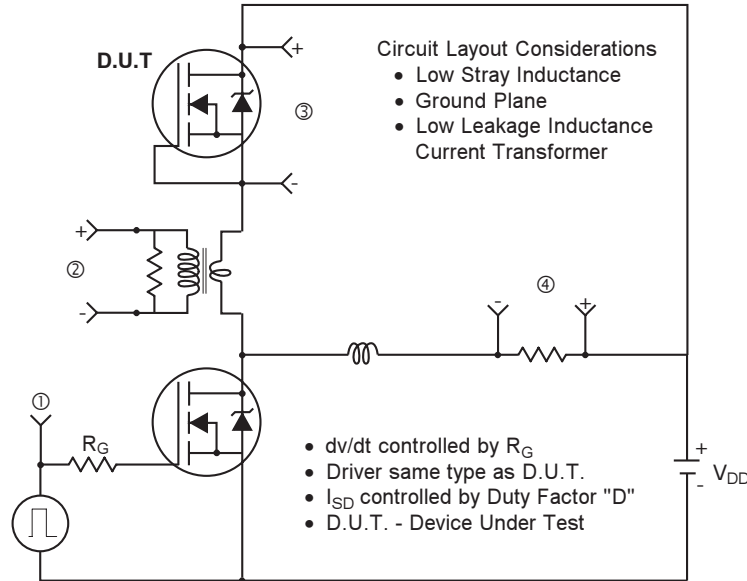


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

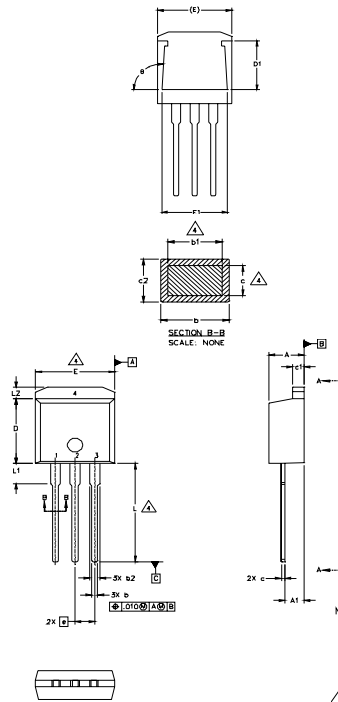
Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

TO-262 Package Outline



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.38	0.63	.015	.025	
c1	1.14	1.40	.045	.055	3
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	
D1	5.33		.210		3
E	9.65	10.67	.380	.420	
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT

- 1 - GATE
- 2 - COLLECTOR
- 3 - EMITTER

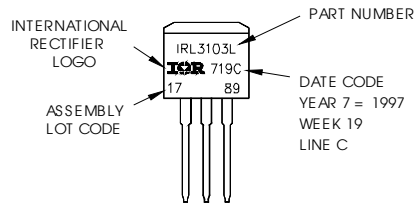
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION- INCH.

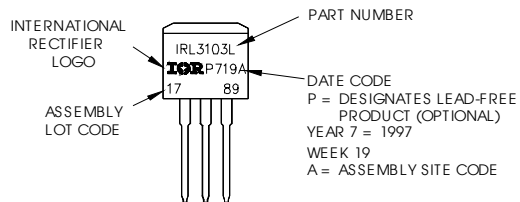
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



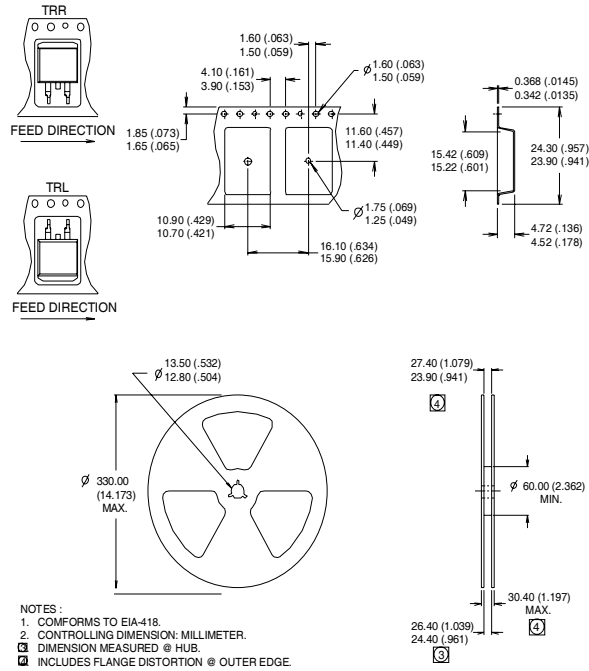
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D²Pak Tape & Reel Infomation



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
 - ② Starting $T_J = 25^\circ\text{C}$, $L = 12.6\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 10\text{A}$. (See Figure 12)
 - ③ $I_{SD} \leq 10\text{A}$, $di/dt \leq 330\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
 - ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
 - ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
 - ⑥ Uses IRF740A data and test conditions
- * When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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