

# MOS FIELD EFFECT TRANSISTOR 2SK4081

### **SWITCHING N-CHANNEL POWER MOS FET**

#### **DESCRIPTION**

The 2SK4081 is N-channel MOS FET device that features a low gate charge and excellent switching characteristics, and designed for high voltage applications such as switching power supply, AC adapter.

#### **FEATURES**

• Low on-state resistance

 $R_{DS(on)} = 5 \Omega MAX. (V_{GS} = 10 V, I_D = 1.0 A)$ 

Low gate charge

 $Q_G = 7.2 \text{ nC TYP}$ . ( $V_{DD} = 450 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ ,  $I_D = 2.0 \text{ A}$ )

- Gate voltage rating: ±30 V
- · Avalanche capability ratings

#### <R> ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE	
2SK4081-S15-AY Note	Pure Sn (Tin)	Tube 70 p/tube	TO-251 (MP-3-a) typ. 0.39 g	
2SK4081(1)-S27-AY Note		Tube 75 p/tube	TO-251 (MP-3-b) typ. 0.34 g	
2SK4081-ZK-E1-AY Note		Tape 2500 p/reel	TO 050 (MD 07K) L 0 07 .	
2SK4081-ZK-E2-AY Note			TO-252 (MP-3ZK) typ. 0.27 g	

Note Pb-free (This product does not contain Pb in external electrode.)

#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V) 600 Voss Gate to Source Voltage (VDS = 0 V) Vgss ±30 Drain Current (DC) (Tc = 25°C) ID(DC) ±2.0 Drain Current (pulse) Note1 ID(pulse)  $\pm 8.0$ Total Power Dissipation (Tc = 25°C)  $P_{T1}$ 30 W Total Power Dissipation (T<sub>A</sub> = 25°C) Note2 P<sub>T2</sub> 1.0 Channel Temperature 150  $\mathsf{T}_{\mathsf{ch}}$ °C Tstg Storage Temperature -55 to +150 °C Single Avalanche Current Note3 las 1.4 Α Single Avalanche Energy Note3 Eas 117 mJ (TO-251)



(TO-252)



**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

- 2. Mounted on glass epoxy board of 40 mm x 40 mm x 1.6 mm
- 3. Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 150 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20  $\rightarrow$  0 V

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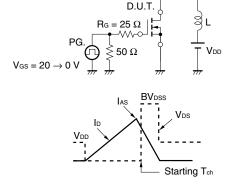
sales representative for availability and additional information.

### **ELECTRICAL CHARACTERISTICS (TA = 25°C)**

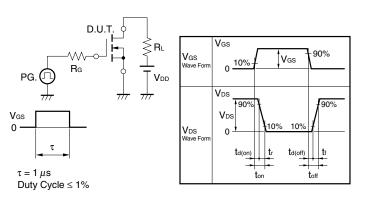
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V			10	μΑ
Gate Leakage Current	Igss	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V			±100	nA
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	2.5	3.0	3.5	٧
Forward Transfer Admittance Note	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.0 A	0.35			S
Drain to Source On-state Resistance Note	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.0 A		4.2	5	Ω
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V,		230		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V,		95		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		11		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 150 V, I <sub>D</sub> = 1.0 A,		11		ns
Rise Time	tr	V <sub>GS</sub> = 10 V,		7		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		13		ns
Fall Time	tf			13.5		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 450 V,		7.2		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V,		2.9		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 2.0 A		3.0		nC
Body Diode Forward Voltage Note	V <sub>F(S-D)</sub>	I <sub>F</sub> = 2.0 A, V <sub>GS</sub> = 0 V		0.87	1.5	V
Reverse Recovery Time	trr	I <sub>F</sub> = 2.0 A, V <sub>GS</sub> = 0 V,		175		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/µs		550		nC

Note Pulsed

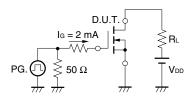
### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**



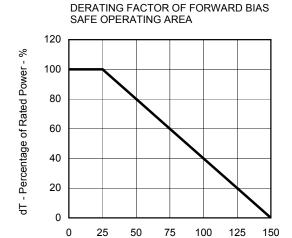
### TEST CIRCUIT 2 SWITCHING TIME

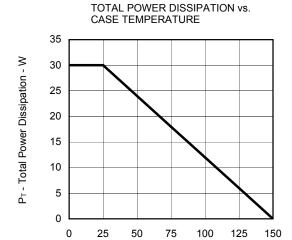


### **TEST CIRCUIT 3 GATE CHARGE**



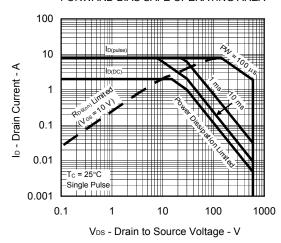
### TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

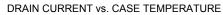




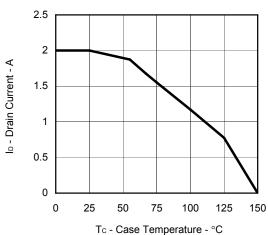


Tch - Channel Temperature - °C

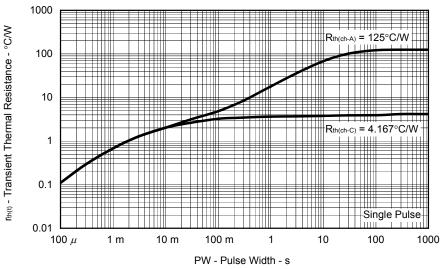




 $\mbox{Tc}$  - Case Temperature -  $^{\circ}\mbox{C}$ 

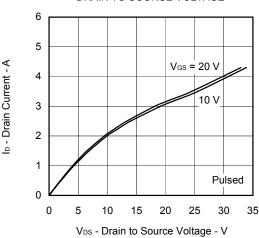


#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

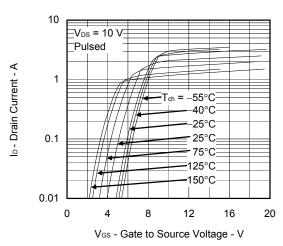


Data Sheet D18785EJ2V0DS

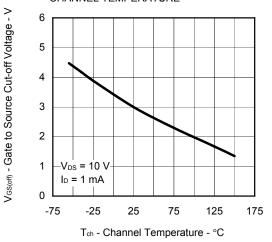
# DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



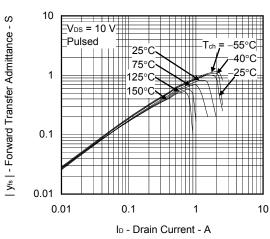
### FORWARD TRANSFER CHARACTERISTICS



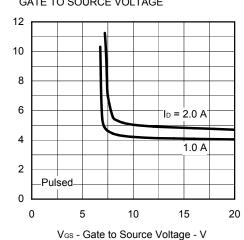
# GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



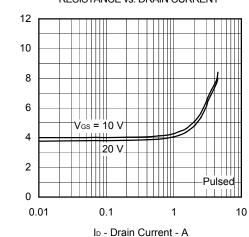
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



# DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



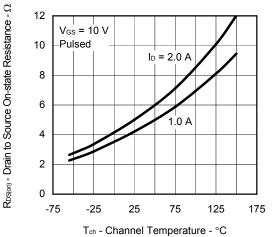
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



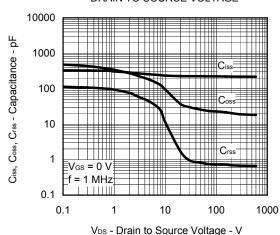
 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$  - Drain to Source On-state Resistance -  $\Omega$ 

 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$  - Drain to Source On-state Resistance -  $\Omega$ 

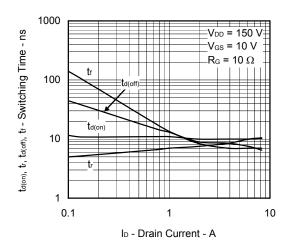
# DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



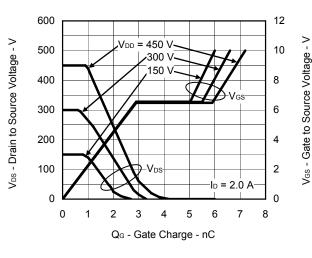
# CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



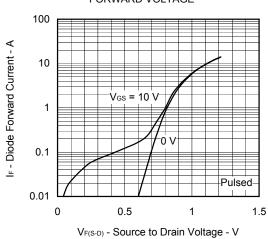
#### SWITCHING CHARACTERISTICS



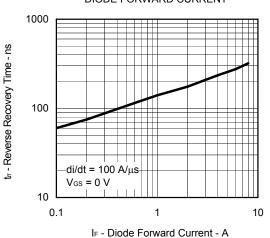
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



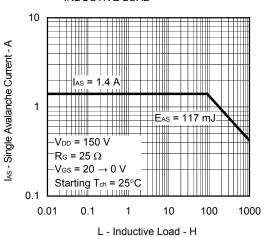
# SOURCE TO DRAIN DIODE FORWARD VOLTAGE



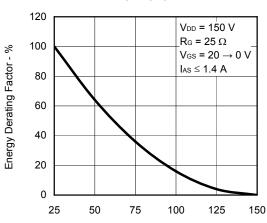
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



# SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

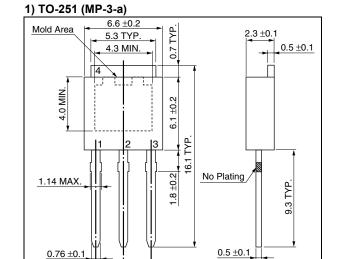


# SINGLE AVALANCHE ENERGY DERATING FACTOR



Starting T<sub>ch</sub> - Starting Channel Temperature -  $^{\circ}$ C

### <R> PACKAGE DRAWINGS (Unit: mm)



2.3 TYP.

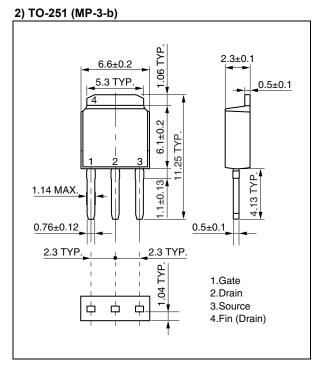
TYP

1.02

1. Gate

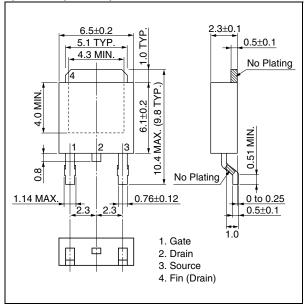
2. Drain

3. Source4. Fin (Drain)

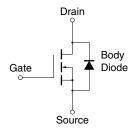


#### 3) TO-252 (MP-3ZK)

2.3 TYP



### **EQUIVALENT CIRCUIT**



**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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