# Design Guidelines for the Low-Noise
Low-Dropout Regulator—Si9181

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INTRODUCTION

This application note discusses the operation and features of the Si9181, a 350-mA CMOS low-dropout (LDO), low-noise voltage regulator. Providing very low ground current to extend battery life, the Si9181 also offers superior line/load transient response and ripple rejection. Designed to maintain regulation while delivering currents from 0 mA to 600 mA, the Si9181 regulator also features an "out of regulation" error flag signal and ON/OFF control input for complete shutdown.

The Si9181 was designed for applications requiring a regulated voltage equal to or less than the voltage of the source or battery, and requiring very low output noise. Such applications include digital signal processors, baseband circuits, mixers, A-to-D converters, or intermediate amplifiers. The Si9181's LDO characteristics are determined by its voltage, ground current, power-dissipation, peak current capability, noise and ripple rejection specifications. The Si9181 is designed to meet the criteria for high quality on each of these determinants, and is suitable for portable and noise–sensitive appliances such as cellular phones.
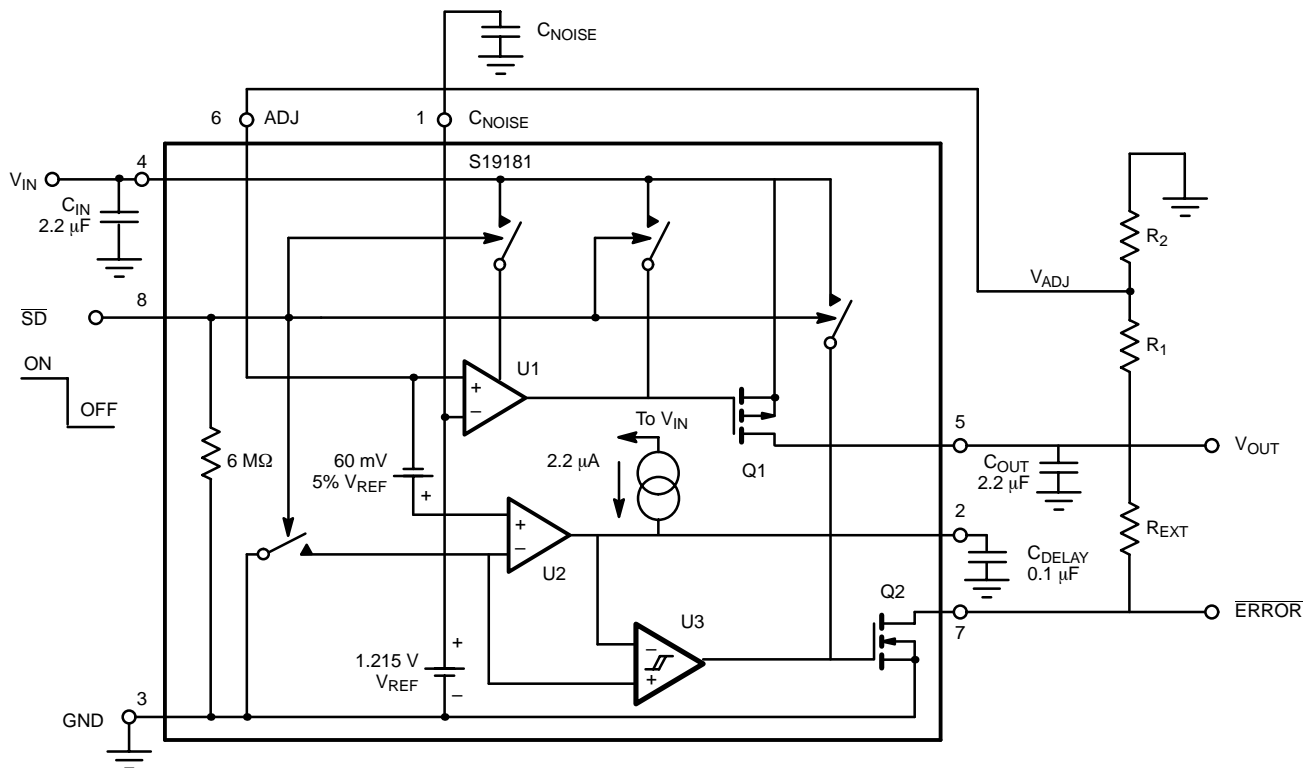
FIGURE 1. 350-mA CMOS LDO Regulator (Adjustable Output)

LDO OPERATION

Choosing the right series pass element for the regulator is key to achieving low dropout voltages and high efficiency. LDO regulators are functionally no different than variable resistance series elements, where the voltage drop across the pass element is equal to the input-to-output voltage differential. The variable resistor can either be a bipolar transistor, controlled by the base current, or a MOS transistor, which is controlled by gate voltage. In bipolar transistors the collector current is controlled by the base current, a process that contributes to a higher ground current, diminishing the efficiency of the regulator.

For CMOS LDOs the series pass element operates in two different regions depending upon the input voltage. If the input voltage is significantly higher than output voltage, the power MOSFET operates in the saturation region and acts as a controllable current source. This drain current is a function of the transconductance of the power MOSFET, $Gm = \dfrac{dI_D}{dV_{GS}}$, where the gate voltage is set by the error amplifier. If the input voltage decreases to $(V_{OUT} + (R_{ON} * I_{OUT}))$, the voltage regulator cannot maintain a regulated output. If the input voltage falls below this voltage, the p-channel power MOSFET enters the linear region. In this linear region, the gate voltage changes with the input voltage, and is not a function of the output or control voltage. All the circuits in the Si9181 are designed to operate with inputs as low as 2 V and, on adjustable Si9181 regulators, outputs can be programmed as low as 1.5 V.

I–V CHARACTERISTIC OF SI9181

The Si9181 uses a p-channel power MOSFET series element that significantly reduces ground current. The Si9181 also facilitates higher peak current capabilities than solutions using bipolar series elements, where the maximum current drawn is limited by the base current. Because the Si9181 uses a p-channel power MOSFET series element, the gate voltage controls the drain current.

The maximum gate-to-source voltage (V_{GS}) is the same as the input voltage at any load or input to output voltage differential. For regulator operation, the gate-to-source voltage should be high enough to operate the p-channel MOSFET in the saturation region. The available drain current is proportional to the square of the difference between the applied gate voltage and transistor threshold voltage. The Si9181 gate threshold is 0.8 V and needs minimum V_{GS} equal to 1.8 V to produce the 600-mA peak current. The 600-mA peak current can be drawn for at least 2 ms. The package can handle the power dissipated during the peak current pulse period. The power han-

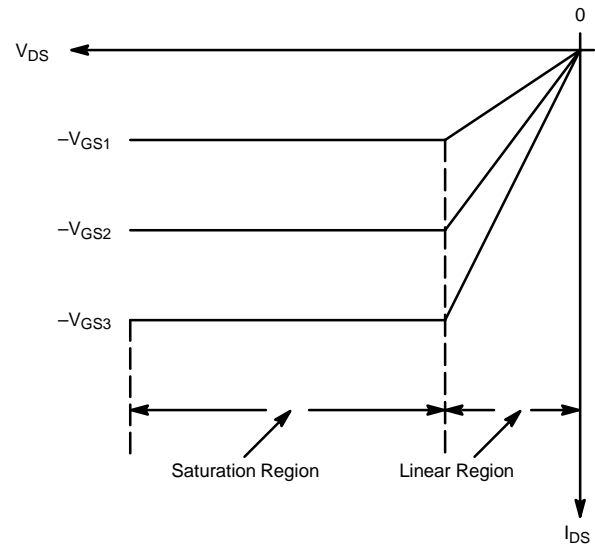dling capability of Si9181 is enhanced by the low junction-to-lead thermal resistance.

FIGURE 2. I-V Characteristic of P-Channel MOSFET

POWER DISSIPATION/JUNCTION TEMPERATURE

The Si9181 is rated to deliver up to 600-mA peak current for 2 ms. The maximum load current is specified for continuous operation and for finite pulse widths. Maximum allowable junction temperature, junction-to-ambient thermal impedance at a thermal equilibrium, and the ambient temperature determine the continuous current rating at a given input-to-output differential. The input voltage, p-channel power MOSFET transconductance, and the transient thermal impedance between junction to lead are major issues for the peak current amplitude and the pulse width. The maximum continuous power dissipation allows for a safe junction temperature and is calculated using the following equation:

$$P_D = \left(V_{IN} - V_{OUT}\right)I_{OUT} + V_{IN} \times I_{GND} \qquad (1)$$

$$\text{Efficiency} = \frac{V_{OUT} \times I_{OUT}}{V_{IN}\left(I_{OUT} + I_{GND}\right)} \qquad (2)$$

$$P_{DMAX} = \frac{\left(150 - T_A\right)}{\theta_{JA}} \qquad (3)$$

Where, $\theta_{JA} = 120°$C/W (All leads soldered to PC board on 1-oz copper)

PROTECTION FEATURES

Short circuit

In the event of a short circuit in the equipment powered by an LDO, the Si9181 limits the maximum current to prevent damage to the electronics. The peak current through the Si9181 is typically limited to 800 mA during a continuous short circuit at the output.

Over-Temperature

The Si9181 is designed with an over temperature protection circuit to prevent thermal runaway in the p-channel power MOSFET. If the temperature reaches 165°C, the internal control circuit shuts off the p-channel power MOSFET. The LDO will remain disabled until the chip temperature drops below 145°C, and will re-engage automatically. The 20°C temperature difference avoids possible oscillation and reduces the average power delivery during fault conditions to reduce the risk of damage.

LOOP COMPENSATION

For the stable operation of a closed loop electronic system, such as a voltage regulator, the feedback loop needs to be compensated to keep the total phase lag at less than 360° for a signal having the total gain more than or equal to unity. The phase lag includes the 180° phase change caused by the negative feedback.

The Si9181 equivalent circuit and its gain characteristic with internal compensation is shown in Figure 3. The closed loop has two low frequency poles. A low frequency pole (P_O) is a result of output capacitance C_{OUT} and the channel length modulation parameter λ of the P-MOS. The location of this pole changes with the load current, I_O.
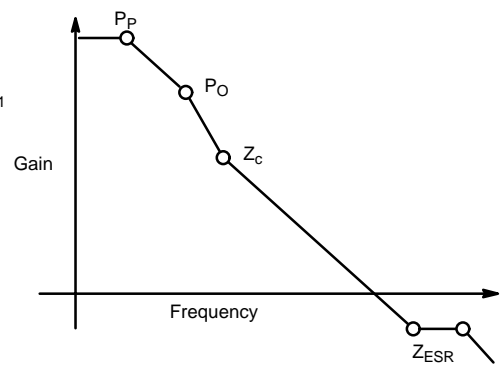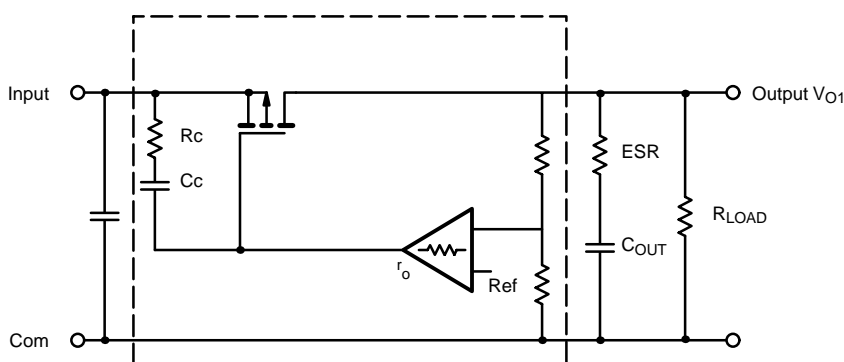
$$P_O = \frac{\lambda I_O}{2\pi \ C_{OUT}} \tag{4}$$

The second pole is introduced by the compensation capacitance Cc, parasitic capacitance of the series pass element and the error amplifier. The error amplifier output impedance r_o and the compensation capacitor along with the gate capacitance of PMOS determine the location of the second pole P_p. The gate capacitance is low enough to be neglected here.

$$P_p = \frac{1}{2\pi \ r_O \ C_c} \tag{5}$$

The Si9181 uses an internal zero to achieve a stable feedback loop, eliminating the need to rely on the ESR value of the output capacitors for a zero. The location of internal zero Z_c is changed to offset any effect of the load on the low frequency pole P_O. This internal zero also offers the freedom to use a low–ESR ceramic X5R or Y5V capacitor for lower noise.

$$Z_{ESR} = \frac{1}{2\pi \times C_O \times ESR} \tag{6}$$

With the native compensation of the Si9181, a closed–loop bandwidth as high as 100 kHz can be achieved easily with a phase margin no lower than 60°. (See Figure 4.)
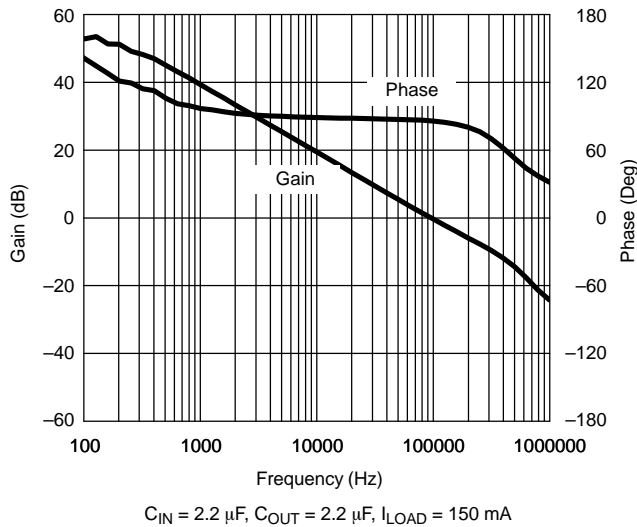

FIGURE 3. Loop Compensation

$C_{IN} = 2.2 \mu F$, $C_{OUT} = 2.2 \mu F$, $I_{LOAD} = 150$ mA

FIGURE 4. Closed Loop Bandwidth

CH1 – V_{OUT} (Pin 5)
CH2 – $\overline{Error}$ (Pin 7)
CH3 – V_{IN} (Pin 4)
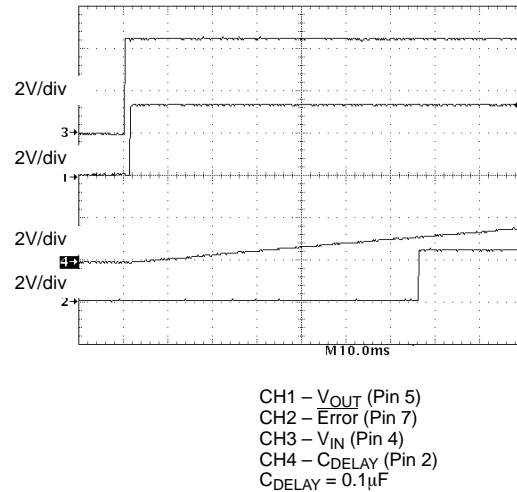CH4 – C_{DELAY} (Pin 2)
$C_{DELAY} = 0.1 \mu F$

FIGURE 5. Programmed Delay for Error
Signal

ERROR SIGNAL WITH PROGRAMMABLE DELAY

The Si9181 is provided with an $\overline{ERROR}$ pin which can be used as a high-going enable or power-good signal to activate the electronic equipment once the output is within 5% of the set value. When output voltage drops below 95% of its set level, the $\overline{ERROR}$ pin can positively disable the electronics before the low-going supply cripples the circuit. The $\overline{ERROR}$ signal required to wake up the electronics can also be delayed with respect to the output by adding a small capacitor at C_{DELAY} (pin 2). The $\overline{ERROR}$ output is a high slew–rate open drain and needs an external pull-up resistor.

The C_{DELAY} capacitor is fully discharged through U2 when the circuit is OFF or when the output is below the set power-good threshold (0.95 V_{OUT}). (See Figure 1.) Once the output goes above the power-good trip threshold, the U2 output switches to a high impedance state and C_{DELAY} charges with a 2.2-μA (typ) constant current. U3 switches Q2 off at 1.215 V across the C_{DELAY} capacitor and the $\overline{ERROR}$ output is pulled high by R_{EXT} (Figure 5).

$$C_{DELAY} = 1.81 \times 10^{-6} t_{DELAY} \qquad (7)$$

SHUTDOWN

The Si9181 is provided with an ON/OFF control pin (named $\overline{SD}$) that opens and closes the internal power MOSFET switch and controls the total current drawn by the entire circuit. The current is less than 1 μA, reducing the drain on the battery in standby mode and increasing standby time. While a low at the $\overline{SD}$ pin opens the switch, a high at the $\overline{SD}$ pin enables the regu-

lator operation. This allows the Si9181 to be used as a high-current simple disconnect switch that works in conjunction with the regulated output. It is recommended that the user connect the $\overline{SD}$ to the input V_{IN} when not in use.

INPUT/OUTPUT CAPACITOR SELECTION

The circuit stability and output voltage during line and load step changes dominate the selection criteria of input and output capacitors. A higher step load current at the output demands higher capacitance with a lower ESR value at the output. An input bypass capacitor is required in applications involving long traces between the source and LDO. The input capacitor should be at least equal to or greater than the output capacitor for proper operation. A 2.2-μF to 10-μF ceramic capacitor with a Y5V dielectric is recommended, and an X5R dielectric is recommended for better temperature characteristics. The Si9181 requires only a small output capacitor because of the high closed loop bandwidth of 100 kHz or more. Also, the freedom to use a very low–ESR ceramic capacitor reduces the form factor further for greater performance.

$$\Delta V = \frac{I_{STEP} \times t_{RESPONSE}}{C_{OUT}} + I_{STEP} \times ESR \qquad (8)$$

where:

I_{STEP} = Output load step (A)
ESR = ESR of Output capacitor (W)
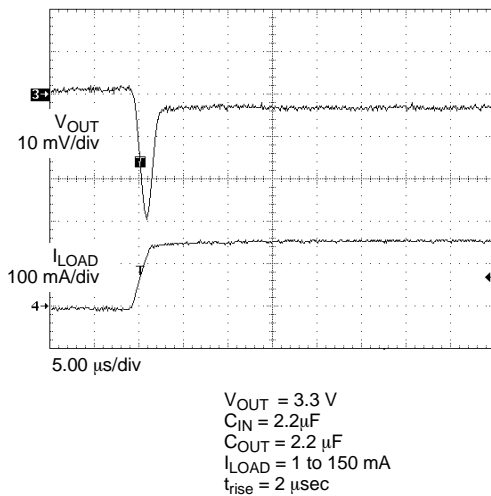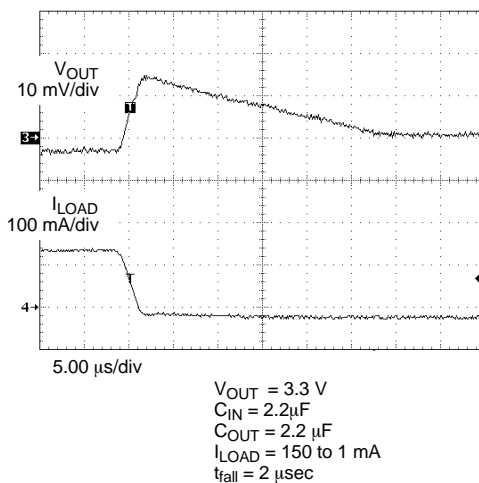$t_{RESPONSE}$ = Response time of the regulator (s)
$t_{RESPONSE}$ depends on the unity gain bandwidth and the phase margin of the closed loop.

DYNAMIC LOAD RESPONSE

The ability to use a low ESR ceramic capacitor at the output of the Si9181 helps reduce the glitch during the high slew-rate step load, while the high closed loop bandwidth reduces the re-covery time. With a 2.2-μF ceramic capacitor at the output, the maximum deviation observed in the output is 30 mV, with bet-ter than 3-μS recovery time. Refer to the Figures 5 and 6. The recovery time of the output from overshoot during the load re-moval is the time required to discharge the output capacitor. The recovery time depends on the voltage overshoot, capaci-tor and the load current.

V_{OUT}
10 mV/div

I_{LOAD}
100 mA/div

5.00 μs/div

V_{OUT} = 3.3 V
C_{IN} = 2.2μF
C_{OUT} = 2.2 μF
I_{LOAD} = 1 to 150 mA
t_{rise} = 2 μsec

Figure 5. Load Transient Response-1

V_{OUT}
10 mV/div

I_{LOAD}
100 mA/div

5.00 μs/div

V_{OUT} = 3.3 V
C_{IN} = 2.2μF
C_{OUT} = 2.2 μF
I_{LOAD} = 150 to 1 mA
t_{fall} = 2 μsec

Figure 6. Load Transient Response-2

PCB LAYOUT

The component placement around the LDO should be done carefully to achieve good dynamic line and load response. The input and noise capacitor should be kept close to the LDO. The rise in junction temperature depends on how efficiently the heat is carried away from the junction to ambient. The junction to lead thermal impedance is a characteristic of the package and is fixed. The thermal impedance between lead to ambient can be reduced by increasing the copper area on PCB. In-crease the input, output and ground trace area to reduce the junction-to-ambient thermal impedance.