DATA SHEET

CX77144: Power Amplifier Module for CDMA (887–925 MHz)

Applications

- CDMA for Japan
- Wireless Local Loop (WLL)

Features

- Low voltage positive bias supply
  - 3.2 V to 4.2 V
- Low V_{REF}
  - 2.85 V, nominal
- Good linearity
- High efficiency
- Large dynamic range
- 10-pin package
  - 4 mm x 4 mm x 1.5 mm
- Power down control
- Low power–state control
- InGaP
- CDMA2000 / IS95

Description

The CX77144 Power Amplifier Module (PAM) is a fully matched, 10-pin surface mount module developed for cellular handset applications utilizing Code Division Multiple Access (CDMA) and Wireless Local Loop (WLL). This small and efficient power amplifier module packs a full 887–925 MHz bandwidth coverage into a single compact package. The device meets the stringent IS95 requirements up 27.5 dBm output power and up to 27 dBm for CDMA2000. A low current digital pin (VCONT) provides improved efficiency for the low RF power range of operation.

The single Gallium Arsenide (GaAs) Microwave Monolithic Integrated Circuit (MMIC) contains all active circuitry in the module. The MMIC contains on-board bias circuitry, as well as input and interstage matching circuits. The output match is realized off-chip and within the module package to optimize efficiency and power performance into a 50 Ω load. This device is manufactured with Skyworks' GaAs Heterojunction Bipolar Transistor (HBT) process that provides for all positive voltage DC supply operation while maintaining high efficiency and good linearity. Primary bias to the CX77144 is supplied directly from a three-cell Ni-Cd, a single-cell Li-Ion, or other suitable battery with an output in the range of 3.2 to 4.2 volts. Power down is accomplished by setting the voltage on the low current reference pin to zero volts. No external supply side switch is needed as typical "off" leakage is a few microamperes with full primary voltage supplied from the battery.

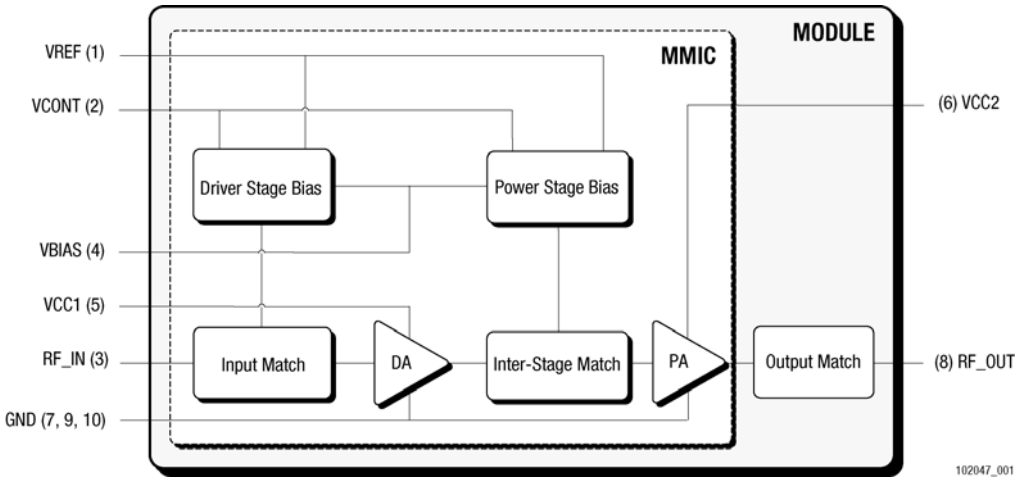


Figure 1. Functional Block Diagram

Electrical Specifications

The following tables list the electrical characteristics of the CX77144 Power Amplifier. Table 1 shows the absolute maximum ratings and Table 2 lists the recommended operating conditions for achieving the electrical performance listed in Table 4. Table 5 shows the specifications for recommended operating conditions. Table 3 lists the settings for the power ranges.

Table 1. Absolute Maximum Ratings (1)

Characteristic	Symbol	Minimum	Nominal	Maximum	Unit
RF Input Power	P_{IN}	—	0.0	7.0	dBm
Supply Voltage	V_{CC}	—	3.5	6.0	Volts
Reference Voltage	V_{REF}	—	2.85	3.1	Volts
Case Operating Temperature (2)	T_C	–30	+25	+85	°C
Case Storage Temperature	T_{STG}	–55	—	+125	°C

(1) No damage assuming only one parameter is set at limit at a time with all other parameters set at nominal value.

(2) Case Operating Temperature refers to the temperature of the GROUND PAD at the underside of the package.

Table 2. Recommended Operating Conditions

Characteristic		Symbol	Minimum	Nominal	Maximum	Unit
Supply Voltage		V_{CC1}	1.4	3.5	4.2	Volts
		V_{CC2}	1.4	3.5	4.2	
		V_{BIAS}	3.2	3.5	4.2	
Reference Voltage	PA ON	V_{REF}	2.75	2.85	2.95	Volts
	PA OFF	V_{REF}	—	—	< 0.5	
Mode Input Impedance > 2.5 kΩ	High Bias Mode	V_{CONT}	0.0	—	0.5	Volts
	Low Bias Mode	V_{CONT}	2.5	—	3.0	
Operating Frequency		F_O	887	906	925	MHz
Case Operating Temperature (1)		T_C	–30	—	+85	°C

(1) Case Operating Temperature refers to the temperature of the GROUND PAD at the underside of the package.

Table 3. Power Range Truth Table

Power Setting	V_{REF}	V_{CONT}	Output Power
High Power	2.85 V	0.0 V–0.5 V	18 dBm to 27 dBm
Low Power	2.85 V	2.5 V–3.0 V	≤ 18 dBm
Shut Down	0.0 V	0.0 V	—

Table 4. Electrical Specifications for CDMA Nominal Operating Conditions (1)

Characteristics		Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain conditions Digital Mode		G_{LOW} (2)	$V_{CONT} \geq 2.5$ V $P_O = 18$ dBm	22.0	24.0	26.0	dB
		G_{HIGH}	$V_{CONT} \leq 0.5$ V $P_O = 27$ dBm	26.5	27.5	29.0	
Power Added Efficiency		PAE_{LOW} (2)	$V_{CONT} \geq 2.5$ V $P_O = 18$ dBm	26.0	30.0	—	%
		PAE_{HIGH}	$V_{CONT} \leq 0.5$ V $P_O = 27$ dBm	37.0	40.0	—	
Total Supply current		I_{CC_LOW} (2)	$P_O = 18$ dBm	—	150	175	mA
		I_{CC_HIGH}	$P_O = 27$ dBm	—	355	390	
Quiescent current		I_{Q_LOW} (2)	$V_{CONT} \geq 2.5$ V	50	60	70	mA
		I_{Q_HIGH}	$V_{CONT} \leq 0.5$ V	65	80	95	
Reference Current		I_{REF}	—	—	2.5	5.0	mA
Control Current		I_{CONT}	$V_{CONT} = 2.5$ V	—	0.315	0.5	mA
Total Supply current in Power-down Mode		I_{PD}	$V_{REF} = 0$ V $V_{CONT} = 0$ V	—	2.0	5.0	µA
Adjacent Channel Power (3)(4)	885 kHz offset	$ACP1_{LOW}$ (2)	$V_{CONT} \geq 2.5$ V $P_O \leq 18$ dBm	—	–50.0	–47.7	dBc
		$ACP1_{HIGH}$	$V_{CONT} \leq 0.5$ V $P_O \leq 27$ dBm	—	–50.0	–47.0	
	1.98 MHz offset	$ACP2_{LOW}$ (2)	$V_{CONT} \geq 2.5$ V $P_O \leq 18$ dBm	—	–62.0	–58.5	
		$ACP2_{HIGH}$	$V_{CONT} \leq 0.5$ V $P_O \leq 27$ dBm	—	–60.0	–58.5	
Harmonic Suppression	Second	Fo2	$P_O \leq 27$ dBm	—	—	–35.0	dBc
	Third	Fo3	$P_O \leq 27$ dBm	—	—	–40.0	
Noise Power in RX Band 832-870 MHz		RxBN	$P_O \leq 27$ dBm	—	–138	–137	dBm/Hz
Noise Figure		NF	—	—	4.5	5.0	dB
Input Voltage Standing Wave Ratio		VSWR	—	—	1.5:1	2.0:1	—
Stability (Spurious output)		S	5:1 VSWR All phases	—	—	–60.0	dBc
Ruggedness – No damage (5)		Ru	$P_O \leq 27$ dBm	10:1	—	—	VSWR

(1) $V_{CC1} = +3.5$ V, $V_{BIAS} = +3.5$ V, $V_{REF} = +2.85$ V, Freq = 906 MHz, $T_C = +25$ °C, unless otherwise specified.

(2) For low power mode, V_{CC1} and $V_{CC2} = 1.4$ V

(3) ACP is specified per CDMA2000 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

(4) CDMA2000 is configured as DCCH = 9600, SCHO = 9600, PCH (Walsh 0) = –3.75 dB, and Peak-to-Average Ratio (CCDF = 1%) = 4.5 dB. For IS95, $P_O = 27.5$ dBm is acceptable to meet the specified ACPR values.

(5) All phases, time = 10 seconds.

Table 5. Electrical Specifications for CDMA Recommended Operating Conditions [1]

Characteristics		Symbol	Condition	Min.	Max.	Unit
Gain conditions Digital Mode		G_{LOW} [2]	$V_{CONT} \geq 2.5$ V $P_O = 18$ dBm	20.8	27.5	dB
		G_{HIGH}	$V_{CONT} \leq 0.5$ V $P_O = 27$ dBm	25.4	30.7	
Reference Current		I_{REF}	—	—	5.0	mA
Control Current		I_{CONT}	$V_{CONT} = 2.5$ V	—	0.5	mA
Total Supply current in Power-down Mode		I_{PD}	$V_{REF} = 0$ V $V_{CONT} = 0$ V	—	5.0	µA
Adjacent Channel Power [3][4]	885 kHz offset	$ACP1_{LOW}$ [2]	$V_{CONT} \geq 2.5$ V $P_O \leq 18$ dBm	—	–44.0	dBc
		$ACP1_{HIGH}$	$V_{CONT} \leq 0.5$ V $P_O \leq 27$ dBm	—	–44.0	
	1.98 MHz offset	$ACP2_{LOW}$ [2]	$V_{CONT} \geq 2.5$ V $P_O \leq 18$ dBm	—	–56.0	
		$ACP2_{HIGH}$	$V_{CONT} \leq 0.5$ V $P_O \leq 27$ dBm	—	–56.0	
Harmonic Suppression	Second	F_O2	$P_O \leq 27$ dBm	—	–35.0	dBc
	Third	F_O3	$P_O \leq 27$ dBm	—	–40.0	
Noise Power in RX Band 832-870 MHz		RxBN	$P_O \leq 27$ dBm	—	–136	dBm/Hz
Noise Figure		NF	—	—	6.0	dB
Input Voltage Standing Wave Ratio		VSWR	—	—	2.0:1	—
Stability (Spurious output)		S	5:1 VSWR All phases	—	–60.0	dBc
Ruggedness – No damage [5]		Ru	$P_O \leq 27$ dBm	10:1	—	VSWR

[1] Per Table 2, unless otherwise specified.

[2] For low power mode, V_{CC1} and $V_{CC2} = 1.4$ V

[3] ACP is specified per CDMA2000 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

[4] CDMA2000 is configured as DCCH = 9600, SCHO = 9600, PCH (Walsh 0) = –3.75 dB, and Peak-to-Average Ratio (CCDF = 1%) = 4.5 dB. For IS95, $P_O = 27.5$ dBm is acceptable to meet the specified ACPR values.

[5] All phases, time = 10 seconds.

Characterization Data

The charts in Figure 2 through Figure 6 illustrate the characteristics of a typical CX77144 power amplifier designed for operation in the CDMA frequency band (887–925 MHz). Shown are power sweep characteristics for key performance parameters over temperature and frequency, up to 27 dBm output power.

Each chart shows two sets of data to illustrate the characteristics in Low Mode and High Mode. This amplifier was selected by characterizing a group of devices and choosing a part with average electrical performance for both nominal and the full range of recommended operating conditions, including worst case limits.

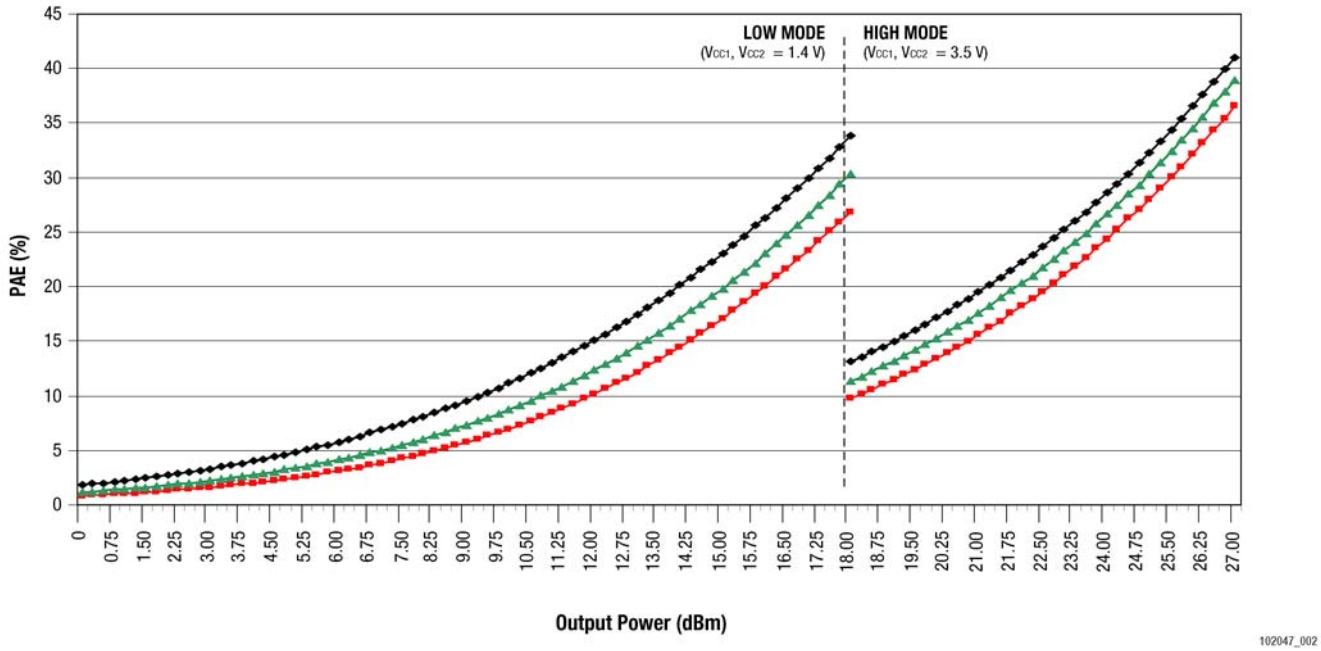


Figure 2. PAE vs. Output Power

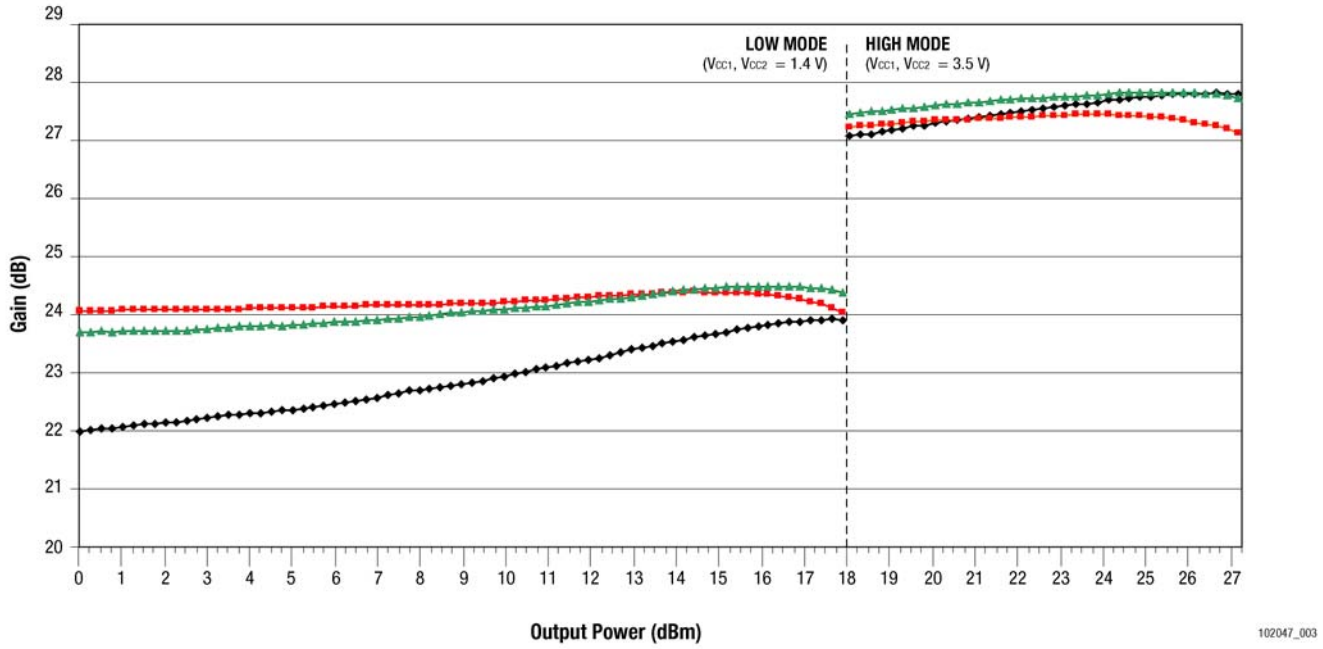


Figure 3. Gain vs. Output Power

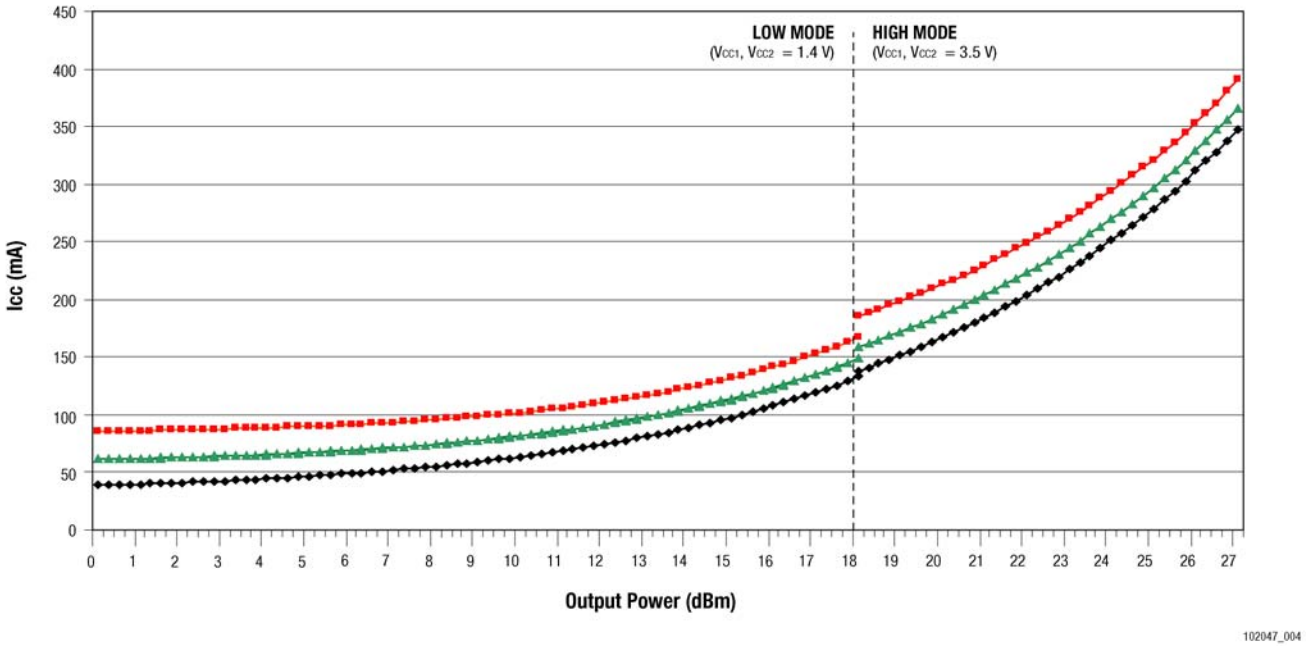


Figure 4. Total Supply Current vs. Output Power

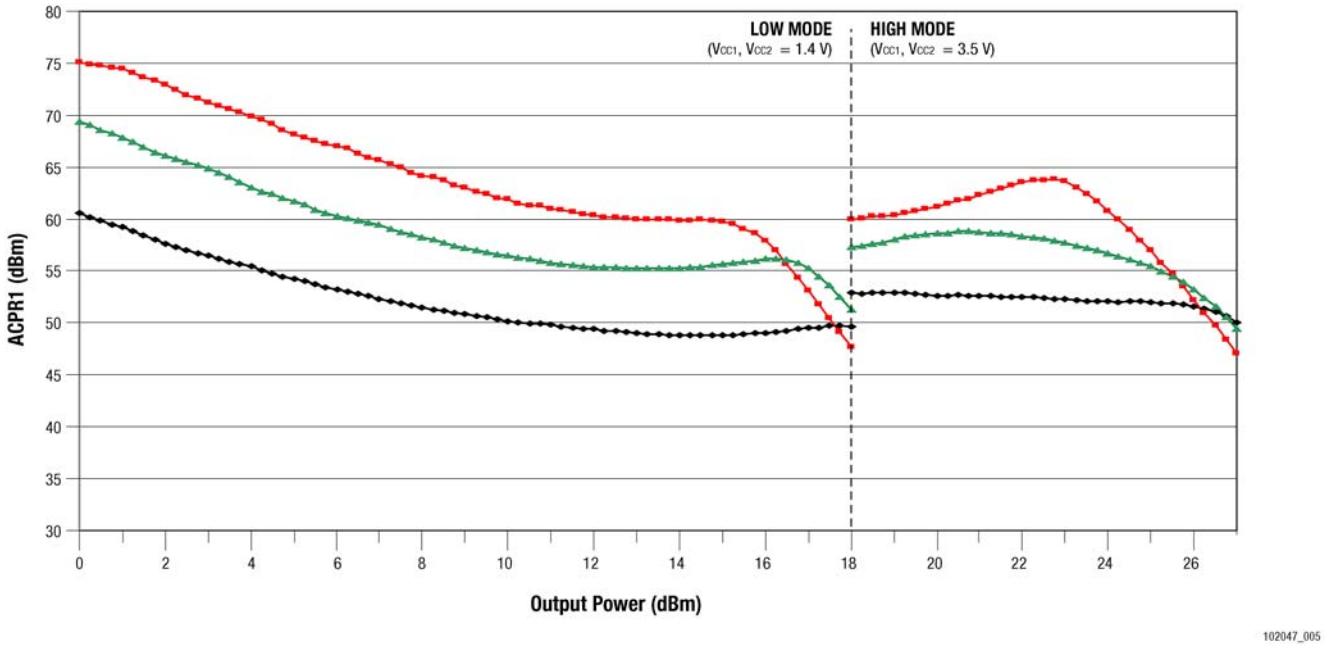


Figure 5. ACPR1 vs. Output Power

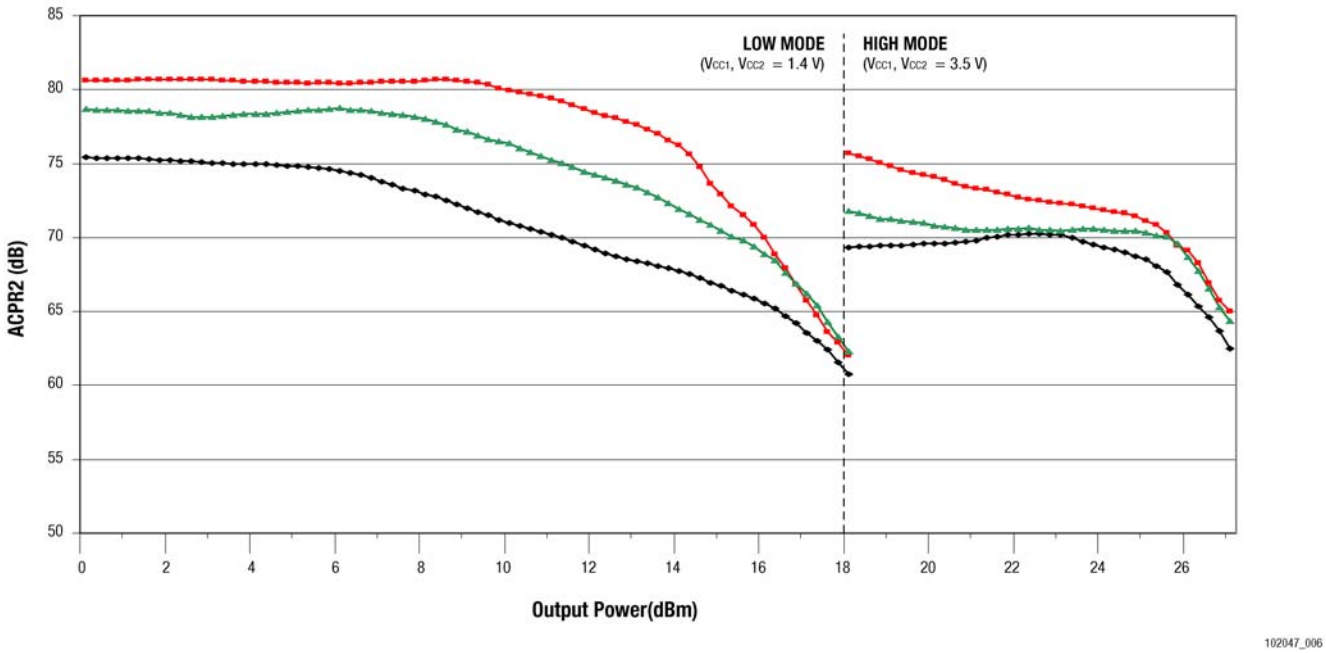


Figure 6. ACPR2 vs. Output Power

Evaluation Board Description

The evaluation board is a platform for testing and interfacing design circuitry. To accommodate the interface testing of the CX77144, the evaluation board schematic and diagrams are included for preliminary analysis and design. Figure 7 shows the basic schematic of the board for the 887 MHz to 925 MHz range and Figure 8 is the assembly diagram.

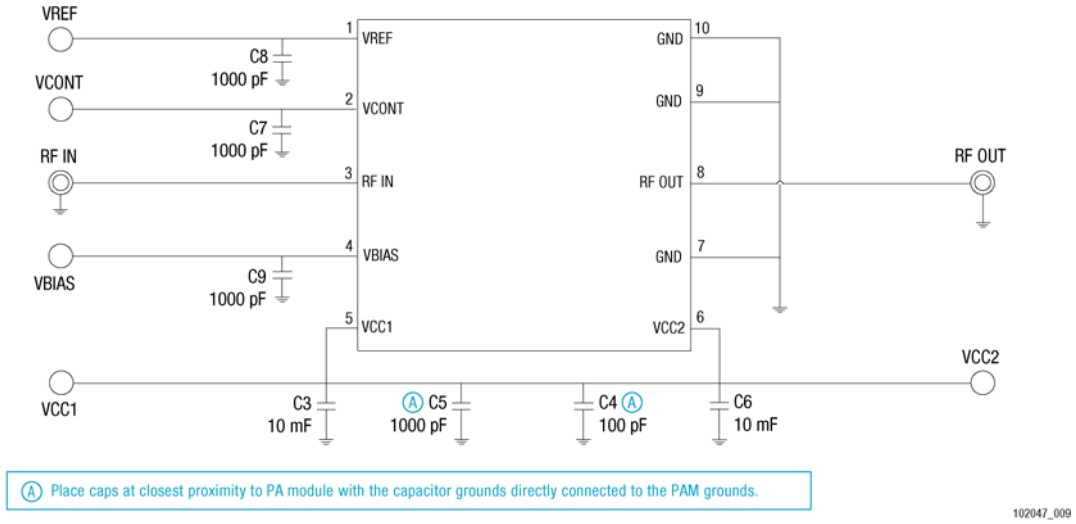


Figure 7. Evaluation Board Schematic

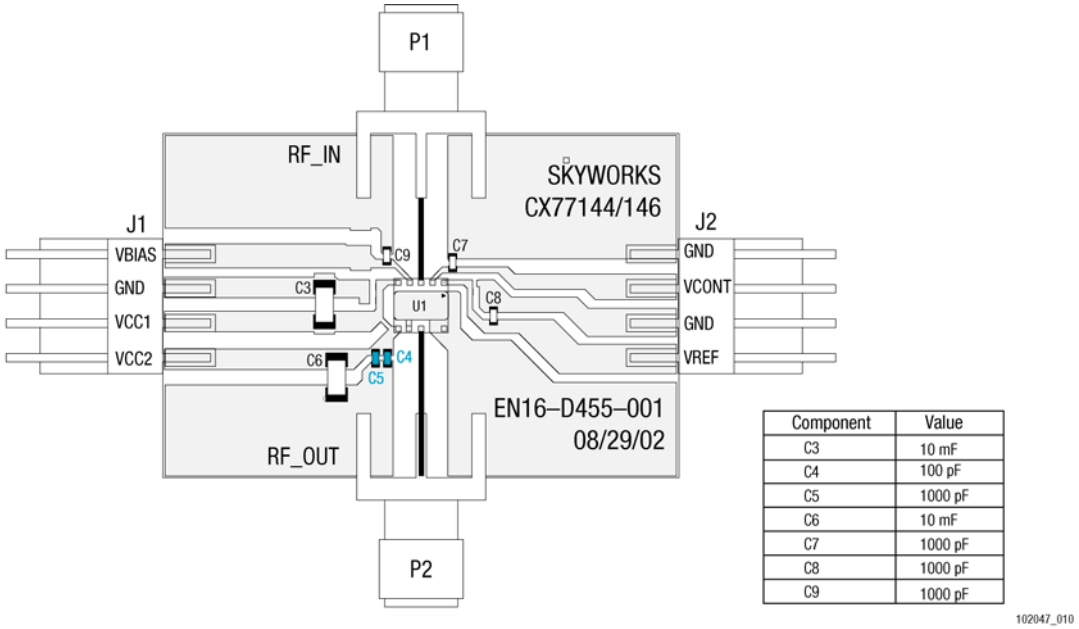
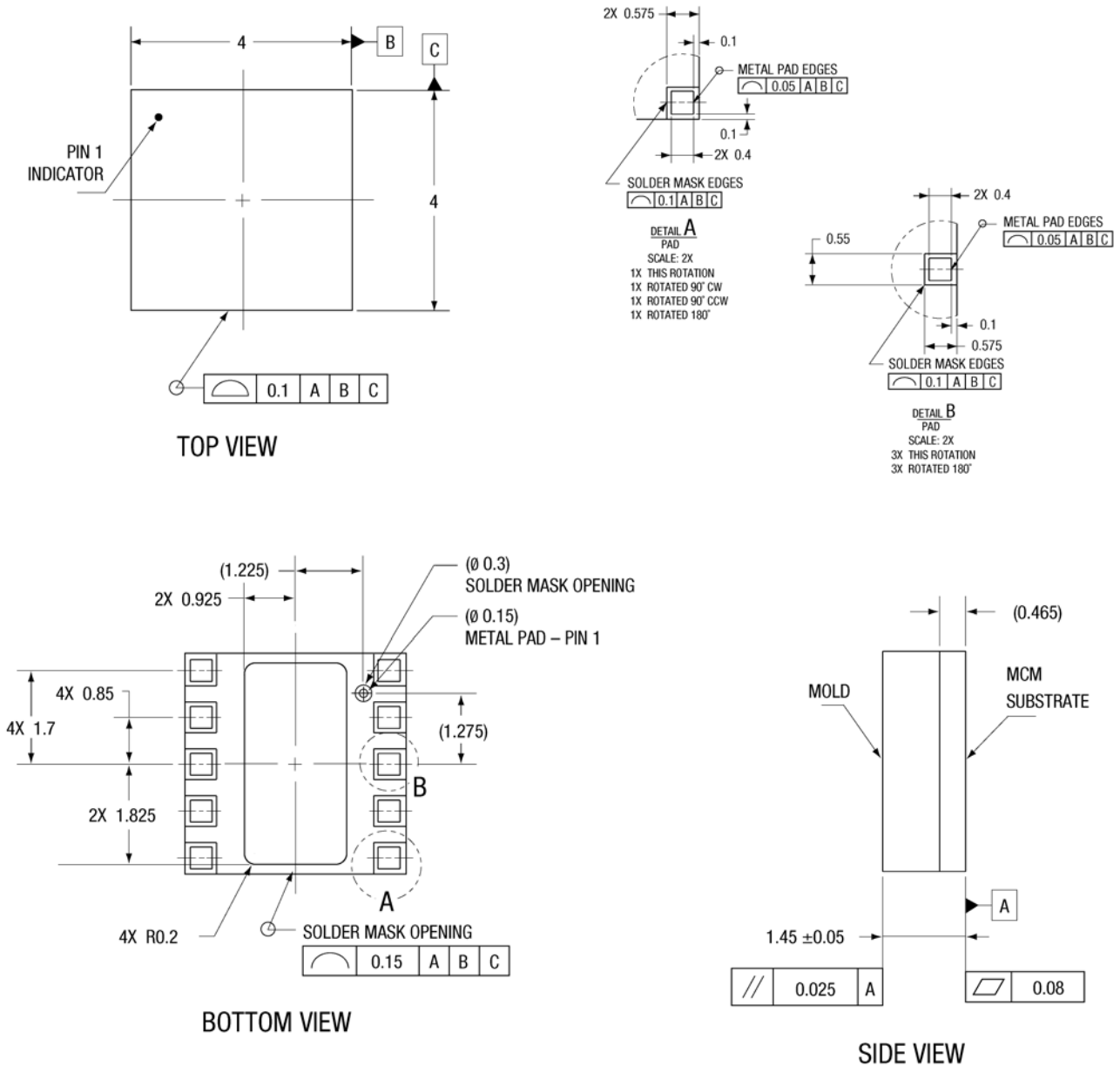


Figure 8. Evaluation Board Assembly Diagram

Package Dimensions and Pin Descriptions

The CX77144 is a multi-layer laminate base, overmold encapsulated modular package designed for surface mount solder attachment to a printed circuit board. Figure 9 is a mechanical drawing of the pad layout for this package. Figure 10 shows the pin names and the pin numbering convention, which starts with pin 1 in the upper left and increments counter-clockwise around the package. Figure 11 illustrates typical case markings.



NOTES: unless otherwise specified
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING IN ACCORDANCE WITH ASME Y14.5M–1994.
3. SEE APPLICABLE BONDING DIAGRAM AND DEVICE ASSEMBLY DRAWING FOR DIE AND COMPONENT PLACEMENT.
4. PADS ARE METAL DEFINED; THE CENTER PAD IS SOLDER MASK DEFINED.

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Figure 9. CX77144 Package Dimensional Drawing – All Views

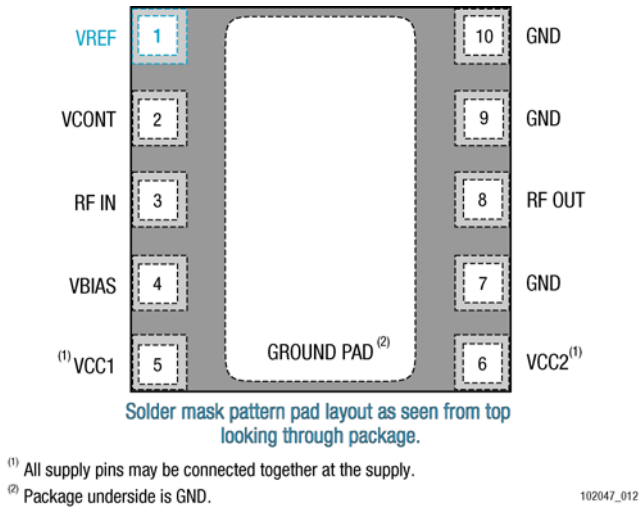

Figure 10. Pin Names and Configuration (Top View)

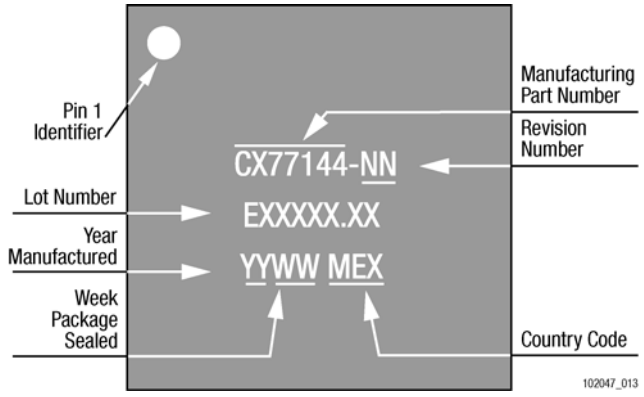

Figure 11. Typical Case Markings

Package and Handling Information

Because of its sensitivity for moisture absorption, this device package is baked and vacuum-packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The CX77144 is capable of withstanding an MSL3/250 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second; maximum temperature should not exceed 250 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 250 °C for more than 10 seconds. For details on both attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to *Skyworks' Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752*. Additional information on standard SMT reflow profiles can also be found in the *JEDEC Standard J-STD–020*.

Production quantities of this product are shipped in the standard tape-and-reel format. For packaging details, refer to Skyworks' *Application Note: Tape and Reel, Document Number 101568*.

Electrostatic Discharge Sensitivity

The CX77144 is a Class I device. Electrostatic Discharge (ESD) immunity levels for each pin of the CX77144 product are shown in Figure 12, using the Human Body Model, and in Figure 13, using the Machine Model.

Various failure criteria can be utilized when performing ESD testing. Many vendors employ relaxed ESD failure standards, which fail devices only after "the pin fails the electrical specification limits" or "the pin becomes completely non-functional". Skyworks employs most stringent criteria, fails devices as soon as the pin begins to show any degradation on a curve tracer.

If ESD damage threshold magnitude is found to consistently exceed 2000 volts on a given pin, this so is indicated. If ESD damage threshold below 2000 volts is measured for either polarity, numbers are indicated that represent the worst case values observed in product characterization.

Human Body Model (HBM)

The numbers in Figure 12 specify the ESD threshold level for each pin where the I-V curve between the pin and ground starts to show degradation. ESD testing was performed in compliance with MIL-STD-883E Method 3015.7 using the Human Body Model (HBM).

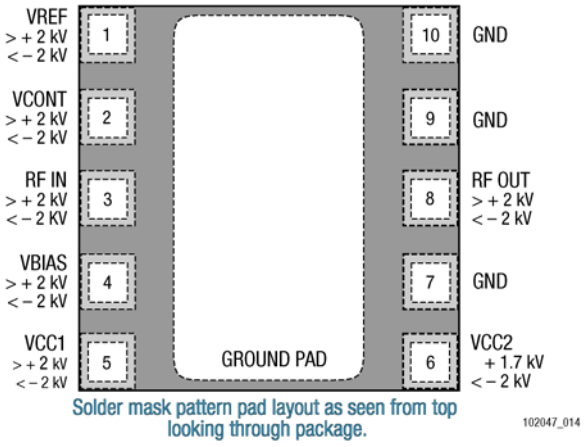

Figure 12. ESD Sensitivity Areas – Human Body Model (Top View)

Machine Model (MM)

The numbers in Figure 13 specify the ESD threshold level for each pin where the I-V curve between the pin and ground starts to show degradation. ESD testing was performed in compliance with JESD22-A115B using the Machine Model (MM) and has met the classification criteria for Class B

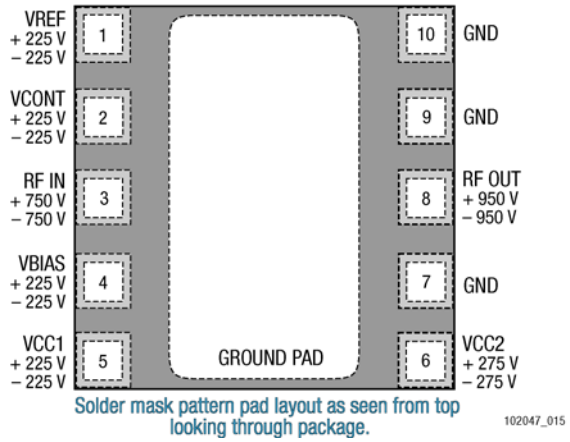

Figure 13. ESD Sensitivity Areas – Machine Model (Top View)

To avoid ESD damage, both latent and visible, it is very important that the product assembly and test areas observe the Class-1 ESD practices for handling GaAs IC-based products to avoid induced damage.

- Personnel Grounding
  - Wrist Straps
  - Conductive Smocks, Gloves and Finger Cots
  - Anti-static ID Badges
- Facility
  - Relative Humidity Control and Air Ionizers
  - Dissipative Floors (less than 10^9 Ω to GND)
- Protective Workstation
  - Dissipative Table Tops
  - Protective Test Equipment (Properly Grounded)
  - Grounded Tip Soldering Irons
  - Conductive Solder Suckers
  - Static Sensors
- Protective Packaging and Transportation
  - Bags and Pouches (Faraday Shield)
  - Protective Tote Boxes (Conductive Static Shielding)
  - Protective Trays
  - Grounded Carts
  - Protective Work Order Holders

Ordering Information

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
CX77144	CX77144–15	–15	4x4LM	–30 °C to +85 °C

Revision History

Revision	Level	Date	Description
A		June 9, 2004	Initial Release

References

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752.

Application Note: Tape and Reel, Document Number 101568

Standard SMT Reflow Profiles: JEDEC Standard J–STD–020.

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