

1M BIT (65,536 WORD × 16 BIT) CMOS MASK ROM

DESCRIPTION

The TC531024P/F is a 1,048,576 bits read only memory organized as 65,536 words by 16 bits.
 The TC531024P/F is fabricated using Toshiba's advanced CMOS technology which provides the high speed and low power features with access time of 120ns/150ns, an operation current of 40mA at 8.3MHz and a standby current of 20µA.

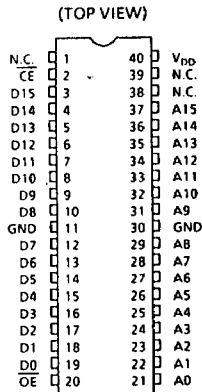
The TC531024P/F is packaged in a standard 600mil 40pin D1P, or 525mil 40pin SOP.

FEATURES

TC531024P/F	- 12	- 15
Power Supply	5V ± 5%	5V ± 10%
Access Time (Max.)	120ns	150ns
Power Dissipation : Operating Current (Max.)	40mA	35mA
Power Dissipation : Standby Current (Max.)	20µA	20µA

- Single 5V Power Supply
- Fully Static Operation
- All Input and Output : TTL Compatible
- Three State Output
- 40pin 600mil width Plastic DIP
- 40pin 525mil width Plastic SOP

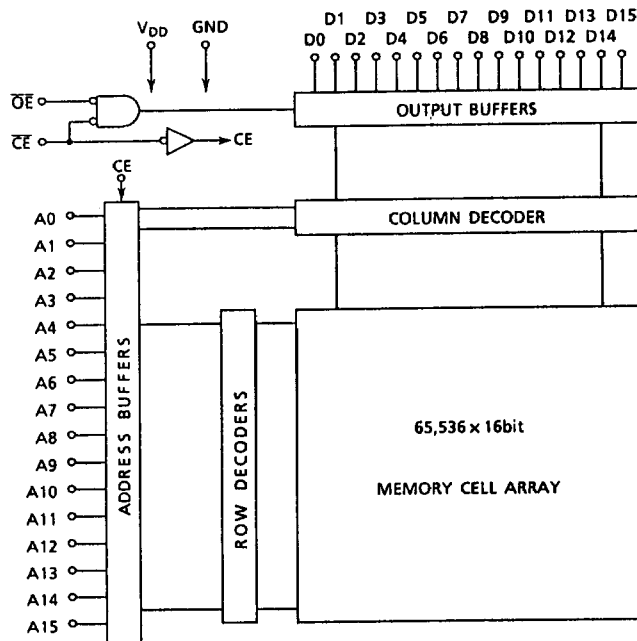
PIN CONNECTION



PIN NAMES

A0~A15	Address inputs
D0~D15	Data Outputs
OE	Output Enable Input
CE	Chip Enable Input
VDD	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



TC531024P-12, TC531024P-15 TC531024F-12, TC531024F-15

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-0.5~ V_{DD}	V
V_{OUT}	Output Voltage	0~ V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	-55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature - Time	260 · 10	°C · sec

Note : * Plastic FP.

D.C. OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3	0.8	V

D.C. OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT	
I_{IL}	Input Leakage Current	$0V \leq V_{IN} \leq V_{DD}$	-	± 1.0	μA	
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{DD}$	-	± 5.0		
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-1.0	-	mA	
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	3.2	-		
I_{DDS1}	Standby Current	$\overline{CE} = 2.2V$	-	2.0	μA	
I_{DD52}		$\overline{CE} = V_{DD} - 0.2V$	-	20		
I_{DD01}	Operating Current	$\overline{CE} = V_{IL}$, $V_{IN} = V_{IH} / V_{IL}$ $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 120\text{ns}$	-	50	mA
			$t_{\text{cycle}} = 150\text{ns}$	-	45	
I_{DD02}		$\overline{CE} = 0.2V$, $V_{IN} = V_{DD} - 0.2V / 0.2V$ $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 120\text{ns}$	-	40	
			$t_{\text{cycle}} = 150\text{ns}$	-	35	

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	-	10	pF
C_{OUT}	Output Capacitance	$f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	-	10	pF

Note : This Parameter is periodically sampled and is not 100% tested.

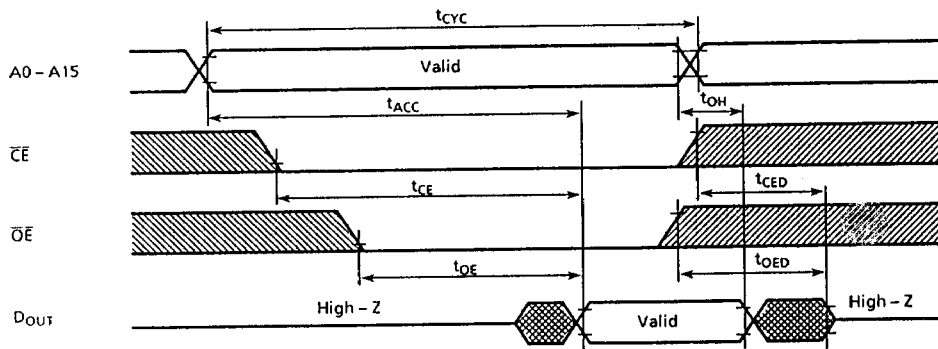
A.C. CHARACTERISTICS (Ta = 0°C~70°C)

SYMBOL	PARAMETER	V _{DD} = 5V ± 5%		V _{DD} = 5V ± 10%		UNIT
		MIN.	MAX.	MIN.	MAX.	
t _{ACC}	Access Time	-	120	-	150	ns
t _{CE}	Chip Enable Access Time	-	120	-	150	ns
t _{OE}	Output Enable Access Time	-	70	-	70	ns
t _{CED}	Output Disable Time from \overline{CE}	0	60	0	60	ns
t _{OED}	Output Disable Time from \overline{OE}	0	60	0	60	ns
t _{OH}	Output Hold Time	5	-	5	-	ns
t _{CYC}	Cycle Time	120	-	150	-	ns

A.C. TEST CONDITIONS

Output Load : 100pF + 1TTL
 Input Levels : 0.6V / 2.4V
 Timing Measurement Reference Levels Input : 0.8V / 2.2V
 Output : 0.8V / 2.0V
 Input Rise and Fall Time (10%~90%) : 5ns

TIMING WAVEFORMS



OPERATION MODE

MODE	\overline{CE}	\overline{OE}	A0~A15	Outputs	Power
Read	L	L	Valid	Data Out	Operating
Standby	H	*	*	High-Z	Standby
Output Deselect	L	H	*	High-Z	Operating

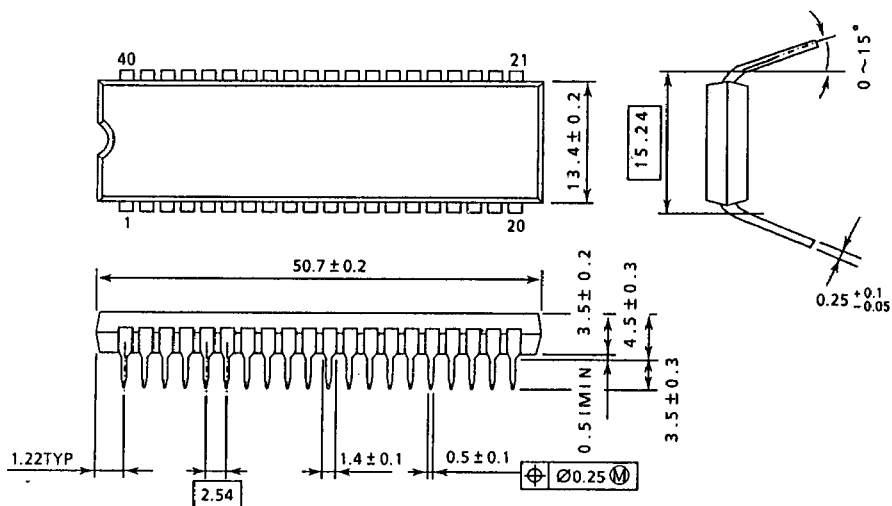
H : VIH L : VIL * : VIH or VIL

TC531024P-12, TC531024P-15 TC531024F-12, TC531024F-15

OUTLINE DRAWINGS

Plastic DIP (DIP40-P-600)

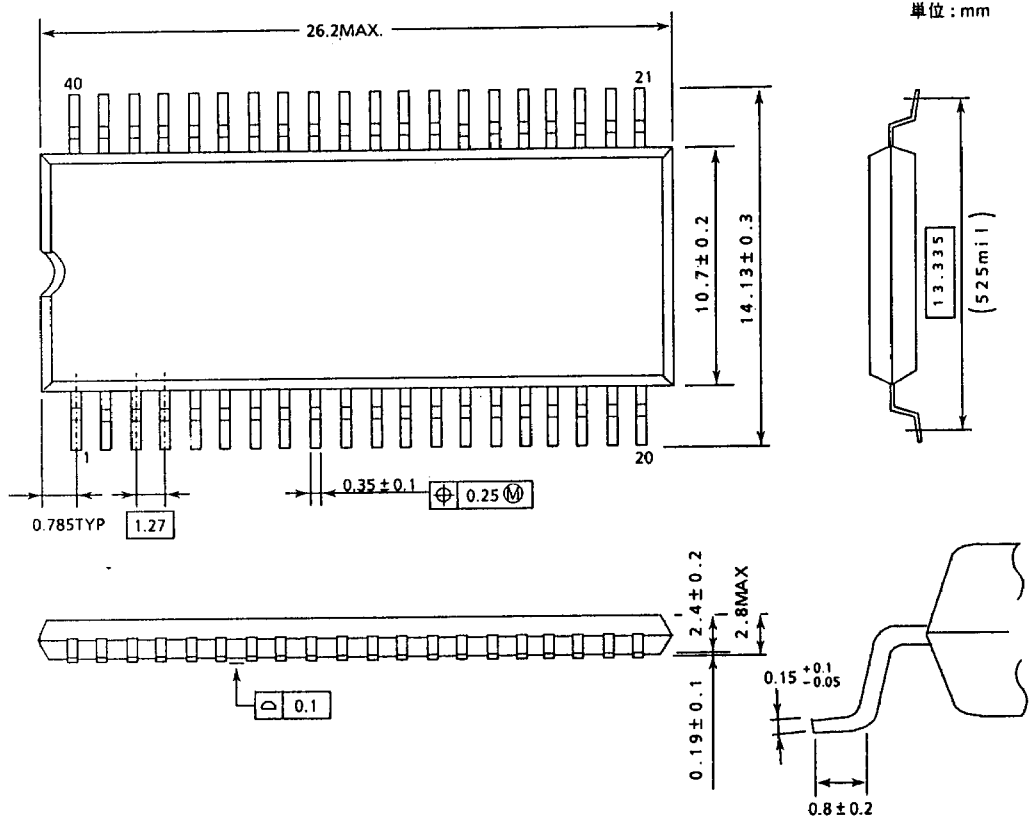
單位 : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

Plastic FP (SOP40-P-525)



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.