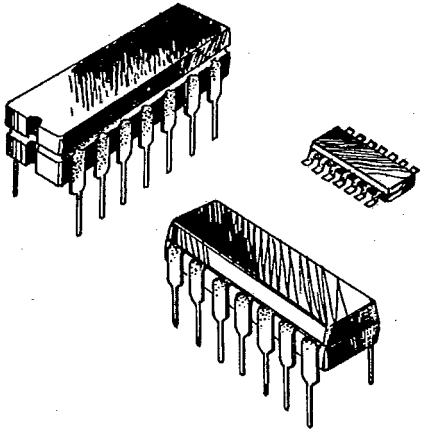
TELEDYNE SEMICONDUCTOR
The Analog Signal Processing Company™

TSC9110
TSC9111

HIGH-VOLTAGE SWITCHMODE CONTROLLERS



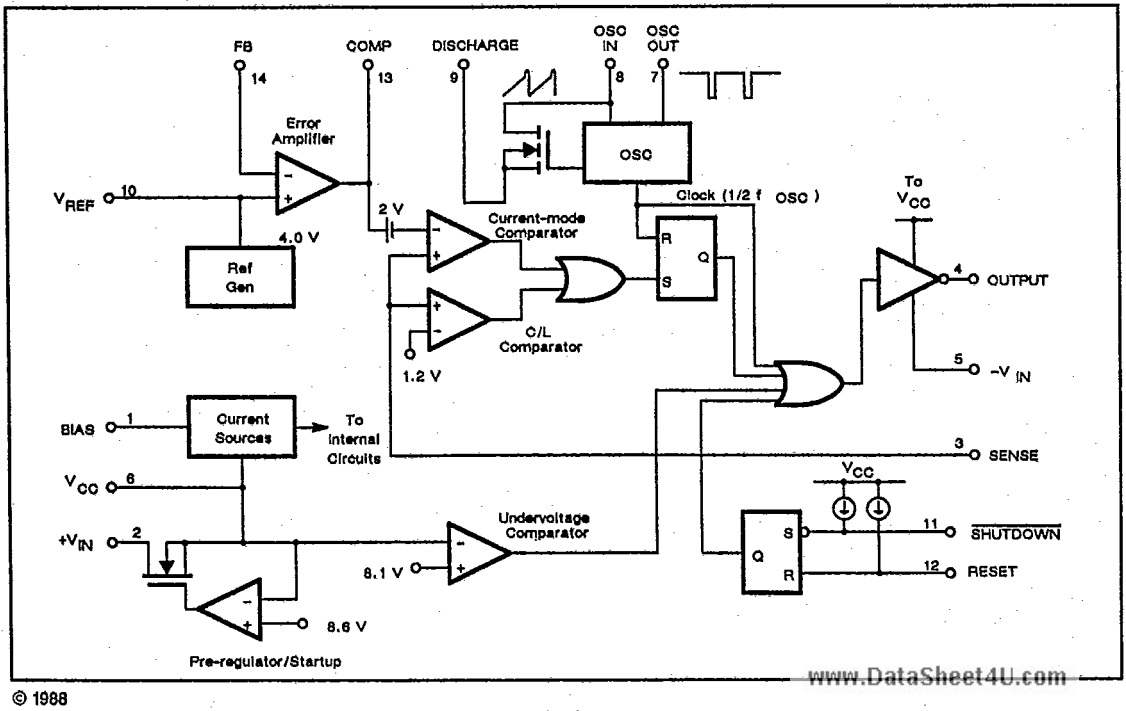
Features

- 10 to 120 V Input Range
- Current-mode Control
- High-Speed, Source-Sink Output Drive
- High Efficiency Operation ..... >80%
- Internal Start-up Circuit
- Internal Oscillator (up to 1 MHz)
- Reference Selection
  - TSC9110 ..... ±1%
  - TSC9111 ..... ±10%

Applications

- DC/DC Converters
- Distributed Power Systems
- ISDN Equipment
- PBX Equipment
- Modems

Functional Diagram



TSC9110
TSC9111

SWITCHMODE CONTROLLERS

T-58-11-31

General Description

The TSC9110/TSC9111 are D/CMOS integrated circuits designed for use as high-performance switchmode controllers. A high-voltage DMOS input allows the controller to work over a wide range of input voltages (10- to 120-VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce internal power consumption to less than 10 mW.

The on-chip oscillator frequency is set by an external resistor, and can be easily synchronized to an external system clock. $\overline{\text{SHUTDOWN}}$ and $\overline{\text{RESET}}$ inputs allow external logic control, and these inputs can also be used to provide a variable shutdown time for fault protection. A push-pull output driver provides high-speed switching for MOSPOWER devices large enough to supply 50 W of output power. When combined with an output MOSFET and transformer, the TSC9110 or TSC9111 can be used to implement most single-ended power converter topologies (i.e., flyback and forward).

The TSC9110 and TSC9111 are available in 14-pin plastic, SO-IC and CerDIP packages, and are specified over the military, M suffix (−55 to +125°C) and industrial, E suffix (−40 to +85°C) temperature ranges.

Absolute Maximum Ratings

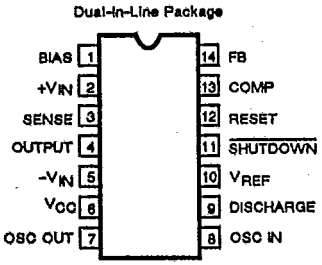
Voltage Referenced to $-V_{IN}$
V_{CC} ..... 15.0 V
$+V_{IN}$ ..... 120 V
Logic Inputs ($\overline{\text{RESET}}$, $\overline{\text{SHUTDOWN}}$, OSC IN) ..... −0.3 V to V_{CC} + 0.3 V
Linear Inputs (FEEDBACK, SENSE) ..... −0.3 V to 7.0 V
HV Preregulator Input Current (continuous) ..... 3 mA
Storage Temperature (M, E Suffix) ..... −65 to +150°C
Operating Temperature (M Suffix) ..... −55 to +125°C
(E Suffix) ..... −40 to +85°C
Junction Temperature (T_J) ..... +150°C

Power Dissipation (Package)[1]
14-Pin Ceramic DIP (K Suffix)[2] ..... 1000 mW
14-Pin Plastic DIP (J Suffix)[3] ..... 750 mW
14-Pin SO-IC (Y Suffix)[4] ..... 800 mW

Thermal Impedance (θ_{JA})
14-Pin Ceramic DIP ..... +100°C/W
14-Pin Plastic DIP ..... +167°C/W
14-Pin SO-IC ..... +140°C/W

NOTES: [1]Device mounted with all leads soldered or welded to PC board
[2]Derate 10 mW/°C above +50°C
[3]Derate 6 mW/°C above +25°C
[4]Derate 7 mW/°C above +25°C

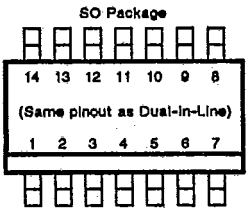
Pin Configuration



Top View

Order Numbers:

CerDIP: TSC9110EJF, TSC9111EJF
Plastic: TSC9110EPF, TSC9111EPF



Top View

Order Numbers:

TSC9110EOF, TSC9111EOF

Electrical Characteristics: DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ, T = +25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	TYP[2]	LIMITS M SUFFIX −55 to +125°C MIN	M SUFFIX −55 to +125°C MAX	E SUFFIX −40 to +85°C MIN	E SUFFIX −40 to +85°C MAX	UNIT
Reference								
V_R	Output Voltage	R_L = 10 MΩ (See Detailed Description)	4.0					V
Z_{OUT}	Output Impedance		30					kΩ
	Short Circuit Current	$V_{REF} = -V_{IN}$	100					μA
	Temperature Stability	See Note 3	1					mV/°C
Oscillator								
f_{OSC}	Maximum Frequency	R_{OSC} = 0	3	1		1		MHz
	Initial Accuracy	See Note 4	100	80	120	80	120	kHz
V_{OSC}	Voltage Stability	9.5 V ≤ V_{CC} ≤ = 13.5 V	±3					%
	Temperature Coefficient	See Note 3	500					ppm/°C
Error Amplifier								
V_{FB}	Feedback Input Voltage	FB tied to COMP TSC9110 See Detailed Description Reference Section TSC9111	4.00	3.96	4.04	3.96	4.04	V
			4.00	3.60	4.40	3.60	4.40	V
	Input BIAS Current	V_{FB} = 4.0 V	25		500		500	nA
A_{VOL}	Open Loop Voltage Gain		80	60		60		dB
	Unity Gain Bandwidth		1					MHz
Z_{OUT}	Output Impedance		50					kΩ
I_{OUT}	Output Current	Source V_{FB} = 3.4 V Sink V_{FB} = 4.5 V	2.0 0.15	1.4 .12		1.4 .12		mA mA
PSRR	Power Supply Rejection	9.5 V ≤ V_{CC} ≤ = 13.5 V	70					dB
Current Limit								
V_{SOURCE}	Threshold Voltage	V_{FB} = 0 V	1.2	1.0	1.4	1.0	1.4	V
t_d	Delay to Output	V_{SENSE} = 1.4 V, See Figure 1	100		150		150	ns
Preregulator/Startup								
$+V_{IN}$	Input Voltage	I_{IN} = 10 μA			120		120	V
$+I_{IN}$	Input Leakage Current	V_{CC} ≥ 9.4 V			10		10	μA
	V_{CC} Preregulator Turn-OFF Threshold Voltage	$I_{PREREGULATOR}$ = 10 μA	8.6		9.4		9.4	V
	Undervoltage Lockout	I_{OUTPUT} = 1 mA (See Detailed Description)	8.1		8.9		8.9	V

Electrical Characteristics (Cont.): DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ, T = +25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	TYP[2]	LIMITS M SUFFIX −55 to +125°C MIN	LIMITS M SUFFIX −55 to +125°C MAX	LIMITS E SUFFIX −40 to +85°C MIN	LIMITS E SUFFIX −40 to +85°C MAX	UNIT
Supply								
I_{CC}	Supply Current		0.6		1.0		1.0	mA
I_{BIAS}	Bias Current		15					µA
Logic								
t_{SD}	$\overline{\text{SHUTDOWN}}$ Delay	C_L = 500 pF $V_{SENSE} = -V_{IN}$ See Figure 2	50		100		100	ns
t_{SW}	$\overline{\text{SHUTDOWN}}$ Pulse Width	See Figure 3		50		50		ns
t_{RW}	RESET Pulse Width	See Figure 3		50		50		ns
t_{LW}	Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET LOW	See Figure 3		25		25		ns
V_{IL}	Input LOW Voltage				2.0		2.0	V
V_{IH}	Input HIGH Voltage			8.0		8.0		V
I_{IH}	Input Current Input Voltage HIGH	V_{IN} = 10V	1		5		5	µA
I_{IL}	Input Current Input Voltage LOW	V_{IN} = 0V	−25		−35		−35	µA
OUTPUT								
V_{OH}	Output HIGH Voltage	I_{OUT} = 1 mA		9.90		9.90		V
		See Note 3		9.75		9.75		V
V_{OL}	Output LOW Voltage	I_{OUT} = −1 mA			0.10		0.10	V
		See Note 3			0.25		0.25	
R_{OUT}	Output Resistance		20		30		30	Ω
		See Note 3	25		50		35	Ω
t_r	Rise Time	C_L = 500 pF	40		75		75	ns
t_f	Fall Time	C_L = 500 pF	40		75		75	ns

NOTES: 1. Guaranteed by design, not subject to production test.
2. Typical Values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
3. Temperature = +125, +85°C; [illegible]
4. C_{STRAY} Pin 8 = 0 pF.

Timing Waveforms

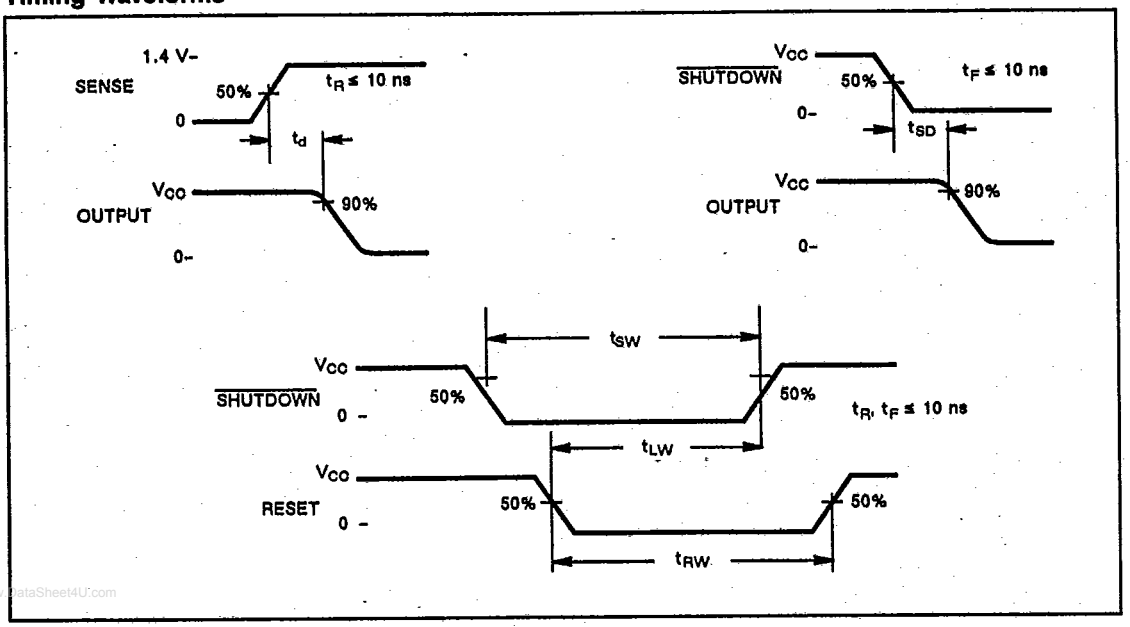
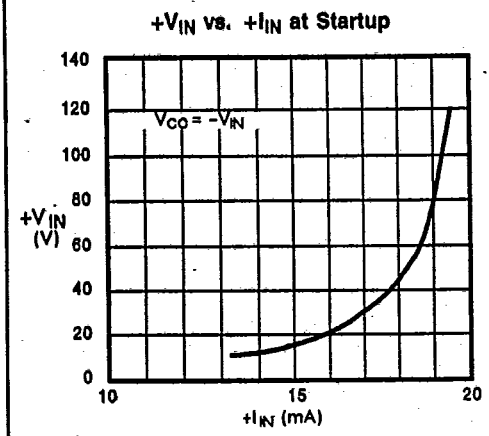


Figure 3

Typical Characteristics



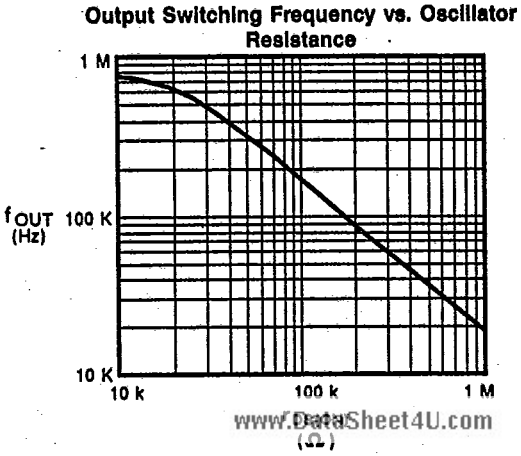


Figure 4 and Figure 5

Detailed Description

Preregulator/Startup Section

Due to the low quiescent current requirement of the TSC9110/TSC9111 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during startup, $+V_{IN}$ (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} (pin 6). This startup circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6 V. If V_{CC} is not forced to exceed the 8.6 V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the preregulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns ON. The design of the IC is such that the undervoltage lockout threshold will not exceed the preregulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

NOTE: During startup or when V_{CC} drops below 8.6 V the startup circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48 V input, approximately 1 W). Excessive startup time can result in device damage. See Figure 4 for calculation of power dissipation during startup.

Bias

To properly set the bias for the TSC9110/TSC9111, a 390 kΩ resistor should be tied from BIAS (pin 1) to $-V_{IN}$ (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

Reference Section

The reference section of the TSC9110 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4.0 V. The trimming procedure that is used on the TSC9110 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±1% of 4.0 V. This automatically compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Applications which use a separate external reference, such as non-isolated converter topologies and circuits employing optical coupling in the feedback loop, do not require a trimmed voltage reference with 1% accuracy. The TSC9111 accommodates the requirements of these applications at a lower cost, by leaving the reference voltage untrimmed. The 10% accurate reference thus provided is sufficient to establish a DC bias point for the error amplifier.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. An MOS differential input stage provides for low input current. The non-inverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to ≤50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization pulse into the OSC IN (pin 8) terminal. For a 5 V pulse amplitude, typical values would be 1000 pF in series with 10 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is OFF whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and can be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Table 1: Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET pins

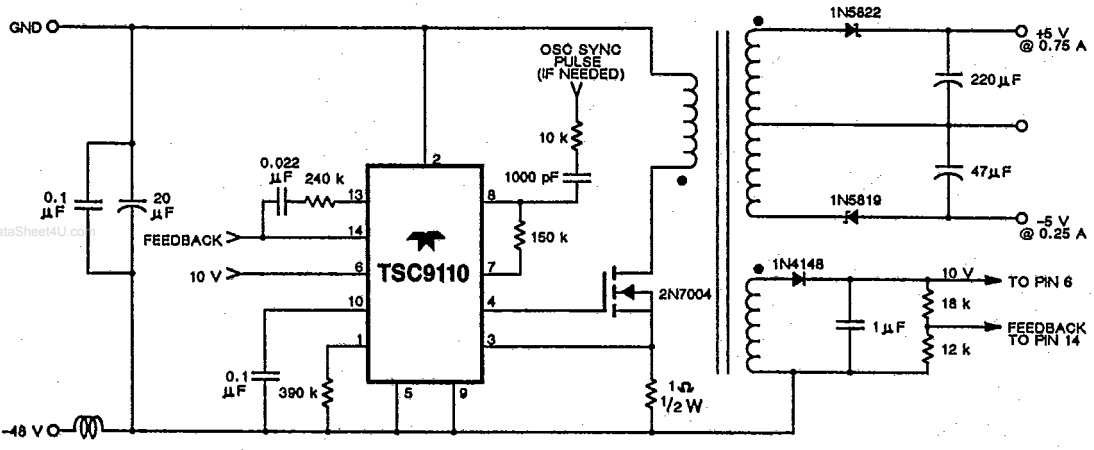
$\overline{\text{SHUTDOWN}}$	RESET	OUTPUT
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	OFF (Not Latched)
L	↓	OFF (Latched)
↓	L	OFF (Latched) (No Change)

Output Switch

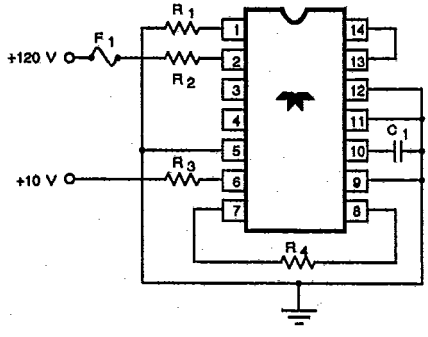
The push-pull driver output has a typical ON resistance of 20 Ω. Maximum switching times are specified at 75 ns for a 500 pF load. This is sufficient to directly drive MOSFETs such as the 2N7004, 2N7005, IRFD120 and IRFD220. Larger devices can be driven, but switching times will be longer, resulting in higher switching losses. In order to drive large MOSPOWER devices, it is necessary to use an external driver IC, such as the Siliconix D469. The D469 can switch very large devices such as the SMM20N50 (500 V, 0.3 Ω) in approximately 100 ns.

Applications

5-Watt Power Supply for Telecom Applications



Burn-In Circuit



NOTES:
1. R_1 = 390 kΩ, ¼ W
2. R_2 = 1 kΩ, 2 W
3. R_3 = 1 kΩ, 2 W
4. R_4 = 100 Ω, ¼ W
5. R_5 = 330 kΩ, ¼ W
6. C_1 = 0.1 µF, 50 V