

UDN-2975W AND UDN-2976W DUAL 4A SOLENOID DRIVERS

FEATURES

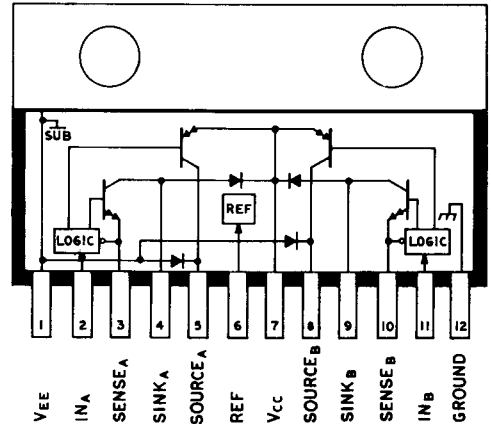
- 5 A Peak Output
- TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Output Voltage to 60 V
- Single-Ended or Split Supply
- Adjustable Short-Circuit Protection
- Internal Clamp Diodes
- Plastic SIP With Heat-Sink Tab

CURRENT CONTROL for operation of a pair of print solenoids is provided by both Type UDN-2975W and UDN-2976W. Each IC's dual driver sections operate directly from the printer control line. The two devices differ only in output-voltage ratings. They can be used at currents of up to 4 A.

Type UDN-2975W is rated at 50 V. Type UDN-2976W is rated at 60 V or ± 30 V. Inputs are compatible with most TTL, DTL, LSTTL, and 5 V to 15 V CMOS and PMOS logic.

Current is controlled by a current-sensing latch method that uses only one external sensing resistor for each driver. The load current is compared with the reference voltage and, at the level fixed by the system designer ($V_{REF}/10 = I_{LOAD} \times R_{SENSE}$), a latch is set, shutting OFF one of the output transistors. The internal flyback diode then maintains the flux without further input from the power supply, resulting in maximum efficiency. The latch is reset by pulling the input high.

For the maximum in power-handling capability, the integrated circuits are supplied in 12-pin single



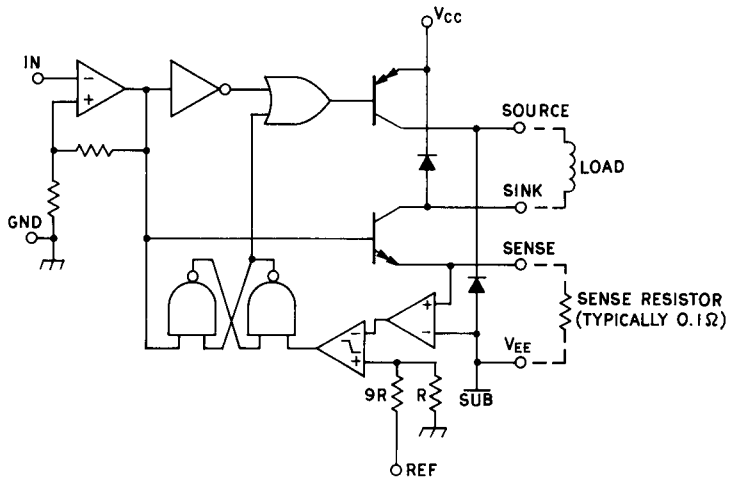
Dwg. No. A-12,105

in-line power tab packages. For proper operation, an external heat sink is required. The tab is at V_{EE} potential and must be insulated from ground when Type UDN-2976W is used with a split supply.

ABSOLUTE MAXIMUM RATINGS at $T_{TAB} = +70^{\circ}\text{C}$

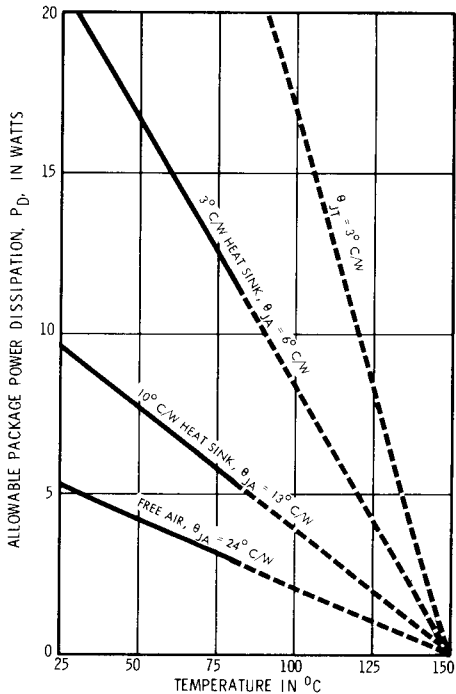
Supply Voltage, V_{CC} (Ref. V_{EE} , UDN-2975W)	50 V
(Ref. V_{EE} , UDN-2976W)	60 V
V_{EE} (Ref. GND, UDN-2975W)	0 V
(Ref. GND, UDN-2976W)	-30 V
Peak Output Current, I_{OUV}	5 A
Input Voltage, V_{IN}	15 V
Reference Voltage, V_{REF}	5 V
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	-20°C to +85°C
Storage Temperature Range, T_S	-55°C to +150°C

FUNCTIONAL BLOCK DIAGRAM
(ONE OF TWO DRIVERS)



Dwg. No. A-12,106A

**ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE**



Dwg. No. A-11,794A

To maintain isolation between integrated circuit components and to provide for normal transistor operation, the substrate (pin 1) must be connected to the most negative point in the external circuit.

TRUTH TABLE

V_{IN}	V_{SENSE}	Source Driver	Sink Driver	Function
High	NA	Off	Off	Off
Low	$< V_{REF}/10$	On	On	On
Low	$> V_{REF}/10$	Off	On	Flyback

UDN-2975W AND UDN-2976W DUAL 4 A SOLENOID DRIVERS

ELECTRICAL CHARACTERISTICS at $T_A = +25^\circ\text{C}$, $T_{\text{TAB}} \leq +70^\circ\text{C}$, $V_{\text{CC}} = 45\text{ V}$ (UDN-2975W) or 55 V (UDN-2976W), $V_{\text{EE}} = V_{\text{SENSE}} = 0\text{ V}$ (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits		
				Min.	Max.	Units
Supply Voltage Range	V_{CC}	UDN-2975W	Operating	20	50	V
		UDN-2976W	Operating	20	60	V
Supply Current	I_{CC}	Both	Outputs Open	—	25	mA
	I_{EE}	Both	Outputs Open	—	-20	mA

Output Drivers

Output Leakage Current	I_{CEX}	UDN-2975W	$V_{\text{IN}} = 2.4\text{ V}$, $V_{\text{CC}} = 50\text{ V}$, $V_{\text{SOURCE}} = 0\text{ V}$	—	100	μA
			$V_{\text{IN}} = 2.4\text{ V}$, $V_{\text{SINK}} = V_{\text{CC}} = 50\text{ V}$	—	100	μA
		UDN-2976W	$V_{\text{IN}} = 2.4\text{ V}$, $V_{\text{CC}} = 60\text{ V}$, $V_{\text{SOURCE}} = 0\text{ V}$	—	100	μA
			$V_{\text{IN}} = 2.4\text{ V}$, $V_{\text{SINK}} = V_{\text{CC}} = 60\text{ V}$	—	100	μA
Output Saturation Voltage	$V_{\text{CE(SAT)}}$	Both	Source Drivers, $I_{\text{LOAD}} = 4\text{ A}$	—	3.5	V
			Sink Drivers, $I_{\text{LOAD}} = 4\text{ A}$	—	2.5	V
Output Sustaining Voltage (Source drivers only)	$V_{\text{CE(SUS)}}$	UDN-2975W	$I_{\text{LOAD}} = 4\text{ A}$, $L = 3.5\text{ mH}$	50	—	V
		UDN-2976W	$I_{\text{LOAD}} = 4\text{ A}$, $L = 3.5\text{ mH}$	60	—	V
Clamp Diode Forward Voltage	V_{F}	Both	$I_{\text{F}} = 4\text{ A}$	—	2.0	V
Output Rise Time	t_{r}	Both	$I_{\text{LOAD}} = 4\text{ A}$, 10% to 90%, Resistive Load	—	2.0	μs
Output Fall Time	t_{f}	Both	$I_{\text{LOAD}} = 4\text{ A}$, 90% to 10%, Resistive Load	—	2.0	μs

Control Logic

Logic Input Voltage	$V_{\text{IN(1)}}$	Both		2.0	—	V
	$V_{\text{IN(0)}}$	Both	See Notes	—	0.5	V
Logic Input Current	$I_{\text{IN(1)}}$	Both	$V_{\text{IN}} = 2.4\text{ V}$	—	20	μA
	$I_{\text{IN(0)}}$	Both	$V_{\text{IN}} = 0.4\text{ V}$	—	-20	μA
	$I_{\text{REF(1)}}$	Both	$V_{\text{REF}} = 5.0\text{ V}$	—	-20	μA
Reference/Sense Ratio	—	Both	$V_{\text{REF}} = 2.0\text{ to }5.0\text{ V}$	9.5	10.5	—
Propagation Delay Time	t_{pd}	Both	50% V_{in} to 50% V_{out} , Resistive Load	—	3.0	μs
			100% V_{sense} to 50% V_{out} *, Resistive Load	—	3.0	μs
Minimum Reset Pulse Width	t_{in}	Both		—	1.0	μs

*Where $V_{\text{sense}} = V_{\text{REF}}/10.5$

NOTES: Negative current is defined as coming out of (sourcing) the specific device pin.

For improved noise immunity, hysteresis insures $V_{\text{in(0)}}$ of 0.8 V max. after V_{in} is 0.5 V or less.