4-Port FC/GE Retimer and FC-AL Port Bypass Controller

GENERAL

- Supports 4 Fibre Channel Physical Interfaces at 1.0625 or 2.125 Gbit/s per Fibre Channel – Physical Interface (FC-PI) or 4 Gigabit Ethernet Retimers at 1.25 Gbit/s per IEEE 802.3z.
- Each port supports FC 1G or 2G rate detection/auto-selection.
- Supports Arbitrated Loop and Retimer configuration.
- Each port is independently selectable to perform retimer, reclocker or bypass-path function.
- Non-blocking crossconnect supports protection switching, broadcasting and multicasting.
- Automatic selection of retimer, reclocker or bypass-path function to minimize latency and jitter when a disk is bypassed.
- Per-port receive monitoring for loss of signal, error rate, and link level violations.
- Supports single-ended or differential 106.25 MHz reference clock REFCLK for Fibre Channel applications or 125 Mhz reference clock for Gigabit Ethernet applications.

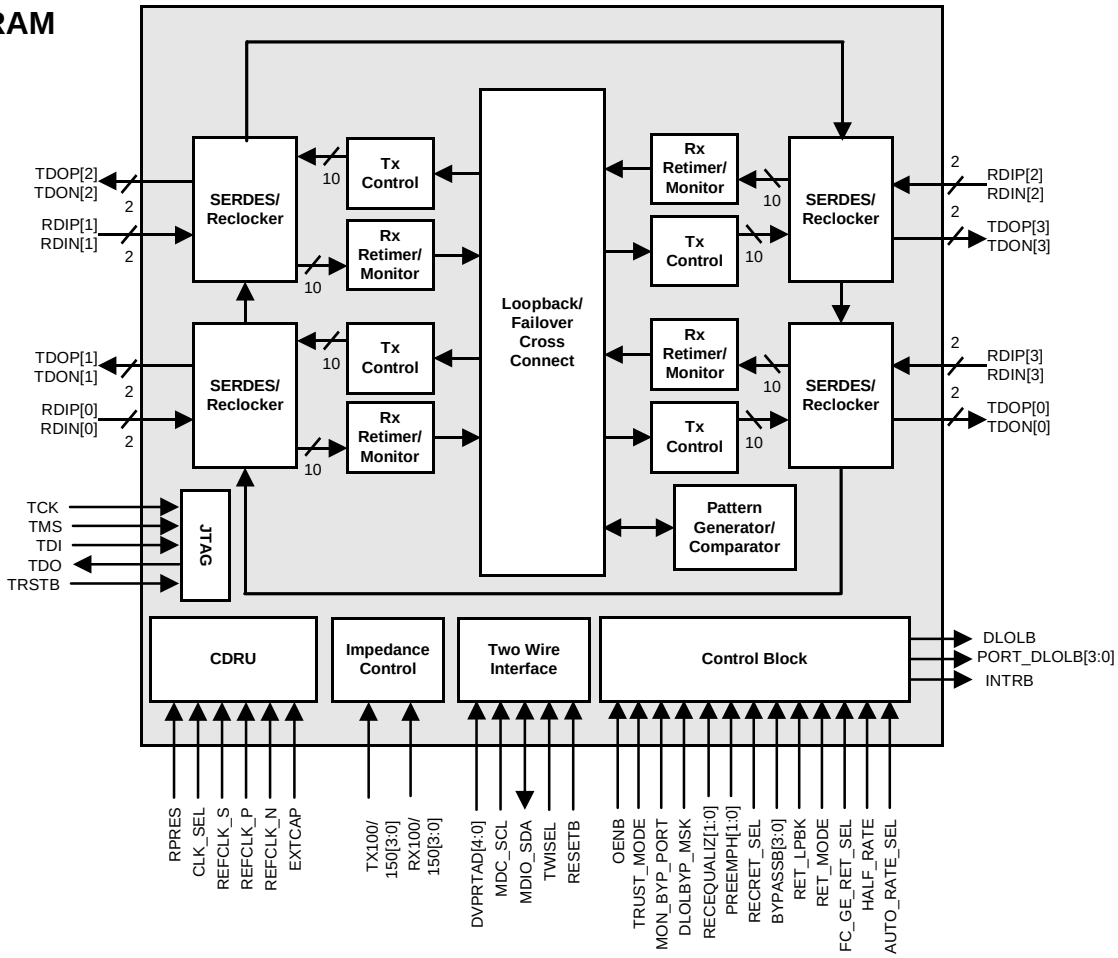
HIGH-SPEED INTERFACE

- High-speed outputs with selectable pre-emphasis per port to counteract dielectric losses and allow maximum reach on printed circuit boards.
- Selectable receive input equalization for improved signal integrity.
- Minimized board footprint and improved signal integrity achieved because:
  - No external components are required to interface the high-speed signals to optics, coax, or serial backplanes using the internal AC coupling capacitors and terminating resistors.
  - Receive input termination of 100 Ω or 150 Ω differential is selectable.
  - Source output impedance of 100 Ω or 150 Ω differential is programmable.

TEST AND CONTROL

- Supports optional 2-pin serial management interface using selectable Two-Wire Interface (TWI) or MDC/MDIO protocol for configuration and diagnostic access.
- For normal mode of operation, a management interface is not required.
- Digital Loss of Link (DLOLB) detect outputs for monitoring individual or multiple links. DLOLB can be programmed to indicate excessive 8B/10B code error rate, loss of synchronization, loss of signal, CRC32 errors, or comma density.
- Interrupt output to flag changes in bypass state and DLOLB error conditions.
- Supports built-in self-test (BIST) via internal Fibre Channel pattern generation and checking.
- External control pins can be overwritten by registers.

BLOCK DIAGRAM



4-Port FC/GE Retimer and FC-AL Port Bypass Controller

- Supports internal serial loop back modes for each port for testing and debugging.
- Provides a standard 5-signal IEEE 1149.1 JTAG test port for boundary scan board testing purposes.

APPLICATIONS

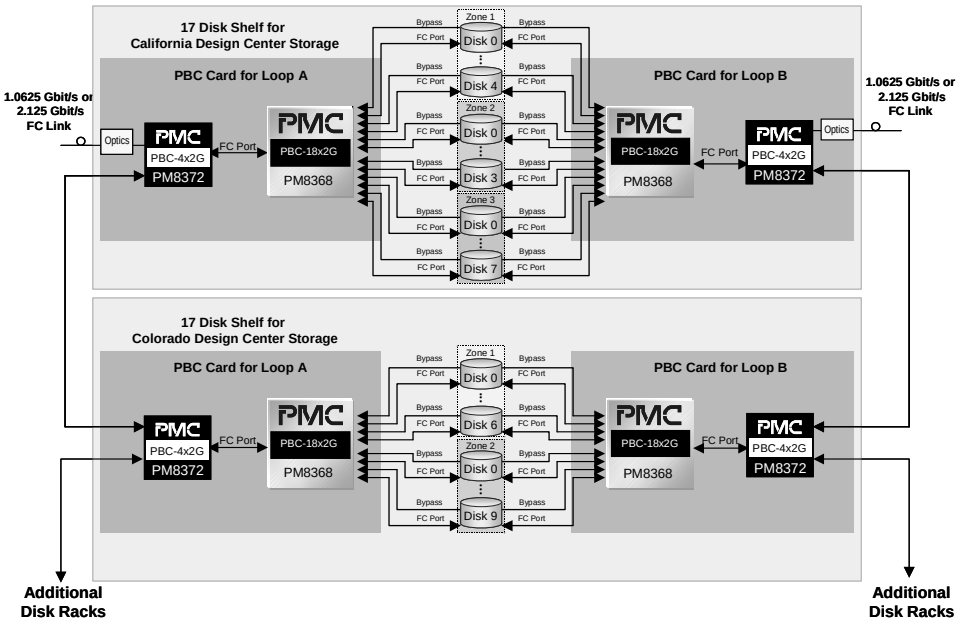
- FC-AL Nodes.
- RAID Storage Systems.
- JBOD Storage Systems.
- MBOD Storage Systems.
- SBOD Storage Systems.
- Fibre Channel Hubs.
- 1.0625/2.125 Gbit/s Backplanes.
- Gigabit Ethernet Retimer.

PHYSICAL

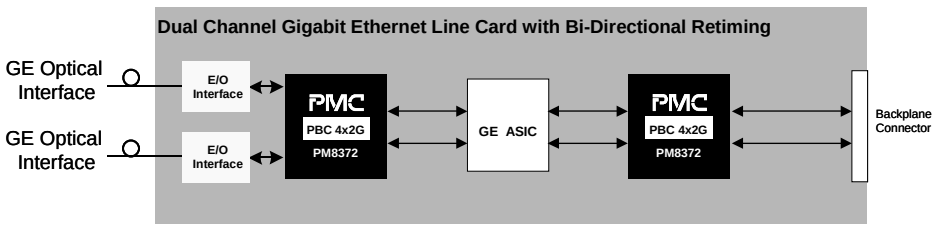
- 0.18 µ CMOS, 1.8 V and 3.3 V supply.
- Small 15 mm x 15 mm footprint, 196-pin CABGA with 1 mm ball pitch.
- Ultra-low operating power of 1.1 W typical with all 4 channels active at 2.125 G.

EXAMPLE APPLICATIONS

MBOD Storage System Application



Gigabit Ethernet Retimer Application



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