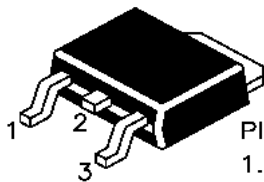


NPN SILICON POWER TRANSISTOR

CJD81

DPAK (TO-252)
Plastic Package



PIN CONFIGURATION
1. BASE
2. COLLECTOR
3. EMITTER

For High Current Driver Applications

ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$)

DESCRIPTION	SYMBOL	VALUE	UNITS
Collector Base Voltage	V_{CBO}	30	V
Collector Emitter Voltage	V_{CEO}	10	V
Emitter Base Voltage	V_{EBO}	6.0	V
Collector Current	I_C	3.0	A
Collector Current (Pulse)	I_{CP}	5.0	A
Collector Power Dissipation	P_D	0.9	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	- 55 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_a=25^\circ\text{C}$ unless specified otherwise)

DESCRIPTION	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Collector Emitter Voltage	V_{CEO}	$I_C=1\text{mA}, I_B=0$	10			V
Collector Base Voltage	V_{CBO}	$I_C=10\mu\text{A}, I_E=0$	30			V
Emitter Base Voltage	V_{EBO}	$I_E=10\mu\text{A}, I_C=0$	6.0			V
Collector Cut Off Current	I_{CBO}	$V_{CB}=20\text{V}, I_E=0$			0.1	μA
Emitter Cut Off Current	I_{EBO}	$V_{EB}=4\text{V}, I_C=0$			0.1	μA
DC Current Gain	h_{FE}	$I_C=3\text{A}, V_{CE}=2\text{V}$	140			

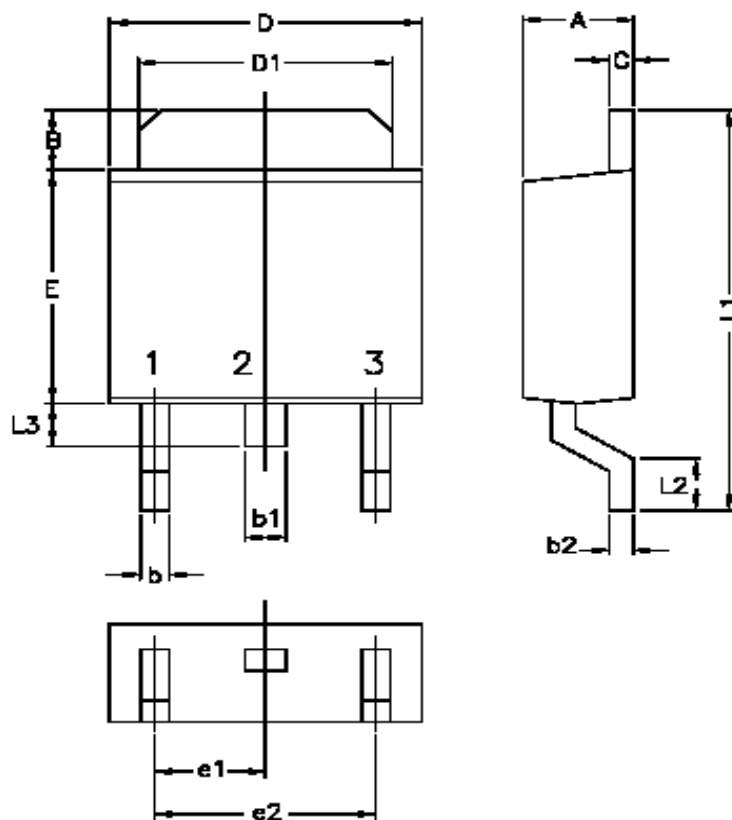
DYNAMIC CHARACTERISTICS

Transition Frequency	f_T	$V_{CE}=10\text{V}, I_C=50\text{mA}$		200		MHz
Output Capacitance	C_{ob}	$V_{CB}=10\text{V}, I_E=0, f=1\text{MHz}$	30			pF

MARKING	CDIL CJD81 MX XY
XY= Date Code	

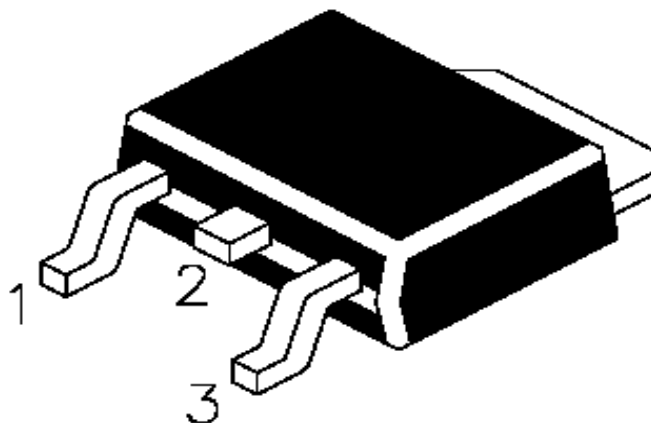
CJD81Rev230205E

DPAK PACKAGE OUTLINE DIMENSIONS



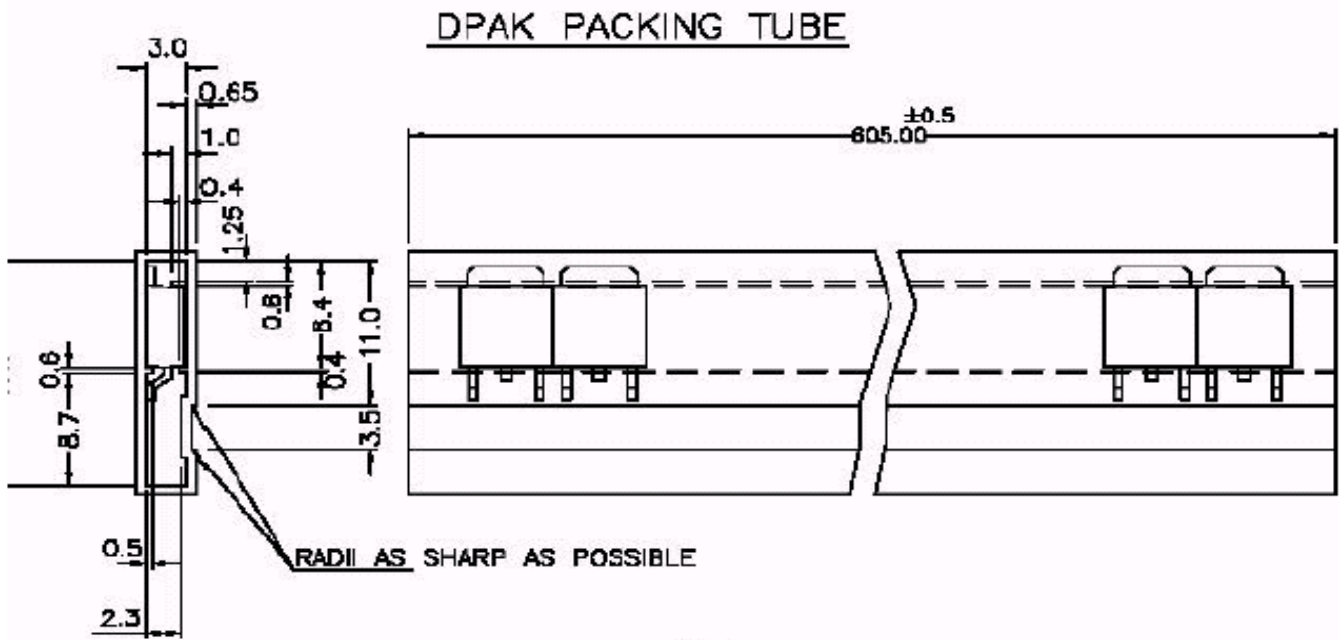
DIM	MIN.	MAX.
A	2.20	2.40
B	1.30	1.50
b	0.55	0.65
b1	0.75	0.85
b2	0.46	0.56
C	0.46	0.56
D	6.40	6.60
D1	5.20	5.40
E	5.40	5.60
e1	2.25	2.35
e2	4.50	4.70
L1	9.25	9.75
L2	0.5	—
L3	0.90	1.10

ALL DIMENSIONS ARE IN mm



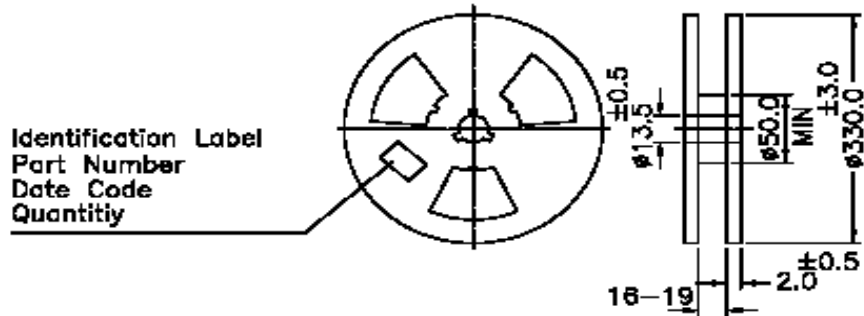
PIN CONFIGURATION

1. BASE
2. COLLECTOR
3. EMITTER



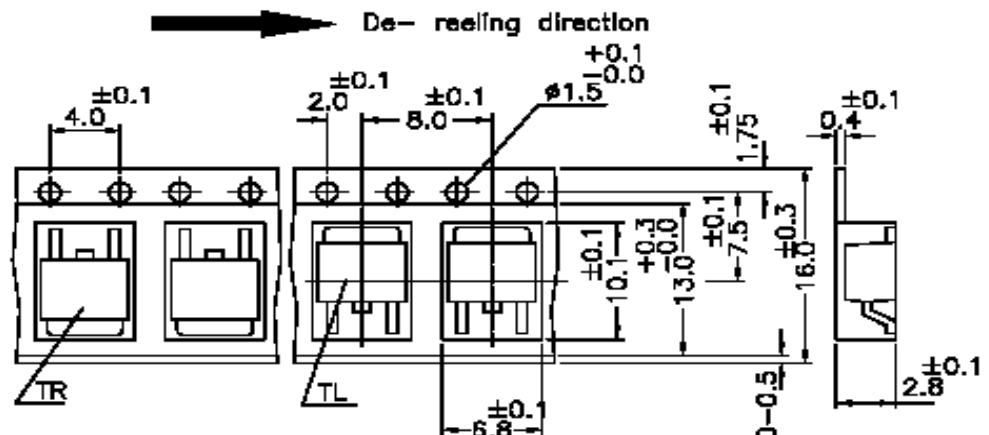
NOTE:—
60 Pcs/TUBE
ALL DIMENSIONS ARE IN mm

DPAK TAPE & REEL SPECIFICATION



ALL DIMENSIONS ARE IN mm
 REEL ϕ 330 mm (13")
 No of Device 2500

TAPE & REEL

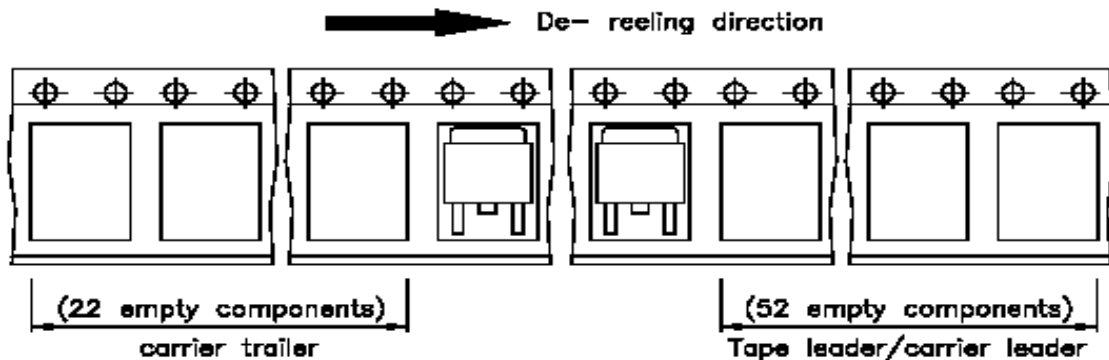


Discrete Suffix - T4
 Analog Suffix - RK

Discrete, Analog Suffix - T5

Notes:-

A maximum of three consecutive components may be missing. Provided this gap is followed by six consecutive components.



Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Discrete Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Discrete Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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