

General Description

The AAT8343 is a low threshold P-channel MOSFET designed for the battery, cell phone, and PDA markets. Using AnalogicTech's ultra-high-density proprietary TrenchDMOS™ technology, this product demonstrates high power handling and small size.

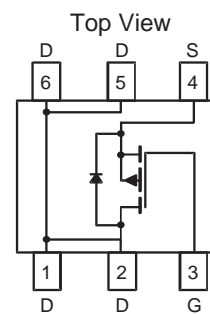
Applications

- Battery Packs
- Battery-Powered Portable Equipment
- Cellular and Cordless Telephones

Features

- Drain-Source Voltage (max): -20V
- Continuous Drain Current¹ (max): -4.5A @ 25°C
- Low On-Resistance:
 - 60mΩ @ $V_{GS} = -4.5V$
 - 110mΩ @ $V_{GS} = -2.5V$

TSOP-6 Package



Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$, unless otherwise noted.

| Symbol | Description | Value | Units | |
|-----------|---|--------------------------|------------------|---|
| V_{DS} | Drain-Source Voltage | -20 | V | |
| V_{GS} | Gate-Source Voltage | ± 12 | | |
| I_D | Continuous Drain Current @ $T_J = 150^\circ\text{C}^1$ | $T_A = 25^\circ\text{C}$ | ± 4.5 | A |
| | | $T_A = 70^\circ\text{C}$ | ± 3.6 | |
| I_{DM} | Pulsed Drain Current ² | ± 16 | | |
| I_S | Continuous Source Current (Source-Drain Diode) ¹ | -1.3 | | |
| T_J | Operating Junction Temperature Range | -55 to 150 | $^\circ\text{C}$ | |
| T_{STG} | Storage Temperature Range | -55 to 150 | $^\circ\text{C}$ | |

Thermal Characteristics¹

| Symbol | Description | Typ | Max | Units |
|------------------|-------------------------------------|--------------------------|-----|---------------------------|
| $R_{\theta JA}$ | Junction-to-Ambient Steady State | 95 | 115 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA2}$ | Junction-to-Ambient $t < 5$ Seconds | 51 | 62 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JF}$ | Junction-to-Foot | 25 | 30 | $^\circ\text{C}/\text{W}$ |
| P_D | Maximum Power Dissipation | $T_A = 25^\circ\text{C}$ | 2.0 | W |
| | | $T_A = 70^\circ\text{C}$ | 1.3 | |

1. Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 5-second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications. $R_{\theta JF} + R_{\theta FA} = R_{\theta JA}$ where the foot thermal reference is defined as the normal solder mounting surface of the device's leads. $R_{\theta JF}$ is guaranteed by design; however, $R_{\theta CA}$ is determined by the PCB design. Actual maximum continuous current is limited by the application's design.

2. Pulse test: Pulse Width = 300μs.

Electrical Characteristics

$T_J = 25^\circ\text{C}$, unless otherwise noted.

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|--|---|---|------|-----|-----------|------------|
| DC Characteristics | | | | | | |
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0V, I_D = -250\mu A$ | -20 | | | V |
| $R_{DS(ON)}$ | Drain-Source On-Resistance ¹ | $V_{GS} = -4.5V, I_D = -4.5A$ | | 49 | 60 | m Ω |
| | | $V_{GS} = -2.5V, I_D = -3.3A$ | | 85 | 110 | |
| $I_{D(ON)}$ | On-State Drain Current ¹ | $V_{GS} = -4.5V, V_{DS} = -5V$ (pulsed) | -16 | | | A |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS} = V_{DS}, I_D = -250\mu A$ | -0.6 | | | V |
| I_{GSS} | Gate-Body Leakage Current | $V_{GS} = \pm 12V, V_{DS} = 0V$ | | | ± 100 | nA |
| I_{DSS} | Drain Source Leakage Current | $V_{GS} = 0V, V_{DS} = -20V$ | | | -1 | μA |
| | | $V_{GS} = 0V, V_{DS} = -16V, T_J = 70^\circ\text{C}^2$ | | | -5 | |
| g_{fs} | Forward Transconductance ¹ | $V_{DS} = -5V, I_D = -4.5A$ | | 7 | | S |
| Dynamic Characteristics² | | | | | | |
| Q_G | Total Gate Charge | $V_{DS} = -10V, R_D = 2.2\Omega, V_{GS} = -4.5V$ | | 8.5 | | nC |
| Q_{GS} | Gate-Source Charge | $V_{DS} = -10V, R_D = 2.2\Omega, V_{GS} = -4.5V$ | | 1.8 | | |
| Q_{GD} | Gate-Drain Charge | $V_{DS} = -10V, R_D = 2.2\Omega, V_{GS} = -4.5V$ | | 2.9 | | |
| $t_{D(ON)}$ | Turn-On Delay | $V_{DS} = -10V, R_D = 2.2\Omega, V_{GS} = -4.5V, R_G = 6\Omega$ | | 12 | | ns |
| t_R | Turn-On Rise Time | $V_{DS} = -10V, R_D = 2.2\Omega, V_{GS} = -4.5V, R_G = 6\Omega$ | | 32 | | |
| $t_{D(OFF)}$ | Turn-Off Delay | $V_{DS} = -10V, R_D = 2.2\Omega, V_{GS} = -4.5V, R_G = 6\Omega$ | | 64 | | |
| t_F | Turn-Off Fall Time | $V_{DS} = -10V, R_D = 2.2\Omega, V_{GS} = -4.5V, R_G = 6\Omega$ | | 40 | | |
| Source-Drain Diode Characteristics | | | | | | |
| V_{SD} | Source-Drain Forward Voltage ¹ | $V_{GS} = 0, I_S = -4.5A$ | | | -1.3 | V |
| I_S | Continuous Diode Current ³ | | | | -1.3 | A |

1. Pulse test: Pulse Width = 300 μs .

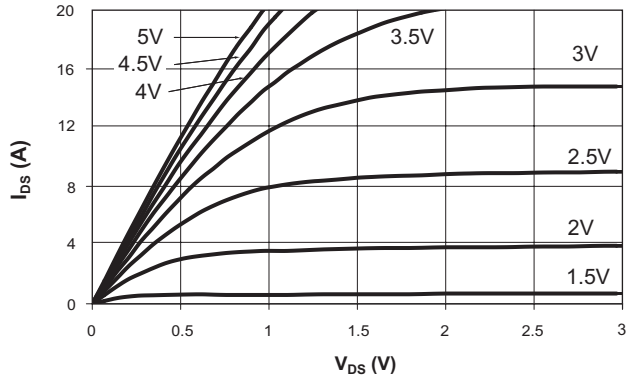
2. Guaranteed by design. Not subject to production testing.

3. Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 5-second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications. $R_{\theta JF} + R_{\theta FA} = R_{\theta JA}$ where the foot thermal reference is defined as the normal solder mounting surface of the device's leads. $R_{\theta JF}$ is guaranteed by design; however, $R_{\theta CA}$ is determined by the PCB design. Actual maximum continuous current is limited by the application's design.

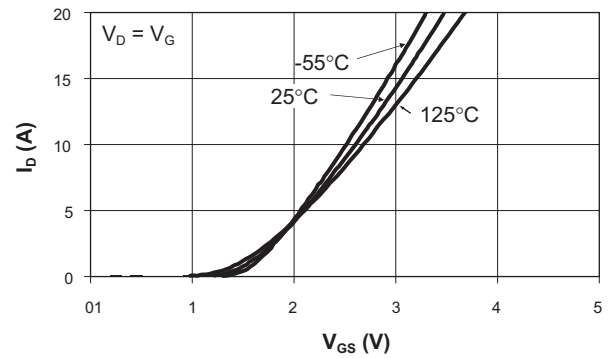
Typical Characteristics

$T_J = 25^\circ\text{C}$, unless otherwise noted.

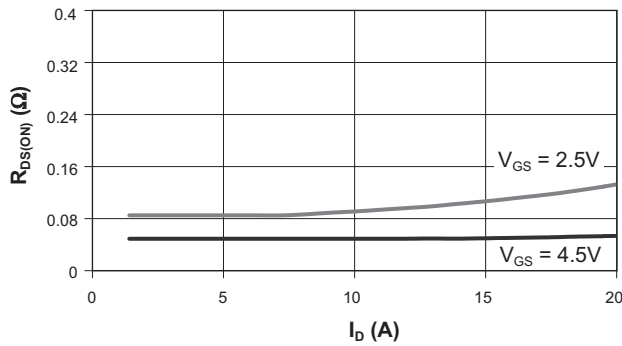
Output Characteristics



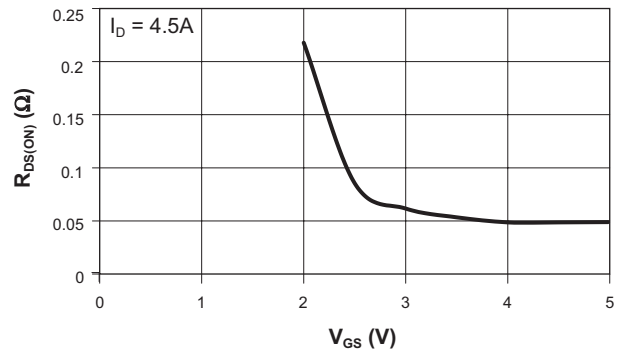
Transfer Characteristics



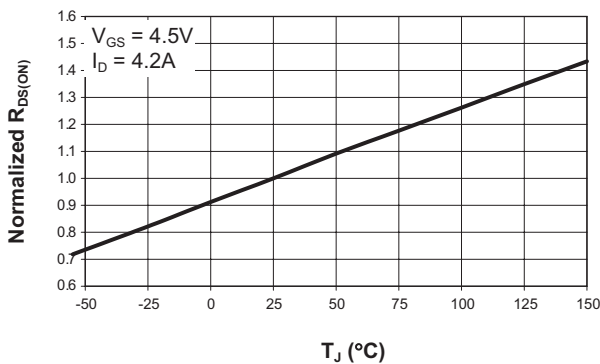
On-Resistance vs. Drain Current



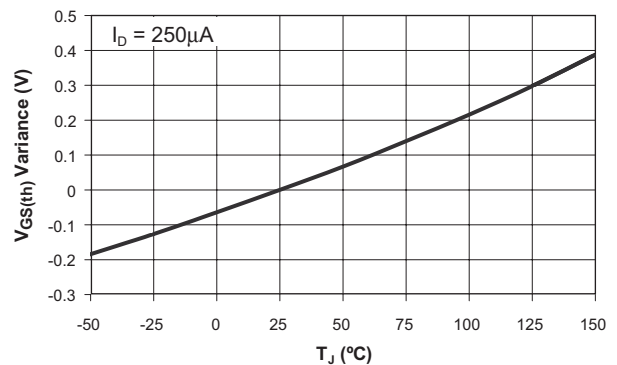
On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Junction Temperature



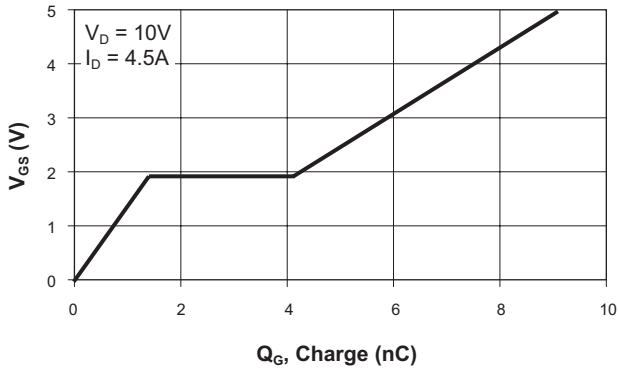
Threshold Voltage



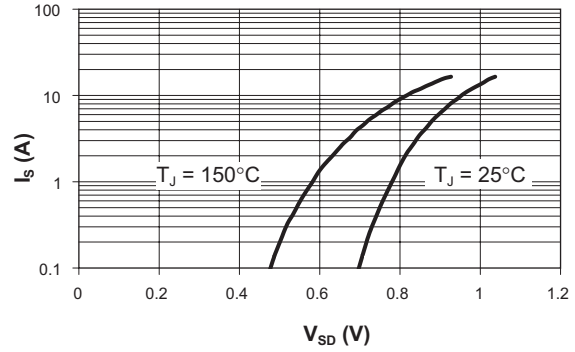
Typical Characteristics

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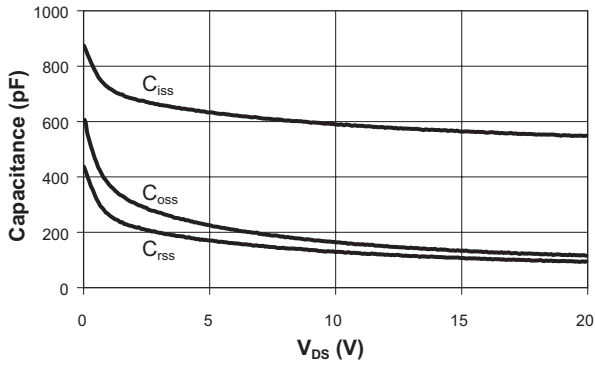
Gate Charge



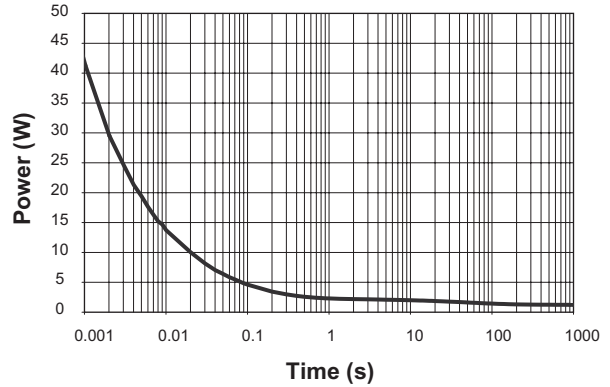
Source-Drain Diode Forward Voltage



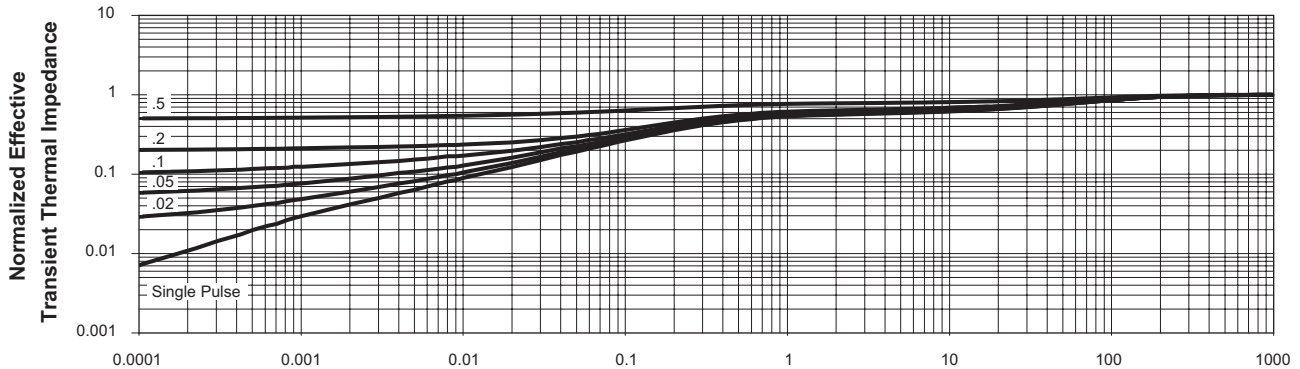
Capacitance



Single Pulse Power, Junction to Ambient



Transient Thermal Response, Junction to Ambient

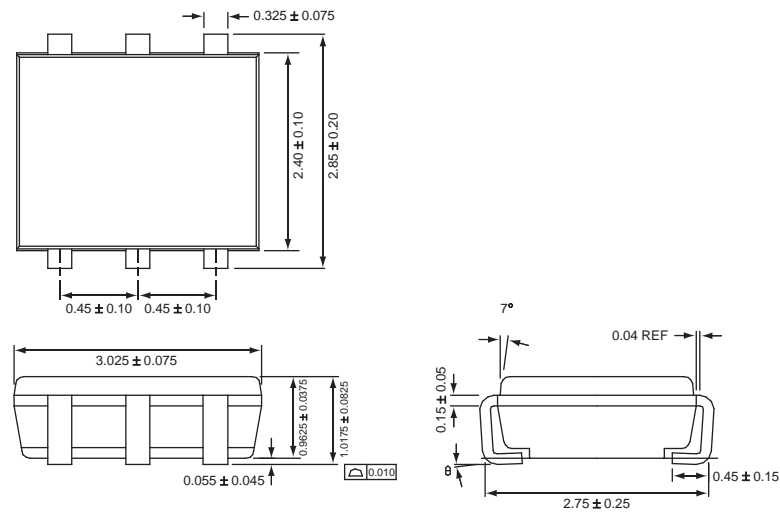


Ordering Information

| Package | Marking ¹ | Part Number (Tape and Reel) ² |
|---------|----------------------|--|
| TSOP-6 | KEXYY | AAT8343IDU-T1 |

Package Information

TSOP-6



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

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