AKD4586
Evaluation board Rev.B for AK4586

GENERAL DESCRIPTION

The AKD4586 is an evaluation board for the AK4586, the Multi-channel Audio CODEC with DIR. The AKD4586 has the digital audio interface and can achieve the interface with digital audio systems via opt-connector or BNC connector.

■ **Ordering guide**

AKD4586 --- Evaluation board for AK4586
(Cable for connecting with printer port of IBM-AT compatible PC and control software are packed with this.)

FUNCTION

- ☐ **On-board analog input buffer circuit**
- ☐ **Compatible with 2 types of interface**
  - **DIT(AK4103)/DIR(AK4586) with optical output/input and BNC input**
  - **Direct interface with AC3 decoder by 10pin header**
- ☐ **10pin header for serial control interface**

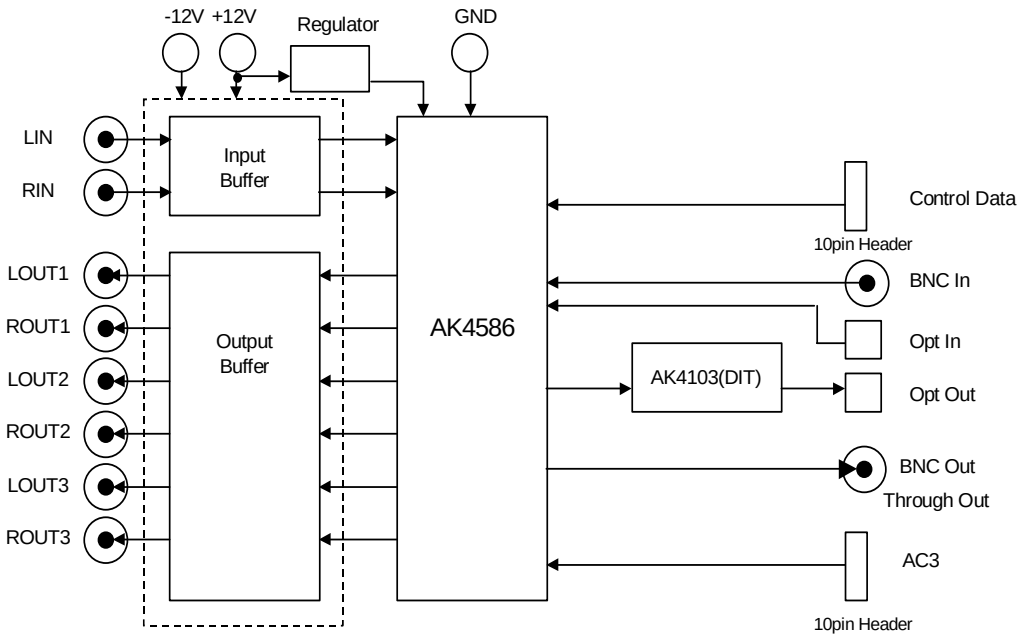
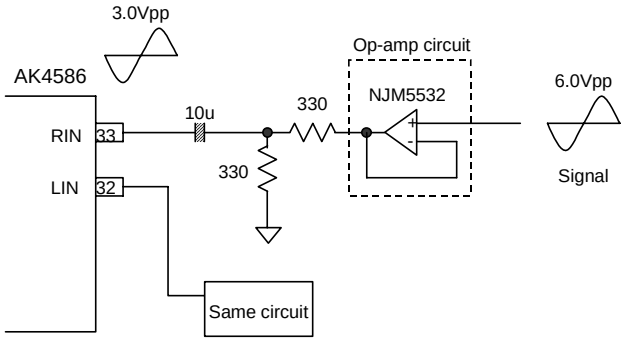


Figure 1. AKD4586 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

■ Consideration for analog input circuit



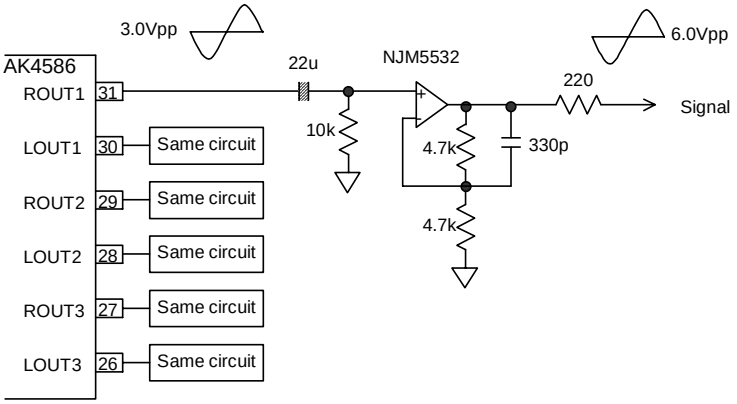
1) Gain

Gain of analog input circuit is
330/(330+330) = -6.02dB.
Therefore input level for this board is
+0.51dBV(=3.0Vpp)+6.02dB
= +6.53dBV = 6.00Vpp = 2.12Vrms.

2) S/N of op-amp circuit (Theory: BW=20k+A)

Non-inverting amp is implemented on board. The output noise level of op-amp circuit is
-126.01dBV = -132.54dB (0dB=+6.53dBV).
S/N of ADC is
101.6dB (measurement).
Therefore total S/N of op-amp circuit and ADC is
101.60dB (measurement: 101.6dB)

■ Consideration for analog output circuit



1) Frequency response of HPF

The HPF is implemented on board to cancel the DC offset of analog output of AK4586.

Frequency response of 1st-order HPF

$|\text{Amplitude}|^2 = 1/\{1+(fc/f)^2\}$; $fc=1/2\pi RC=$**0.7Hz**@R=10k,C=22u

fin	20Hz
Frequency Response	**-0.006dB**

2) Gain, S/N and frequency response of op-amp circuit

1st-order filter with non-inverting amp is implemented on board to double the analog output level and attenuate outband noise.

a) Gain

The gain is

1+4.7k/4.7k = +6.02dB.

Therefore the output level of this board is

0.51dBV(=3.0Vpp) + 6.02dB

= 6.53dBV = 6.00Vpp = 2.12Vrms.

b) S/N (Theory: BW=20k+A)

The output noise level of non-inverting amp

-110.36dBV = -116.89dB (0dB=6.53dBV)

S/N of DAC is

106.3dB (measurement)

Therefore total S/N of op-amp circuit and DAC is

105.90dB (measurement: 105.8dB).

c) Frequency response of filter

Frequency response of the 1st-order filter

$|\text{Amplitude}|^2 = K*\{1+(f/fc_2)^2\}/\{1+(f/fc_1)^2\}$;

$K = 1+4.7k/4.7k = 2$,

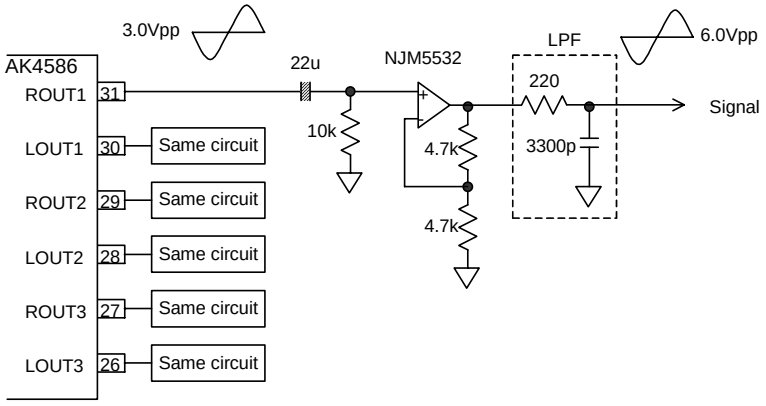
$fc_1 = 1/2\pi RC = 102.7kHz@R=4.7k,C=330p$,

$fc_2 = K*fc_1 = 205.3kHz$

Frequency response referenced to output level of this board is as following table:

fin	DC	20kHz	40kHz	80kHz	145kHz	∞
Frequency Response	0dB	**-0.121dB**	**-0.452dB**	**-1.448dB**	-3dB	-6dB

If the frequency response of filter influences the system, 1st-order LPF is also available as the following figure:



Frequency response of this LPF

$|\text{Amplitude}|^2 = 1/\{1+(f/fc)^2\}$;

$fc = 1/2\pi RC = 219kHz@R=220,C=3300p$

Frequency response referenced to output level of this board is as following table:

fin	DC	20kHz	40kHz	80kHz	219kHz	∞
Frequency Response	0dB	**-0.036dB**	**-0.142dB**	**-0.543dB**	-3dB	-∞dB

The total frequency response of this board is sum of the external filter and internal LPF of AK4586.

These filters are effective to attenuate the high frequency noise since some measurement units is sensitive for out-of-band noise.

■ Digital Inputs

Toslink(TORX176: PORT2) or BNC connector(J10) is used for digital inputs. Using Toslink or BNC connector is selected by (JP2).

■ Digital Outputs

TOTX176(PORT2) is used for ADC output, and BNC connector(J3) is used for through data output.

■ Operation sequence

1) Set up the power supply lines. (See "Other jumpers set-up".)

Name	Color	Voltage	Contents	Contents
+12V	Orange	12~15V	Regulator and Analog interface	
-12V	Blue	-15~-12V	Analog interface	
AGND	Black	0V	Analog ground	AGND jack should be always shorted.
DGND	Black	0V	Digital ground	If JP1 is shorted ,DGND is not needed.

Table 1. Set up of power supply lines

Each supply line should be distributed from the power supply unit

2) Set-up the evaluation modes, jumper pins and DIP switches. (See the followings.)

3) Power on.
The AK4586 should be reset once bringing SW1(PDN) "L" upon power-up.

■ Serial control

The AK4586 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT1(uP-I/F) with PC by 10-line flat cable packed with the AKD4586.

Take care of the direction of connector. There is a mark at pin#1.
The pin layout of PORT1 is as Figure 2.

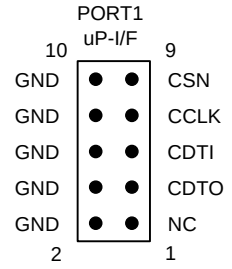


Figure 2 PORT1 pin layout

■ Evaluation mode

Applicable evaluation modes

(1) Loopback mode
(2) Evaluation of A/D
(3) Evaluation of D/A<default>
(4) Evaluation using AC3 Decoder

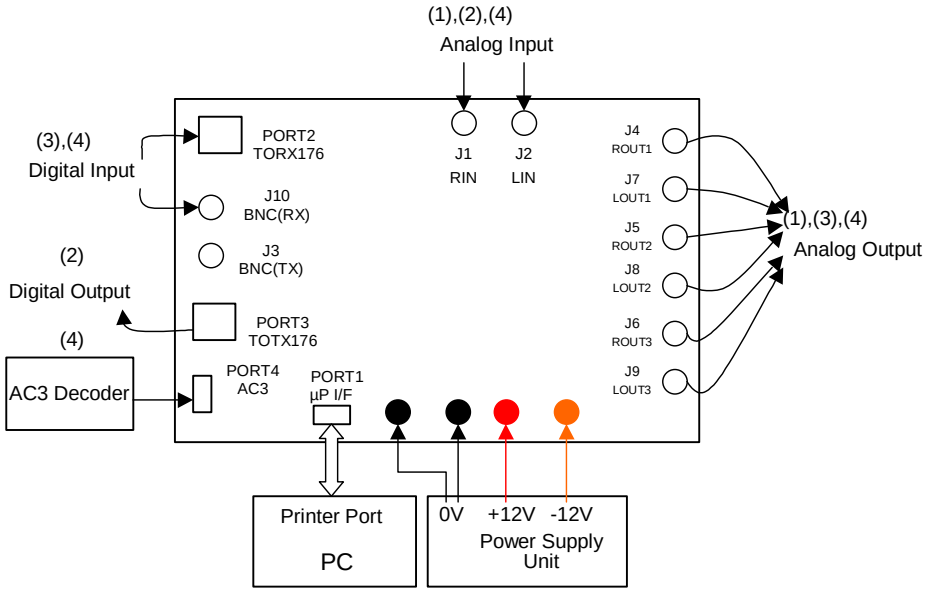


Figure 3. Connection diagram for each evaluation mode

(1) Loopback mode

MCLK, BICK and LRCK are fed from AK4586. JP26(SDTI1), JP27(SDTI2) and JP28(SDTI3) should be shorted.

JP26(SDTI1) shorted → Loopback outputs to ROUT1, LOUT1
JP27(SDTI2) shorted → Loopback outputs to ROUT2, LOUT2
JP28(SDTI3) shorted → Loopback outputs to ROUT3, LOUT3

Nothing should be connected to PORT4(AC3). Clock operation mode of the AK4586 should be set to X'tal mode by the control software packed with the AKD4586. Clock operation mode is set by CM1-0 bit of Addr=02H.

(2) Evaluation of ADC

PORT2(TOTX176) is used for digital output. AK4103(DIT) generates audio bi-phase signal from received data and which is output through optical connector (TOTX176). It is possible to connect AKM's D/A converter evaluation boards or the digital-amplifier which equips DIR input. SW2 is used to set the interface format and clock mode of AK4103 (see DIP-SW set-up). Clock operation mode of the AK4586 should be set to X'tal mode by the control software packed with the AKD4586. Clock operation mode is set by CM1-0 bit of Addr=02H.

(3) Evaluation of DAC<default>

PORT2(TORX176) or J10(BNC(RX)) is used for digital input. DIR of AK4586 generates MCLK, BICK, LRCK and SDATA from the received data through optical connector(TORX176) or BNC connector. Used for the evaluation using CD test disk. In case of using BNC connector, set JP2(RX) to "BNC" side. Nothing should be connected to PORT4(AC3).

(4) Evaluation using AC3 decoder

Connect the AC3 decoder with PORT4(AC3). Decoded serial data is sent to AKD4586. JP26(SDTI1), JP27(SDTI2) and JP27(SDTI3) should be open.

■ Clock operation mode set-up

Clock operation mode should be set as Table 2 at evaluation modes (1), (2) and (3). Both clock operation mode can be used at other evaluation modes. Clock operation mode can be set by CM1-0 bits(Addr=02H) of AK4586. CM1-0 bits can be set by the software packed with AKD4586. Please refer to the datasheet of AK4586 for details.

Clock operation mode	Corresponding eva-mode	
PLL mode	(3)	Default
X'tal mode	(1),(2)	

Table 2. Clock operation mode set-up

■ Jumpers set up

[JP1](GND): Analog ground and digital ground.
This jumper pin should always be shorted.

[JP2] (RX):Source of digital inputs.
RX side: Toslink(TORX176: PORT2) <default>
BNC side: BNC connector(JP10)

[JP26] (SDTI1):Source of SDTI1 input
Short: SDTO of AKD4586 <default>
Open: PORT4

[JP27] (SDTI2): Source of SDTI2 input
Short: SDTO of AKD4586 <default>
Open: PORT4

[JP28] (SDTI3): Source of SDTI3 input
Short: SDTO of AKD4586 <default>
Open: PORT4

■ DIP-SW set-up(Setup of interface format and clock mode of AK4103)

[SW1]: No.4-8 set the mode of AK4586 and No.6-10 set the mode of AK4103.

Pin No.	Name	Contents
1	Reserve	Always OFF
2	Reserve	
3	Reserve	
4	DIF2	AK4103 interface format(see Table 4) (Default: No.4=ON, No.5,6=OFF: 24bit MSB justified)
5	DIF1	
6	DIF0	
7	CKS1	AK4103 clock mode(see Table 5) (Default: No.7,8=OFF: 256fs)
8	CKS0	

Table 3. SW1 set-up
(Note: No.8 is "0" at ON, others are "1" at ON.)

Mode	Format	No.4	No.5	No.6	
		DIF2	DIF1	DIF0	
0	16bit, LSB justified	0	0	0	
1	18bit, LSB justified	0	0	1	
2	20bit, LSB justified	0	1	0	
3	24bit, LSB justified	0	1	1	
4	24bit, MSB justified	1	0	0	Default
5	I^2S	1	0	1	
6	24bit, MSB justified (Master)	1	1	0	
7	I^2S(Master)	1	1	1	

Table 4. AK4103 interface format set-up (1=ON, 0=OFF)

Clock mode	No.7	No.8	
	CKS1	CKS0	
128fs	OFF	ON	
256fs	OFF	OFF	Default
384fs	ON	ON	
512fs	ON	OFF	

Table 5. AK4103 clock mode set-up

■ The indication content for LED

LED turns on when each output goes “H”.

[LE1] (DZF1): DZF1 of AK4586
[LE2] (DZF2/OVF): DZF2/OVF of AK4586
[LE3] (INT0): INT0 of AK4586
[LE4] (INT1): INT1 of AK4586

■ Interface with AC3 decoder

PORT3(AC3) is used for interface with AC3 decoder.
3-line serial data can be input from the decoder via PORT6.
Pin layout of PORT4 is as Figure 4.

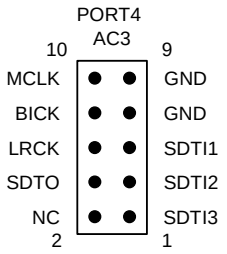


Figure 4. PORT4 pin layout

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4586 according to previous term.

2. Connect IBM-AT compatible PC with AKD4586 by 10-line type flat cable (packed with AKD4586). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AKD4586 Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of "akd4586.exe" to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.

■ Explanation of each buttons

1. [Port Reset] : Set up the USB interface board (AKDUSBIF-A) .
2. [Write default] : Initialize the register of AK4586.
3. [All Write] : Write all registers that is currently displayed.
4. [Function1] : Dialog to write data by keyboard operation.
5. [Function2] : Dialog to write data by keyboard operation.
6. [Function3] : The sequence of register setting can be set and executed.
7. [Function4] : The sequence that is created on [Function3] can be assigned to buttons and executed.
8. [Function5]: The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
9. [SAVE] : Save the current register setting.
10. [OPEN] : Write the saved values to all register.
11. [Write] : Dialog to write data by mouse operation.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

If you want to write the input data to AK4586, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog] : Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to AK4586, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog] : Dialog to evaluate ATT

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to AK4642 by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to AK4586, click [OK] button. If not, click [Cancel] button.

4. [Save] and [Open]

4-1. [Save]

Save the current register setting data. The extension of file name is “akr”.

(Operation flow)
(1) Click [Save] Button.
(2) Set the file name and push [Save] Button. The extension of file name is “akr”.

4-2. [Open]

The register setting data saved by [Save] is written to AK4586. The file type is the same as [Save].

(Operation flow)
(1) Click [Open] Button.
(2) Select the file (*.akr) and Click [Open] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

(2) Set the control sequence.
Set the address, Data and Interval time. Set “-1” to the address of the step where the sequence should be paused.

(3) Click [Start] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [Save] and [Open] button on the Function3 window. The extension of file name is “aks”.

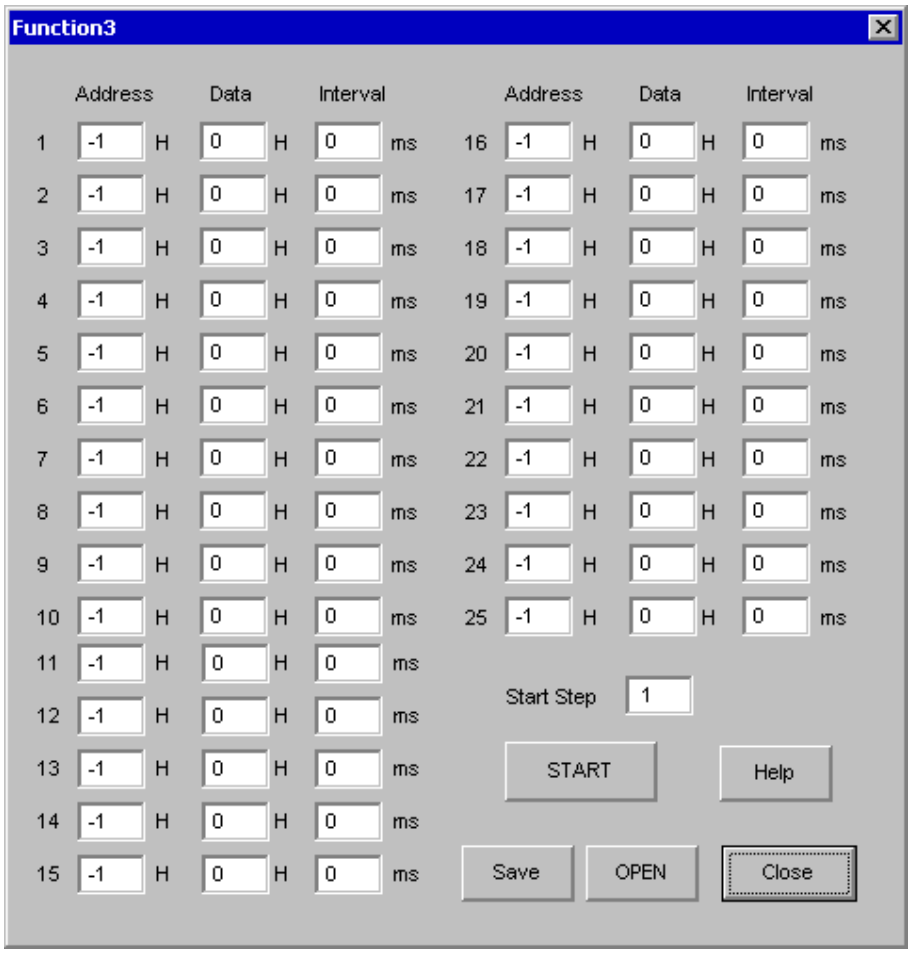


Figure 2. Window of [F3]

6. [Function4 Dialog]

The sequence that is created on [Function3] can be assigned to buttons and executed. When [F4] button is clicked, the window as shown in Figure 3 opens.

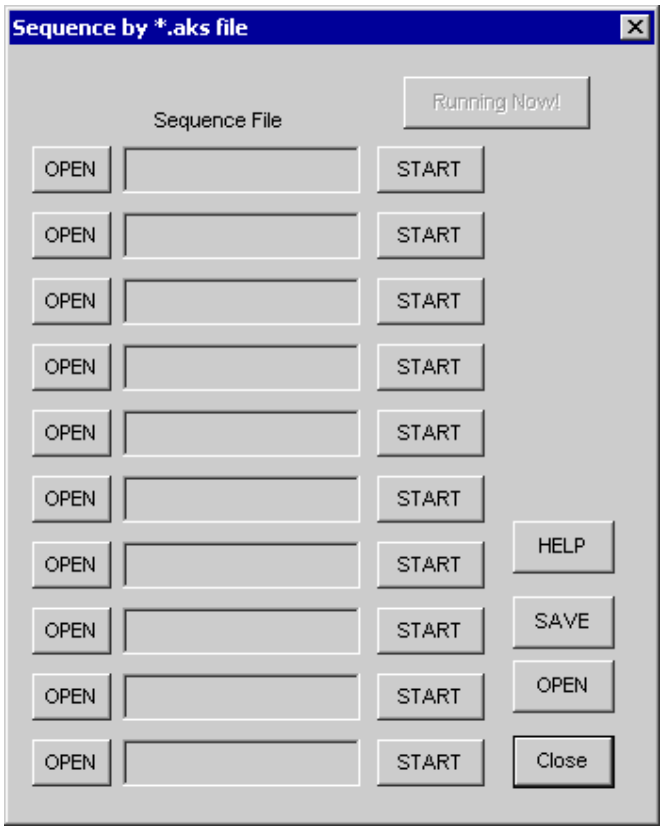


Figure 3. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks).

The sequence file name is displayed as shown in Figure 4.

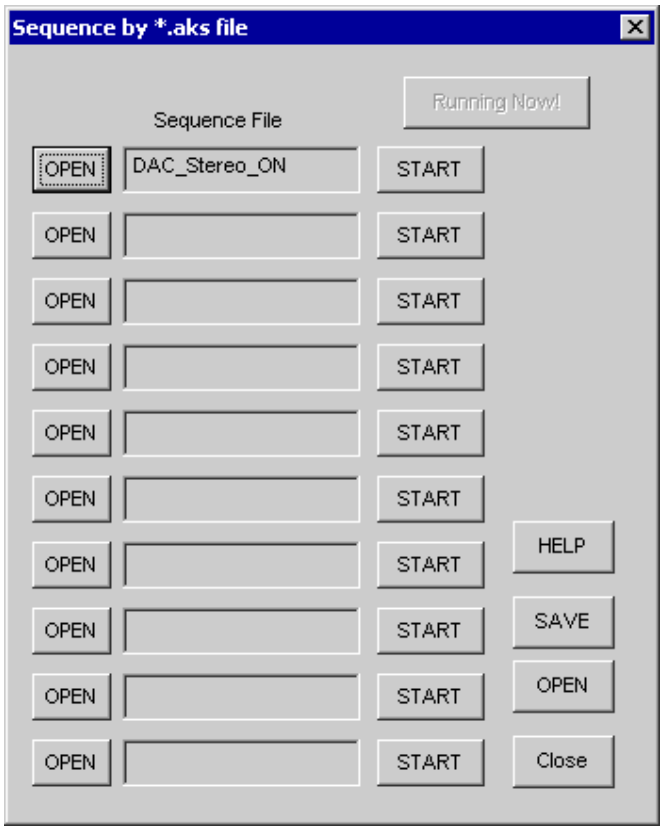


Figure 4. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

3-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The sequence file names can assign be saved. The file name is *.ak4.

[OPEN] : The sequence file names assign that are saved in *.ak4 are loaded.

3-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(3) When the sequence is changed in [Function3], the file should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed. When [F5] button is clicked, the following window as shown in Figure 5opens.

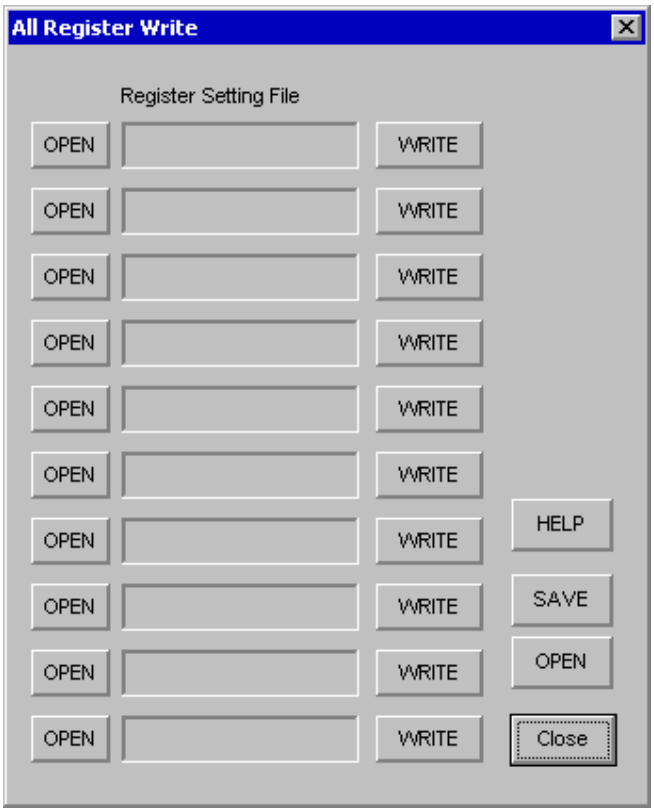


Figure 5. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

(2) Click [WRITE] button, then the register setting is executed.

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The register setting file names assign can be saved. The file name is *.ak5.

[OPEN] : The register setting file names assign that are saved in *.ak5 are loaded.

7-3. Note

(1) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(2) When the register setting is changed by [Save] Button in main window, the file should be loaded again in order to reflect the change.

MEASUREMENT RESULTS

1) ADC part

[Measurement condition]

- Measurement unit : Audio Precision System two Cascade
- MCLK : 256fs
- BICK : 64fs
- fs : 48kHz, 96kHz
- BW : 10Hz~20kHz (fs=48kHz), 10Hz~48kHz (fs=96kHz)
- Bit : 24bit
- Power Supply : AVDD=PVDD=DVDD=TVDD=5V
- Interface : DIT
- Temperature : Room

fs=48kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, -0.5dB	20kLPF	95.6 dB
DR	1kHz, -60dB	20kLPF, A-weighted	101.4 dB
S/N	No signal	20kLPF, A-weighted	101.6 dB

fs=96kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, -0.5dB	fs/2	92.5 dB
DR	1kHz, -60dB	fs/2, A-weighted	103.4 dB
S/N	No signal	fs/2, A-weighted	103.4 dB

2) DAC part

[Measurement condition]

- Measurement unit : Audio Precision System two Cascade
- MCLK : 256fs
- BICK : 64fs
- fs : 48kHz, 96kHz
- BW : 10Hz~20kHz (fs=48kHz), 10Hz~40kHz (fs=96kHz)
- Bit : 24bit
- Power Supply : AVDD=PVDD=DVDD=TVDD=5V
- Interface : DIR
- Temperature : Room

fs=48kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, 0dB	20kLPF	97.3 dB
DR	1kHz, -60dB	22kLPF, A-weighted	105.3 dB
S/N	“0” data	22kLPF, A-weighted	105.8 dB

fs=96kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, 0dB	40kLPF	95.5 dB
DR	1kHz, -60dB	22kLPF, A-weighted	105.5 dB
S/N	“0” data	22kLPF, A-weighted	105.8 dB

■ Plots

(1) ADC part

[Measurement condition]

- Measurement unit : Audio Precision, System two, Cascade
- MCLK : 256fs
- BICK : 64fs
- fs : 48kHz, 96kHz
- BW : 10Hz~20kHz (fs=48kHz), 10Hz~48kHz (fs=96kHz)
- Bit : 24bit
- Power Supply : AVDD=DVDD=TVDD=PVDD=5V
- Interface : DIT
- Temperature : Room

fs=48kHz

Figure 1-1. FFT (1kHz, -0.5dBFS input)
Figure 1-2. FFT (1kHz, -60dBFS input)
Figure 1-3. FFT (Noise floor)
Figure 1-4. THD+N vs Input Level (fin=1kHz)
Figure 1-5. THD+N vs fin (Input Level=-0.5dBFS)
Figure 1-6. Linearity (fin=1kHz)
Figure 1-7. Frequency Response (Input Level=-0.5dBFS)
Figure 1-8. Crosstalk (Input Level=-0.5dBFS)

fs=96kHz

Figure 2-1. FFT (1kHz, -0.5dBFS input)
Figure 2-2. FFT (1kHz, -60dBFS input)
Figure 2-3. FFT (Noise floor)
Figure 2-4. THD+N vs Input Level (fin=1kHz)
Figure 2-5. THD+N vs fin (Input Level=-0.5dBFS)
Figure 2-6. Linearity (fin=1kHz)
Figure 2-7. Frequency Response (Input Level=-0.5dBFS)
Figure 2-8. Crosstalk (Input Level=-0.5dBFS)

(ADC, fs=48kHz)

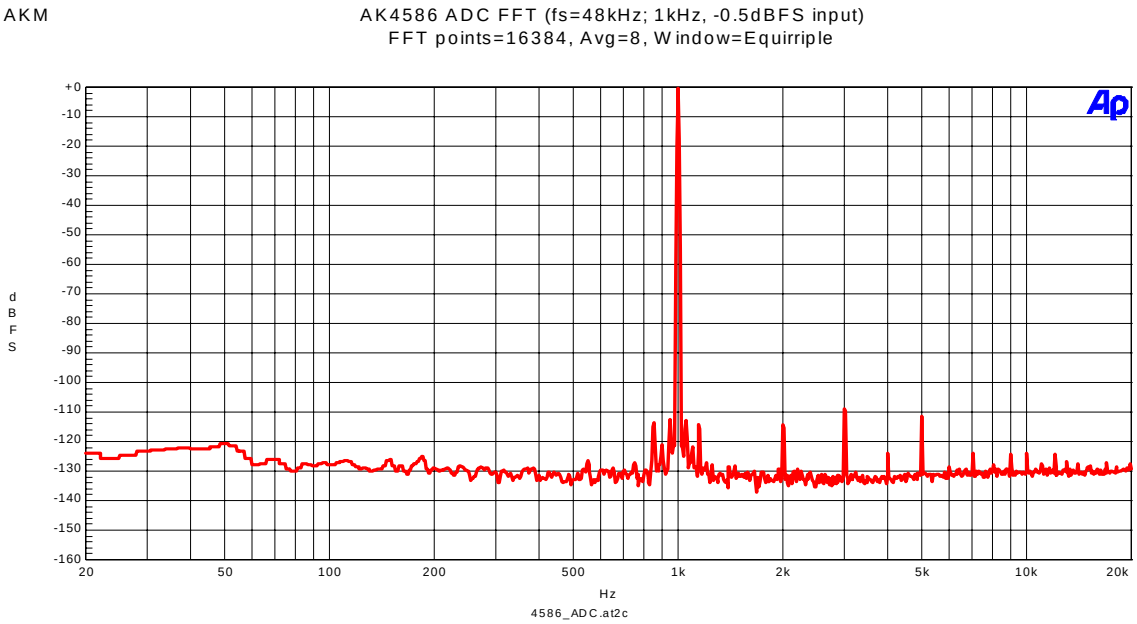


Figure 1-1. FFT (1kHz, -0.5dBFS input)
FFT points=16384, Avg=8, Window=Equiripple

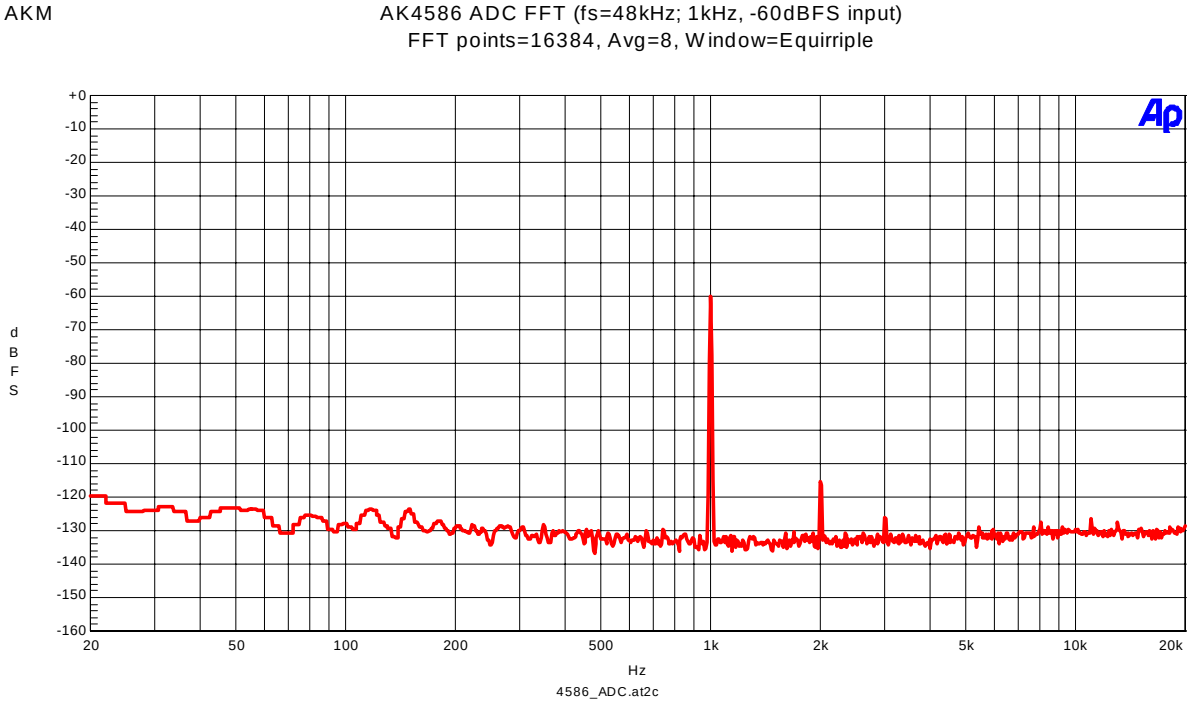


Figure 1-2. FFT (1kHz, -60dBFS input)
FFT points=16384, Avg=8, Window=Equiripple

(ADC, fs=48kHz)

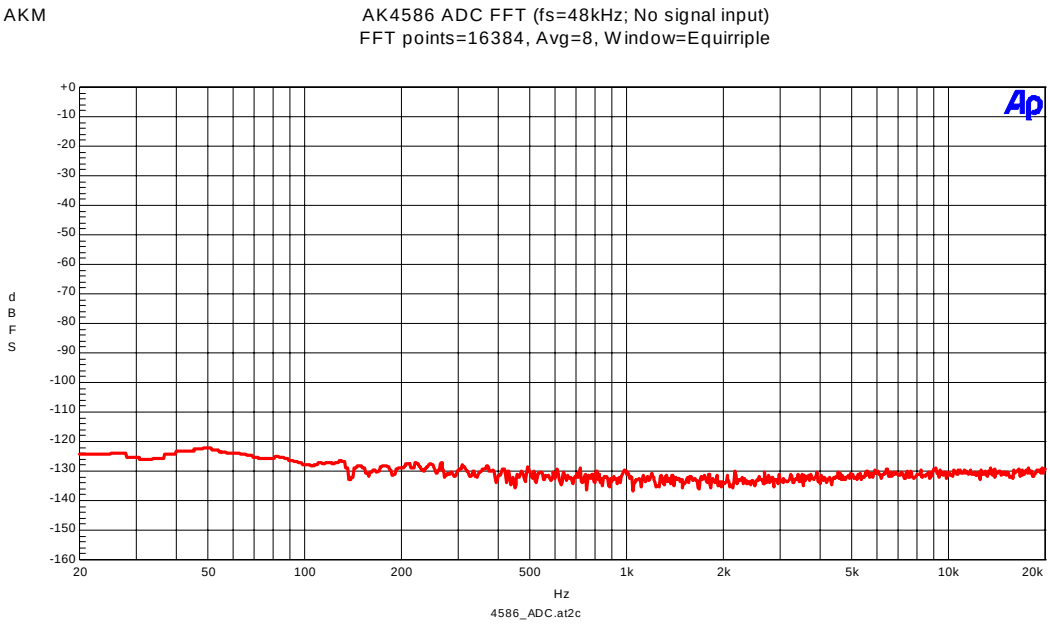


Figure 1-3. FFT (Noise floor)
FFT points=16384, Avg=8, Window=Equiripple

(ADC, fs=48kHz)

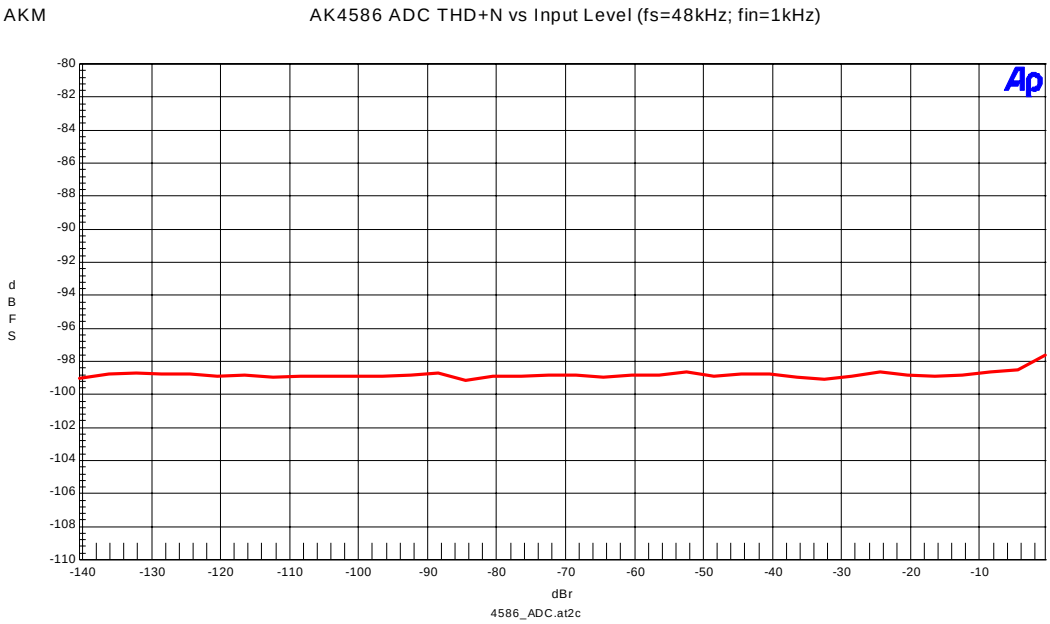


Figure 1-4. THD+N vs Input Level (fin=1kHz)

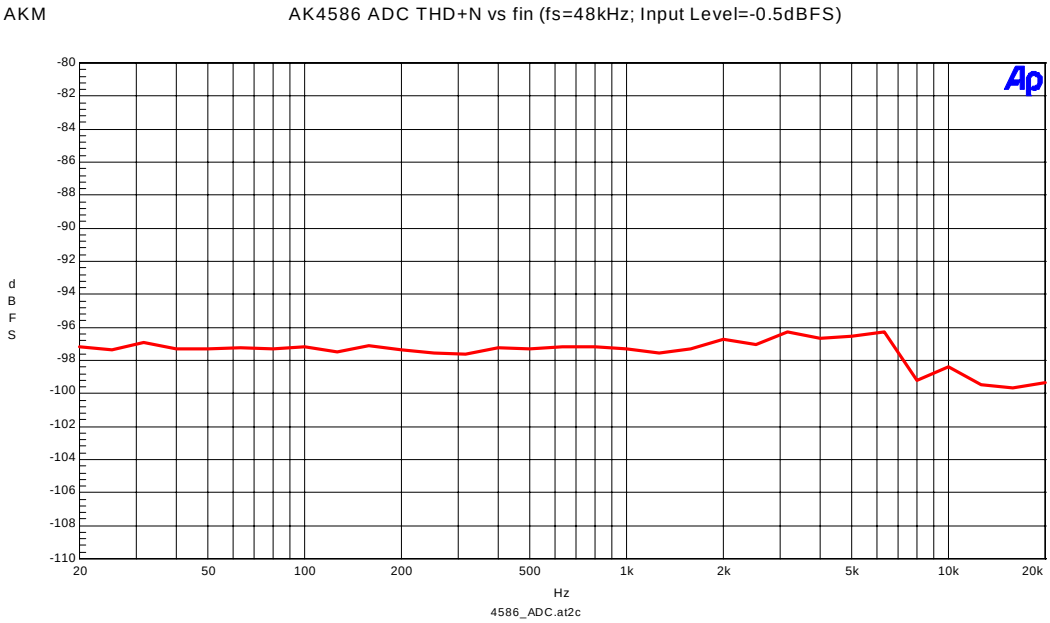


Figure 1-5. THD+N vs fin (Input Level=-0.5dBFS)

(ADC, fs=48kHz)

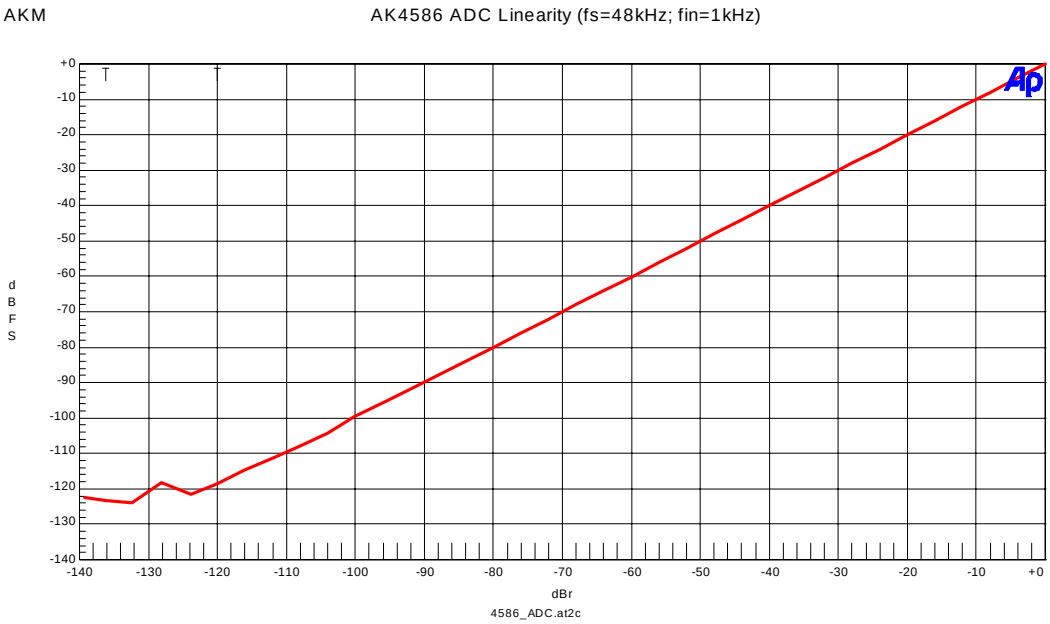


Figure 1-6. Linearity (fin=1kHz)

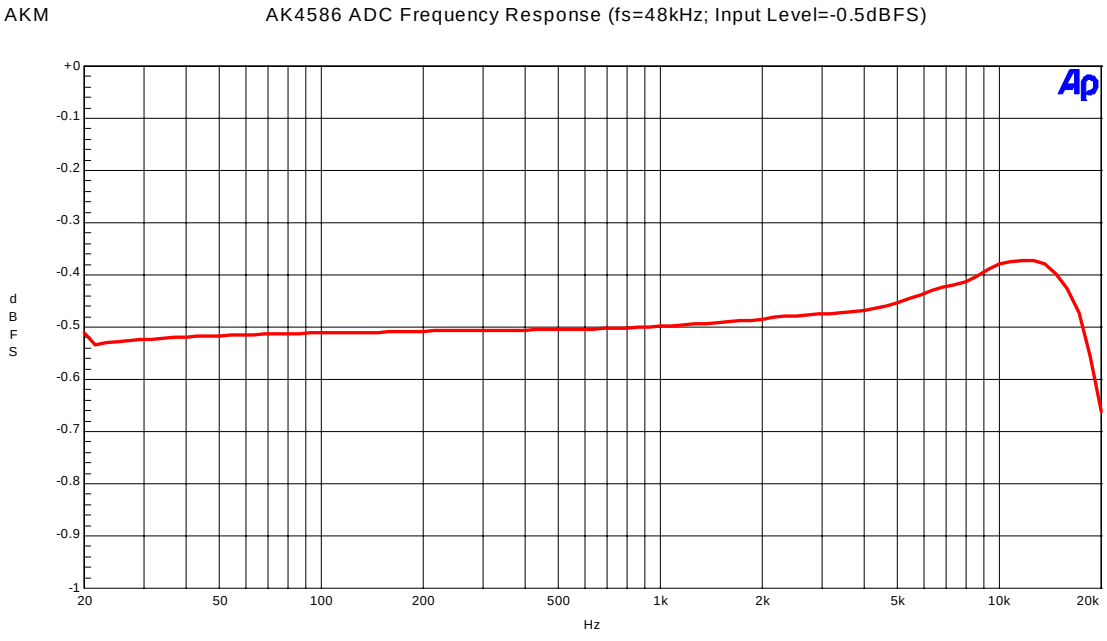


Figure 1-7. Frequency Response (Input Level=-0.5dBFS)

(ADC, fs=48kHz)

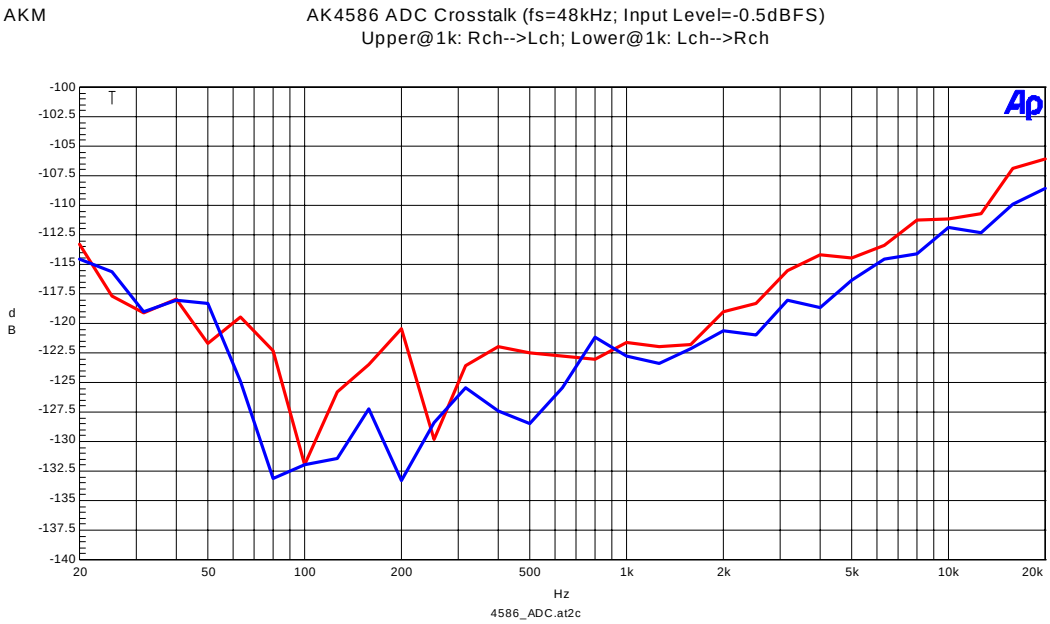


Figure 1-8. Crosstalk (Input Level=-0.5dBFS)

(ADC, fs=96kHz)

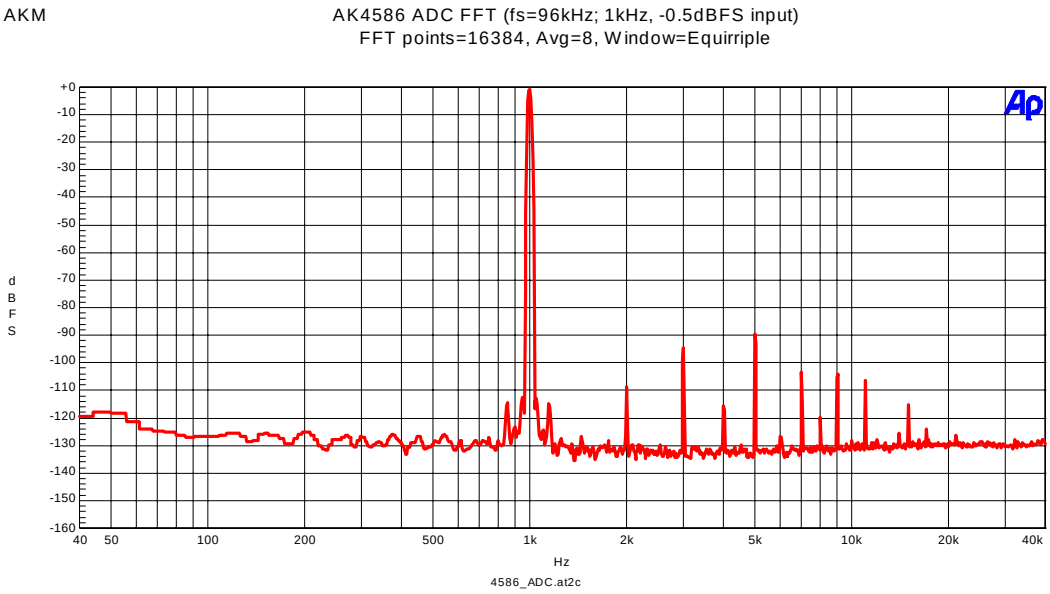


Figure 2-1. FFT (1kHz, -0.5dBFS input)
FFT points=16384, Avg=8, Window=Equiripple

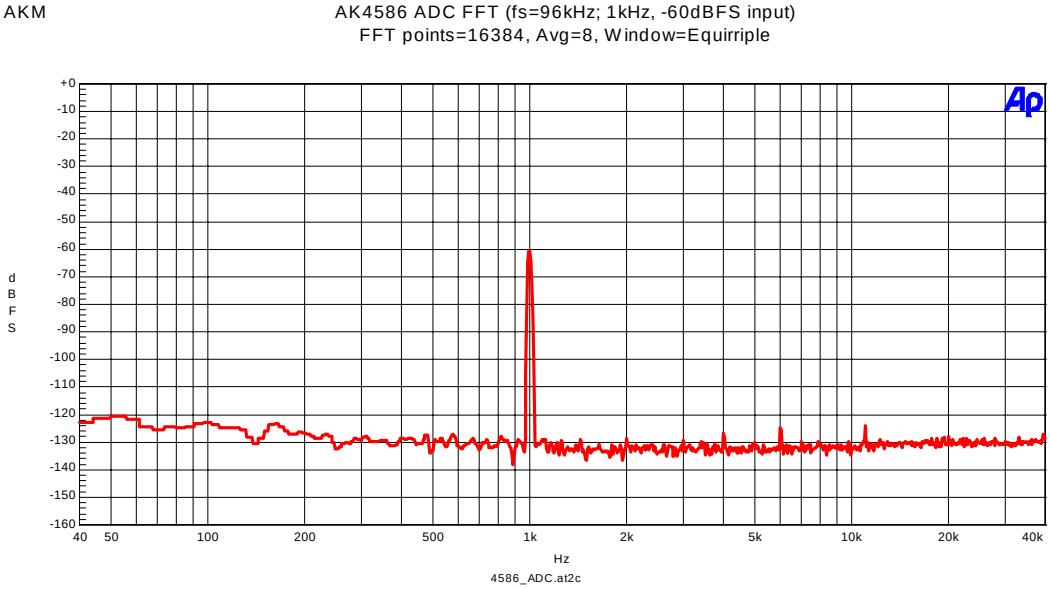


Figure 2-2. FFT (1kHz, -60dBFS input)
FFT points=16384, Avg=8, Window=Equiripple

(ADC, fs=96kHz)

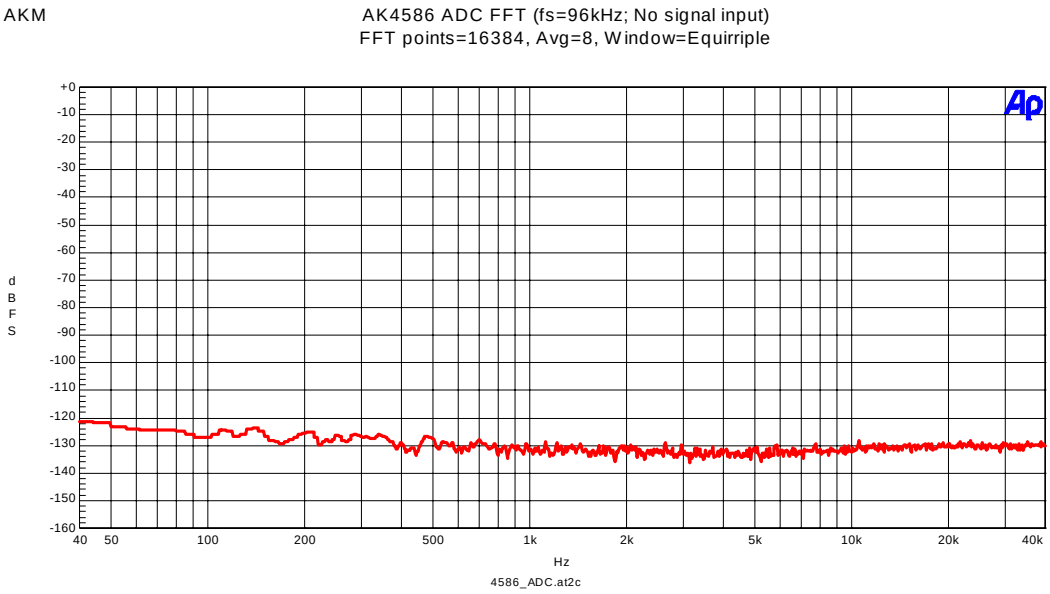


Figure 2-3. FFT (Noise floor)
FFT points=16384, Avg=8, Window=Equiripple

(ADC, fs=96kHz)

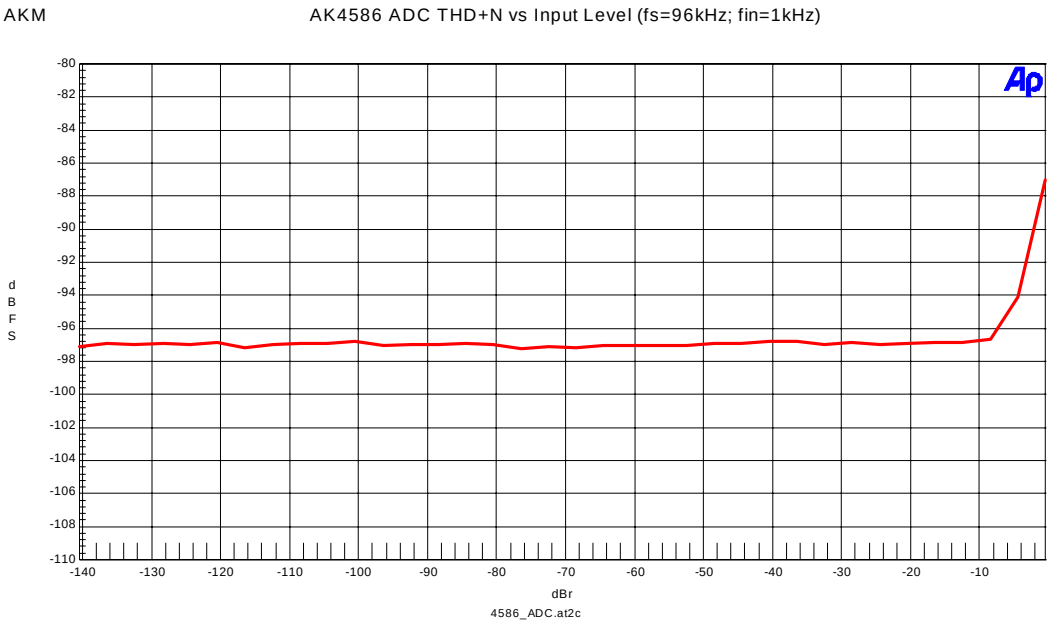


Figure 2-4. THD+N vs Input Level (fin=1kHz)

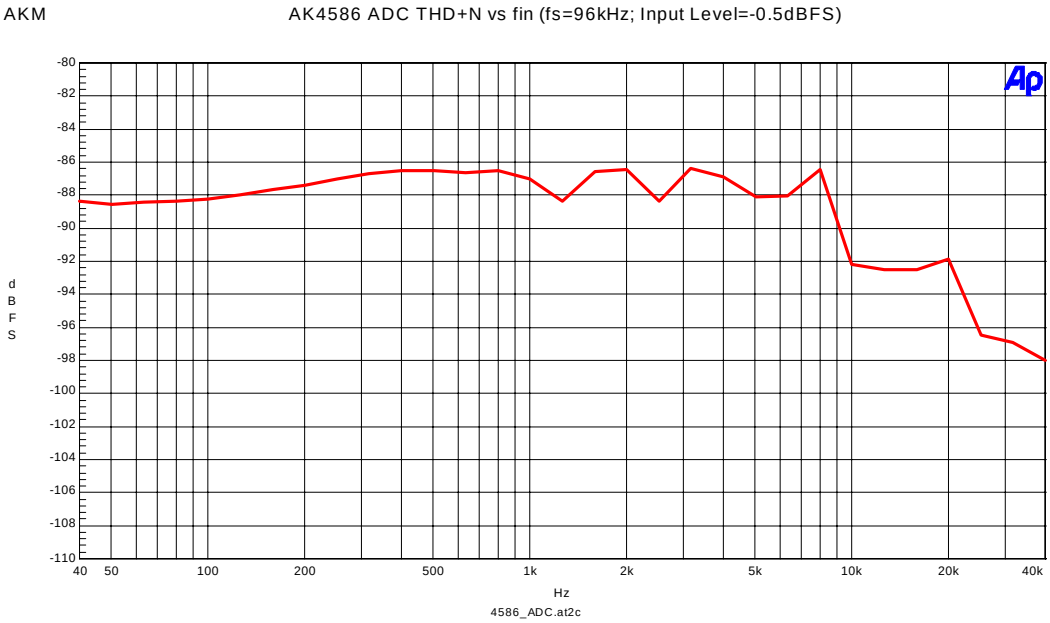


Figure 2-5. THD+N vs fin (Single-ended input, Input Level=-0.5dBFS)

(ADC, fs=96kHz)

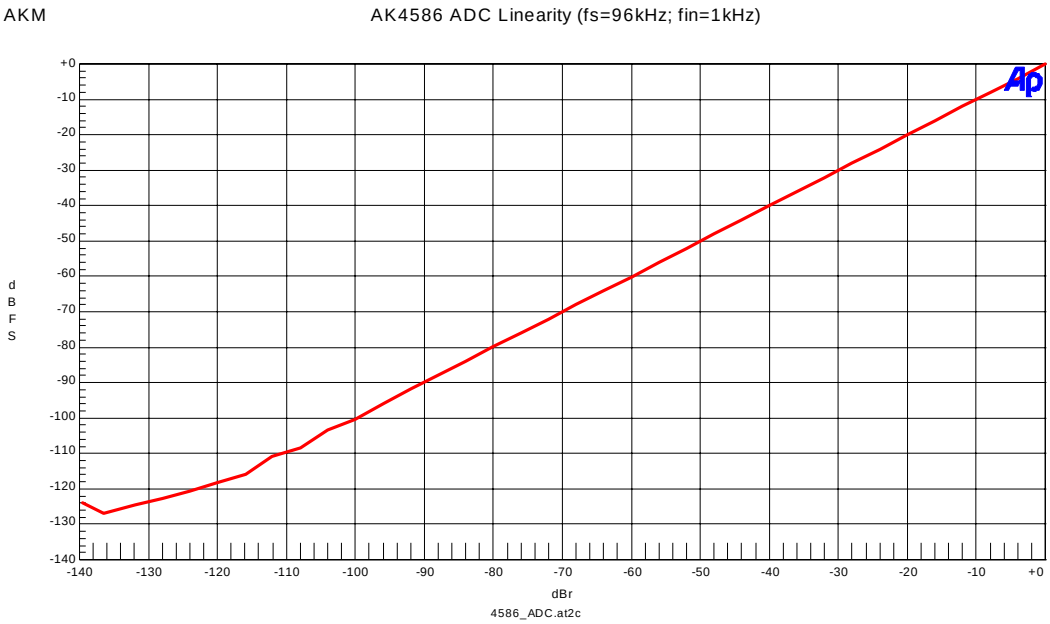


Figure 2-6. Linearity (fin=1kHz)

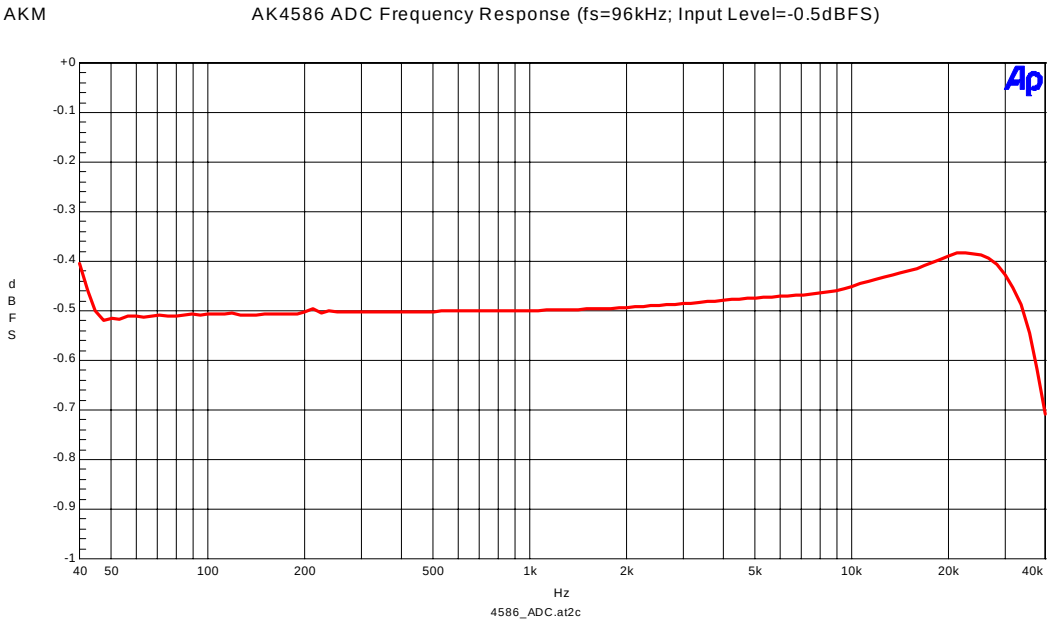


Figure 2-7. Frequency Response (Input Level=-0.5dBFS)
(Including Internal RC filter: fc=424kHz)

(ADC, fs=96kHz)

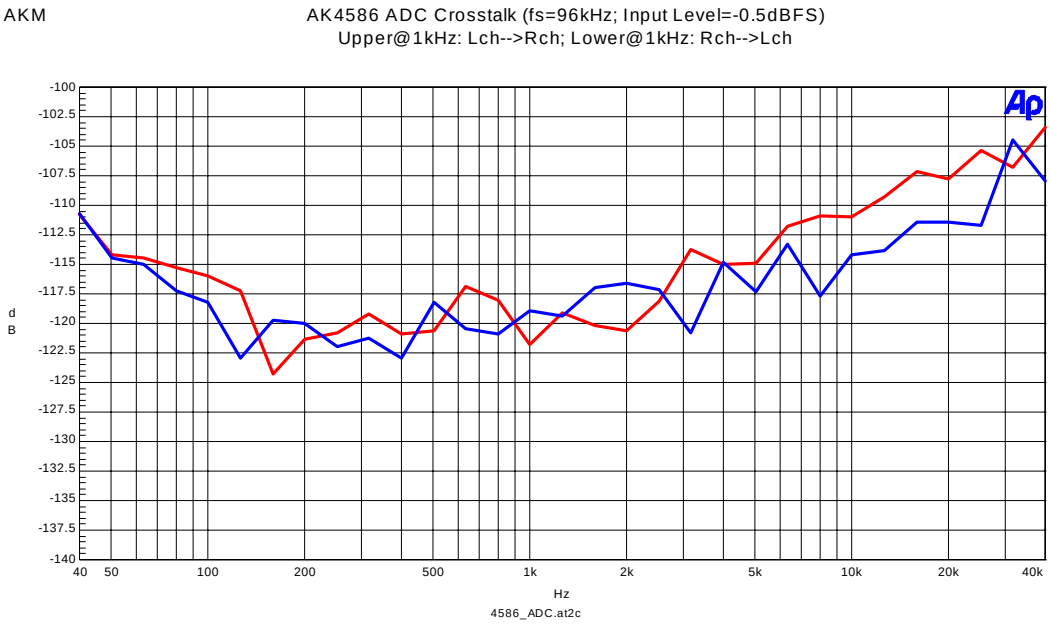


Figure 2-8. Crosstalk (Input Level=-0.5dBFS)

(2) DAC part

[Measurement condition]
- Measurement unit : Audio Precision, System two, Cascade
- MCLK : 256fs
- BICK : 64fs
- fs : 48kHz, 96kHz
- BW : 10Hz~20kHz (fs=48kHz), 10Hz~40kHz (fs=96kHz)
- Bit : 24bit
- Power Supply : AVDD=DVDD=TVDD=PVDD=5V
- Interface : DIR
- Temperature : Room

fs=48kHz

Figure 3-1. FFT (1kHz, 0dBFS input)
Figure 3-2. FFT (1kHz, -60dBFS input)
Figure 3-3. FFT (Noise floor)
Figure 3-4. FFT (Outband noise)
Figure 3-5. THD+N vs Input Level (fin=1kHz)
Figure 3-6. THD+N vs fin (Input Level=0dBFS)
Figure 3-7. Linearity (fin=1kHz)
Figure 3-8. Frequency Response (Input Level=0dBFS)
Figure 3-9. Crosstalk (Input Level=0dBFS)

fs=96kHz

Figure 4-1. FFT (1kHz, 0dBFS input; Notch=OFF)
Figure 4-2. FFT (1kHz, 0dBFS input; Notch=ON)
Figure 4-3. FFT (1kHz, -60dBFS input)
Figure 4-4. FFT (Noise floor)
Figure 4-5. FFT (Outband noise)
Figure 4-6. THD+N vs Input Level (fin=1kHz)
Figure 4-7. THD+N vs fin (Input Level=0dBFS)
Figure 4-8. Linearity (fin=1kHz)
Figure 4-9. Frequency Response (Input Level=0dBFS)
Figure 4-10. Crosstalk (Input Level=0dBFS)

(DAC, fs=48kHz)

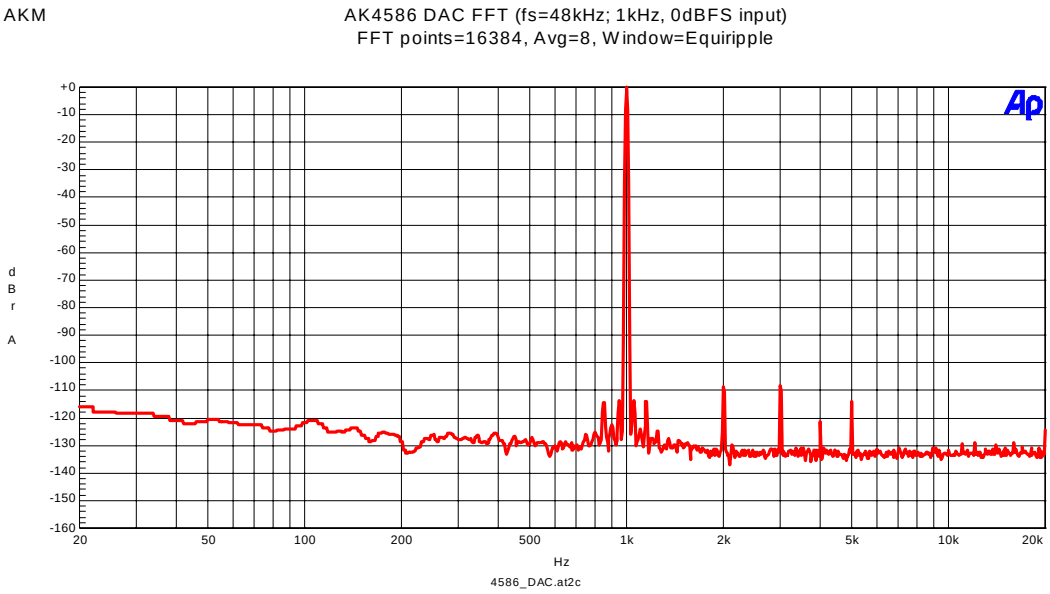


Figure 3-1. FFT (1kHz, 0dBFS input)
FFT points=16384, Avg=8, Window=Equiripple

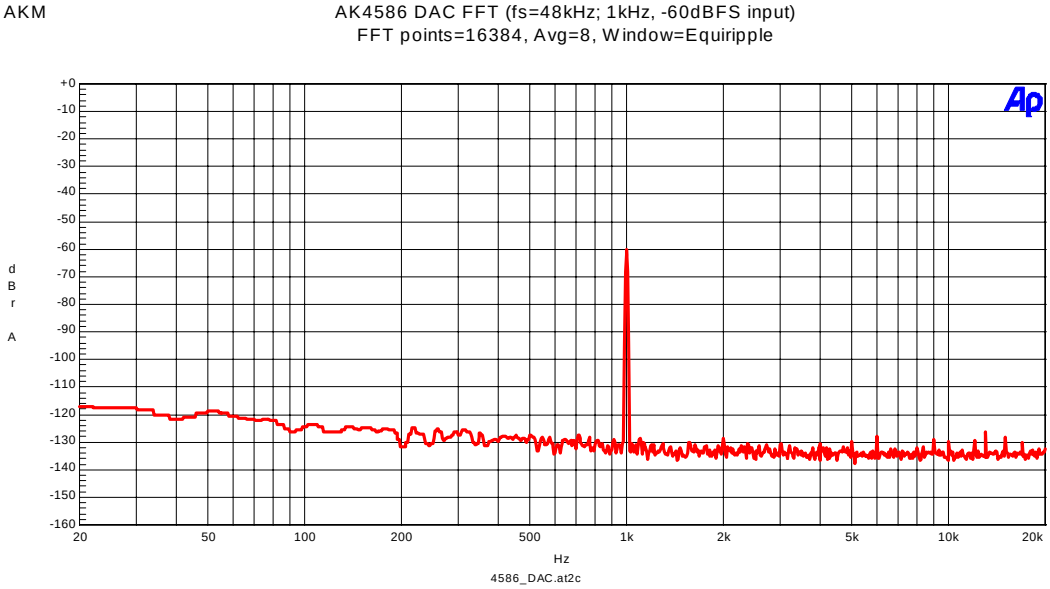


Figure 3-2. FFT (1kHz, -60dBFS input)
FFT points=16384, Avg=8, Window=Equiripple

(DAC, fs=48kHz)

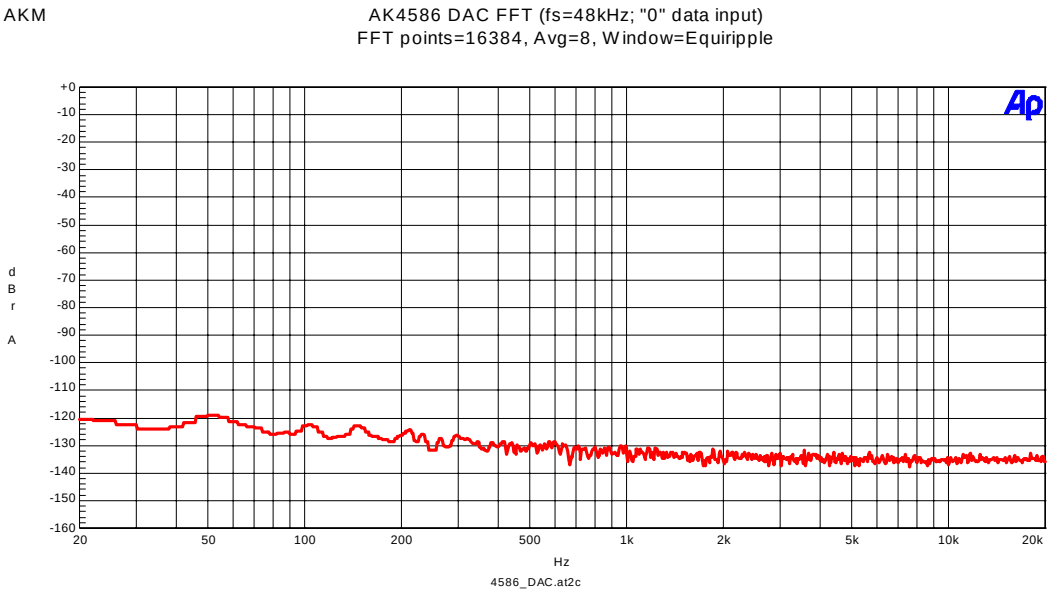


Figure 3-3. FFT (Noise floor)
FFT points=16384, Avg=8, Window=Equiripple

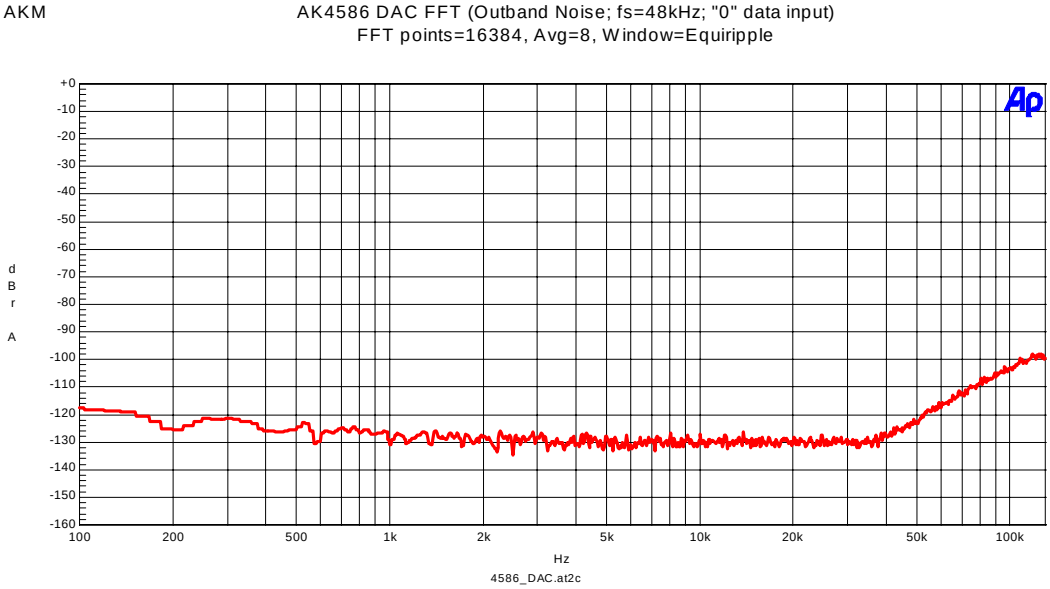


Figure 3-4. FFT (Outband noise)
FFT points=16384, Avg=8, Window=Equiripple

(DAC, fs=48kHz)

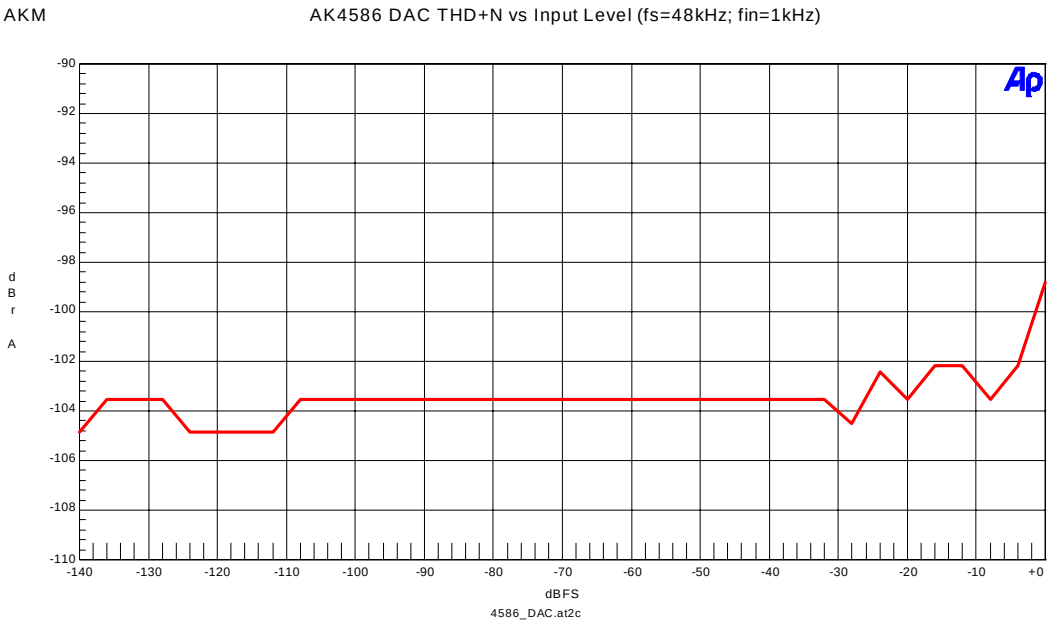


Figure 3-5. THD+N vs Input Level (fin=1kHz)

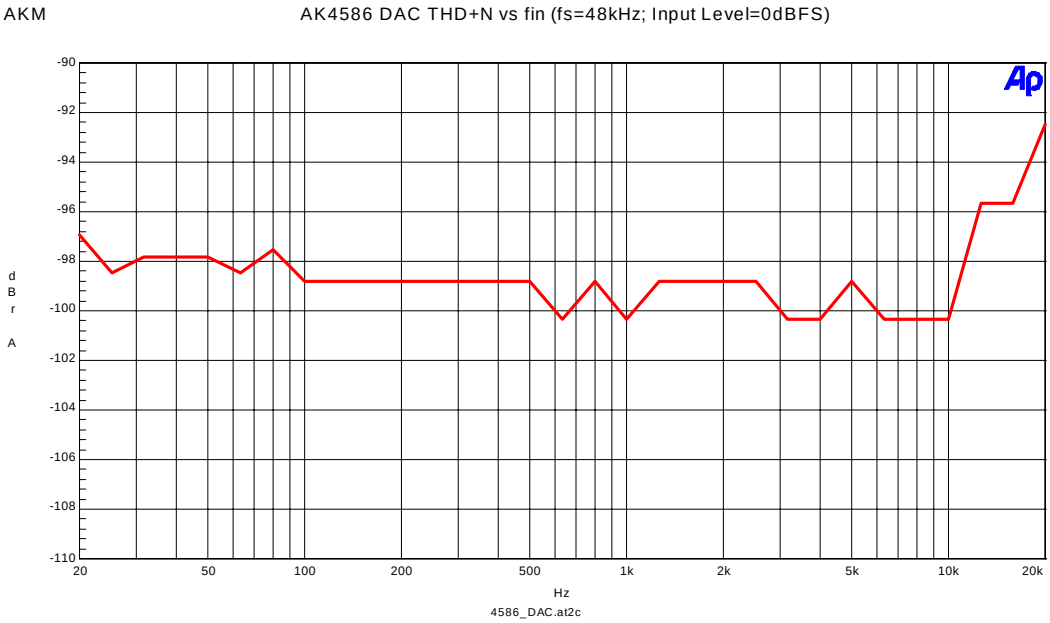


Figure 3-6. THD+N vs fin (Input Level=0dBFS)

(DAC, fs=48kHz)

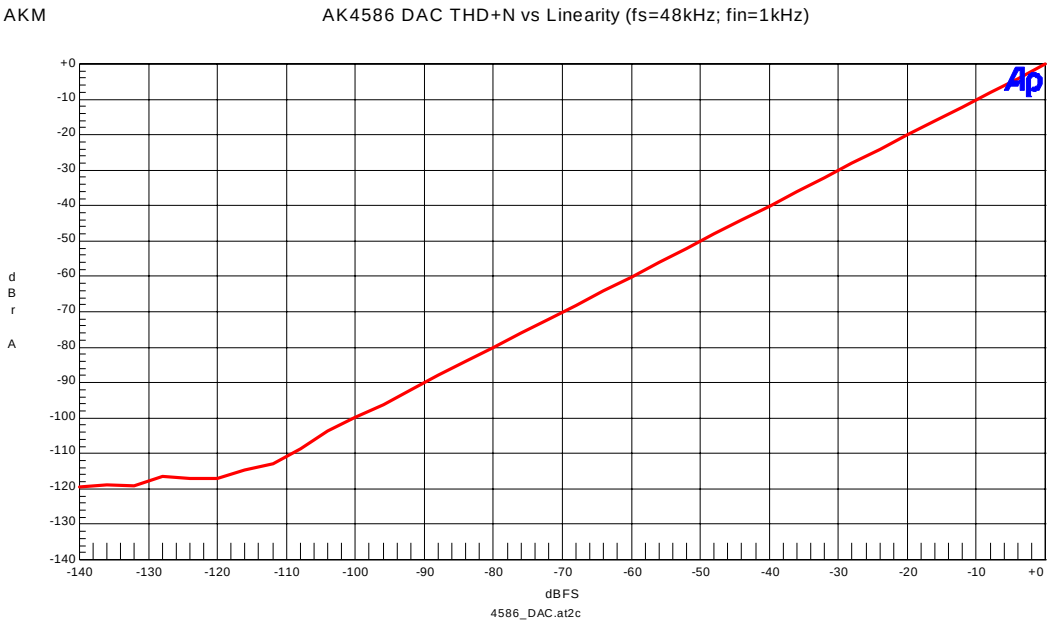


Figure 3-7. Linearity (fin=1kHz)

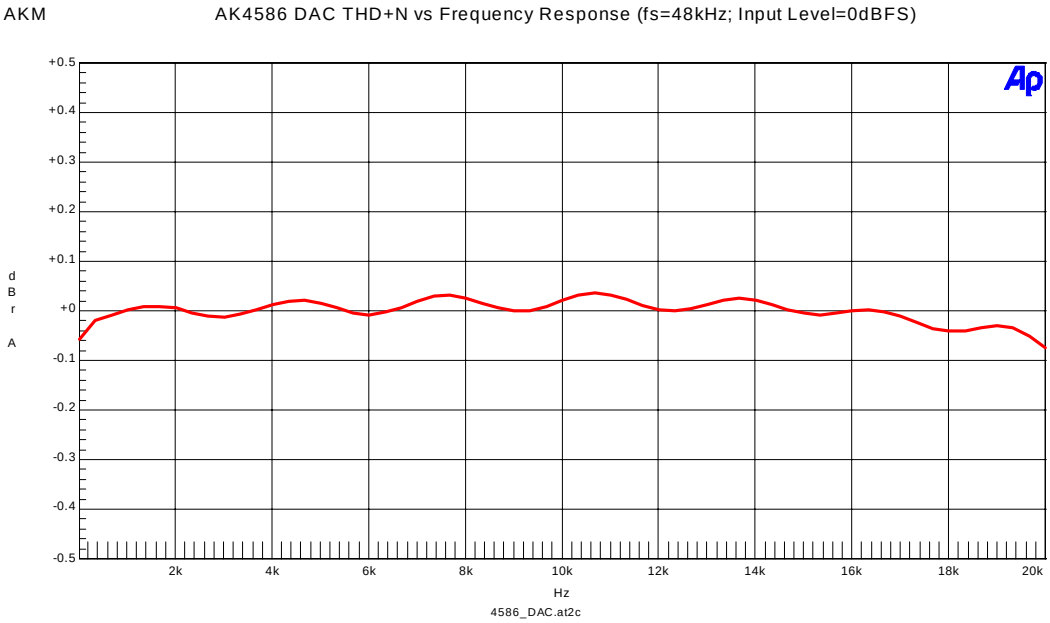


Figure 3-8. Frequency Response (Input Level=0dBFS)

(DAC, fs=48kHz)

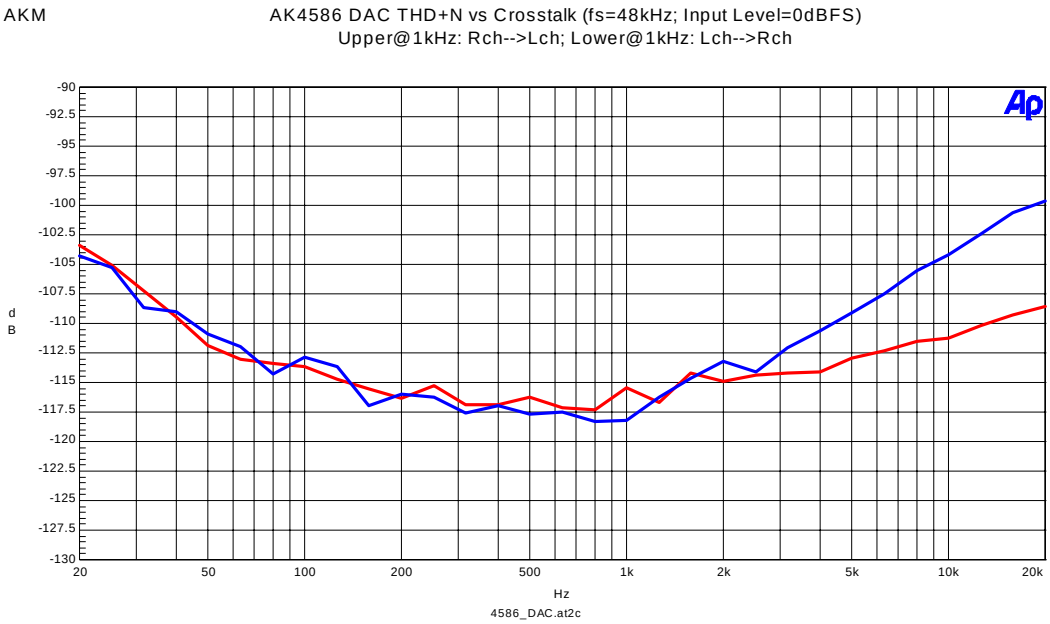


Figure 3-9. Crosstalk (Input Level=0dBFS)

(DAC, fs=96kHz)

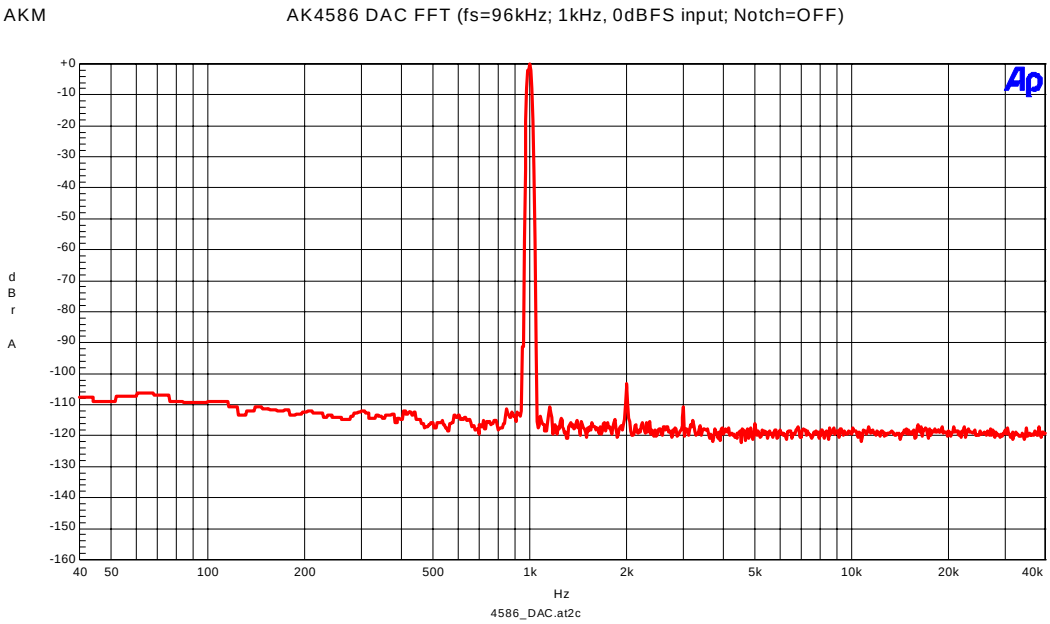


Figure 4-1. FFT (1kHz, 0dBFS input; Notch=OFF)
FFT points=16384, Avg=8, Window=Equiripple

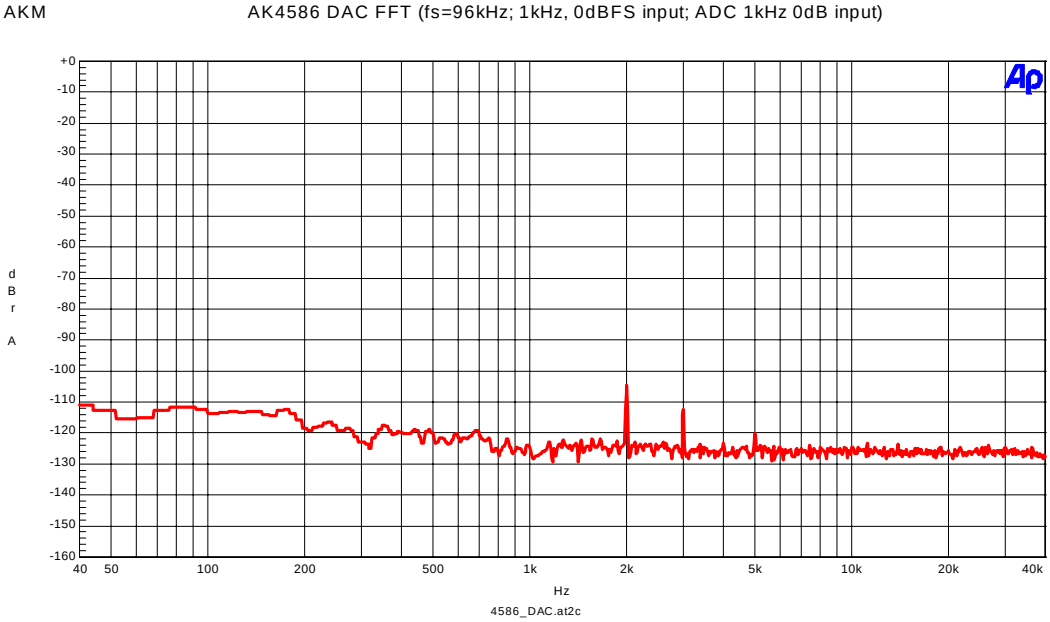


Figure 4-2. FFT (1kHz, 0dBFS input; Notch=ON)
FFT points=16384, Avg=8, Window=Equiripple

(DAC, fs=96kHz)

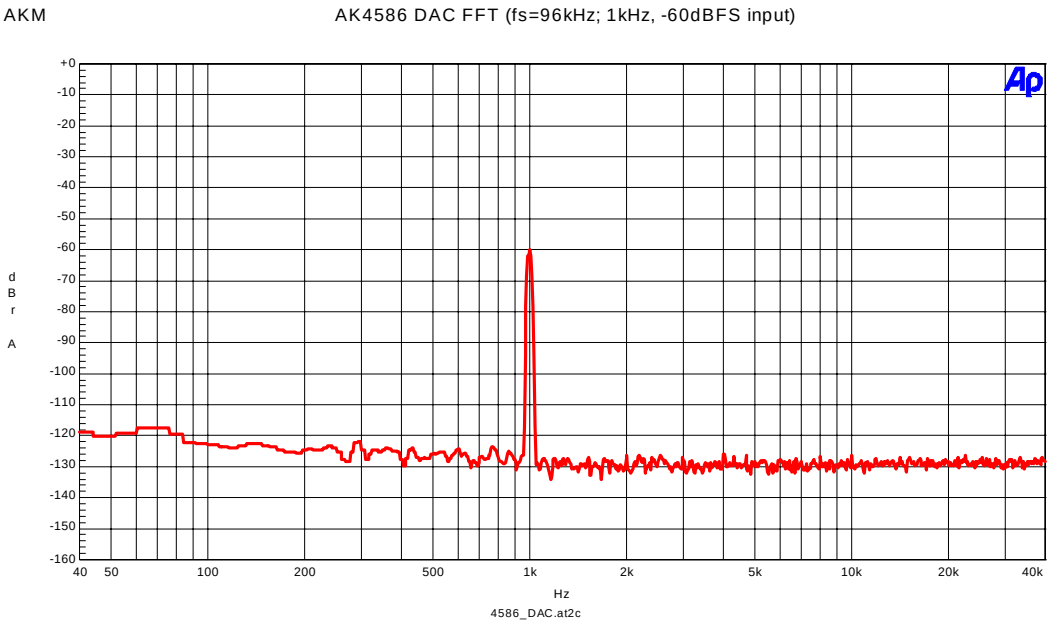


Figure 4-3. FFT (1kHz, -60dBFS input)
FFT points=16384, Avg=8, Window=Equiripple

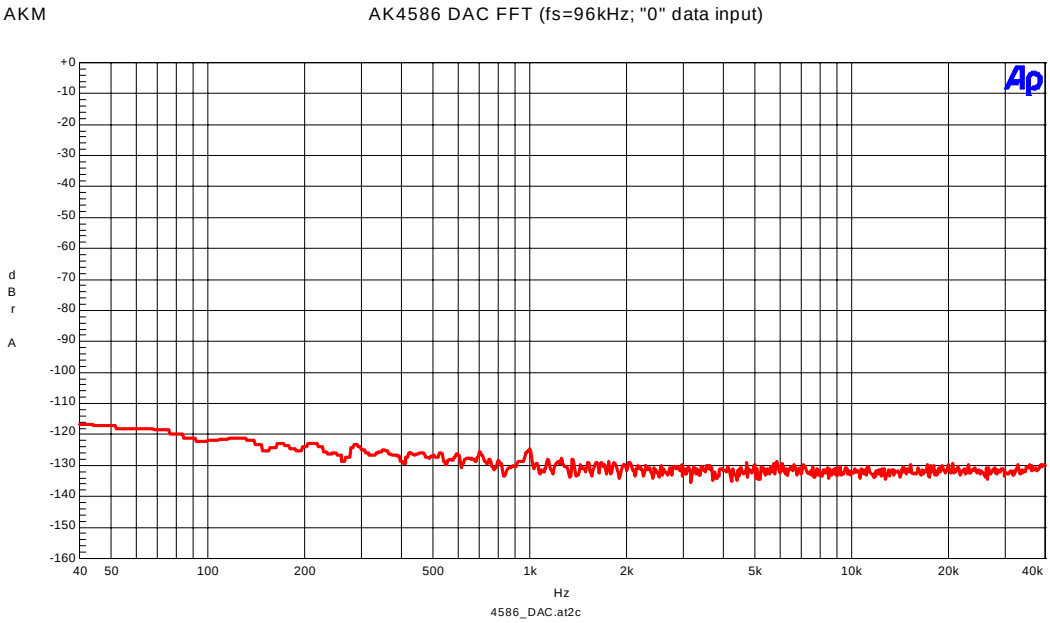


Figure 4-4. FFT (Noise floor)

(DAC, fs=96kHz)

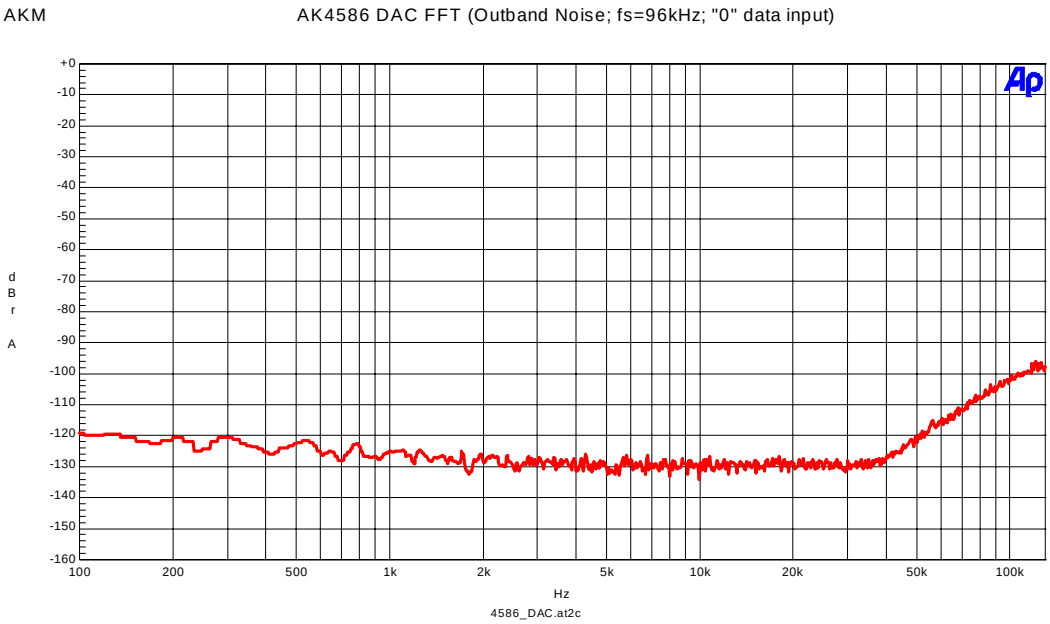


Figure 4-5. FFT (Outband noise)

(DAC, fs=96kHz)

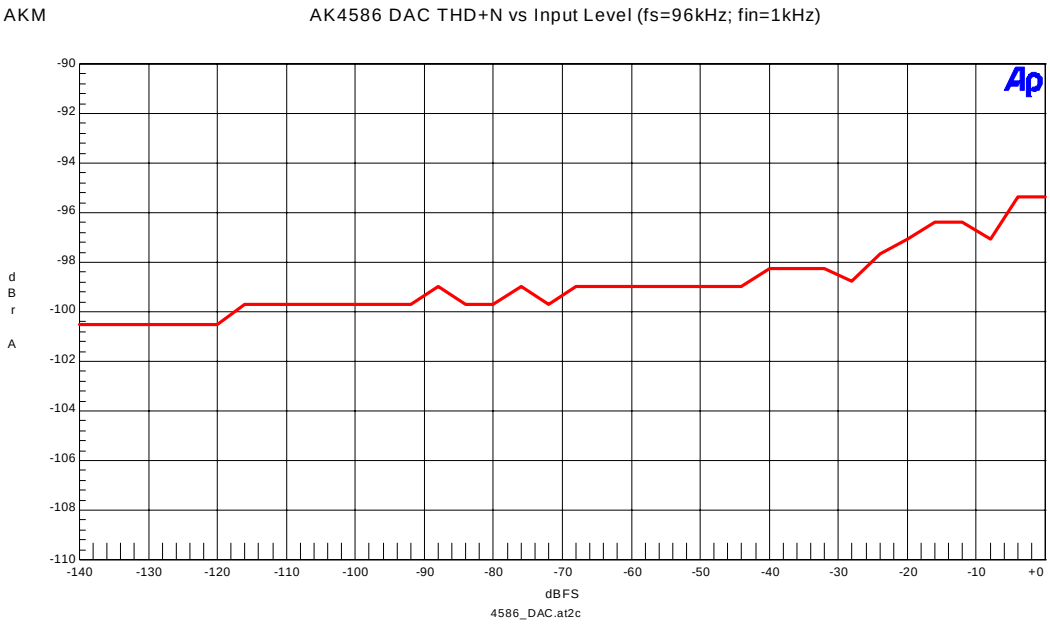


Figure 4-6. THD+N vs Input Level (fin=1kHz)

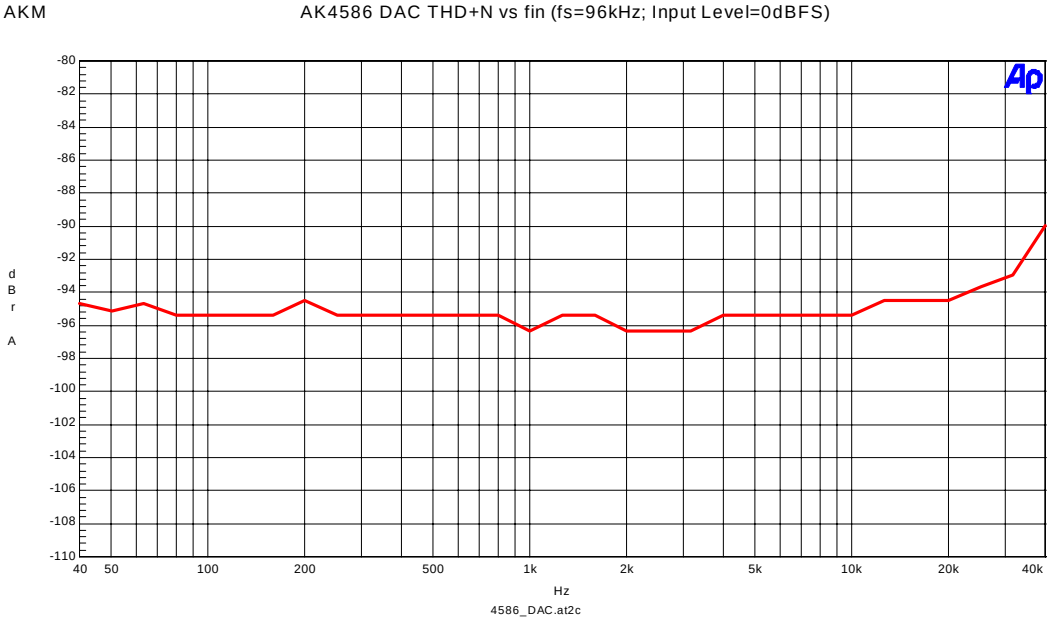


Figure 4-7. THD+N vs fin (Input Level=0dBFS)

.

(DAC, fs=96kHz)

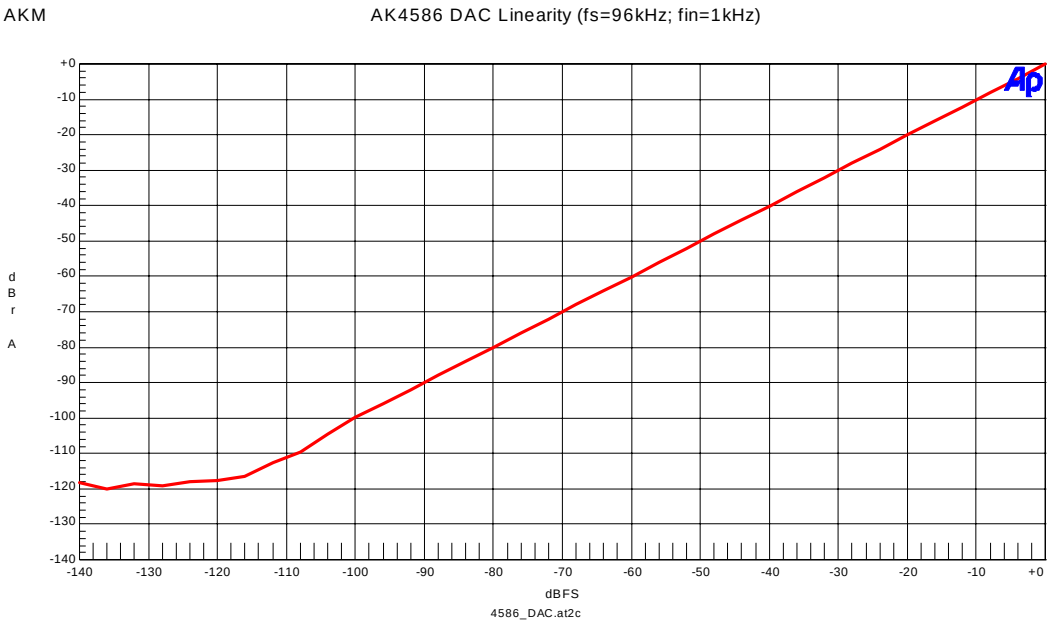


Figure 4-8. Linearity (fin=1kHz)

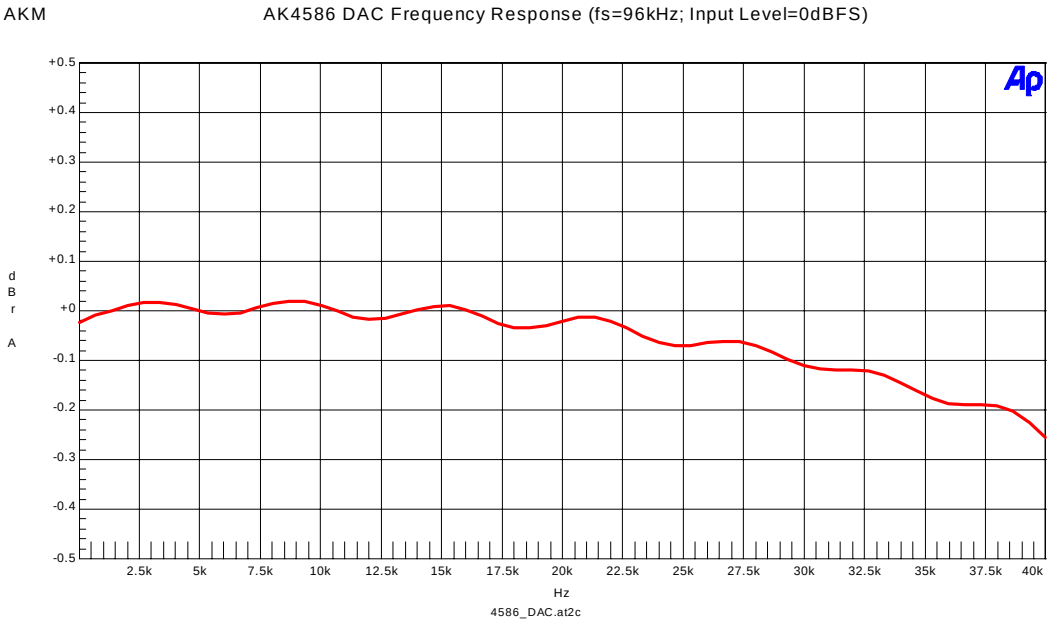


Figure 4-9. Frequency Response (Input Level=0dBFS)

(DAC, fs=96kHz)

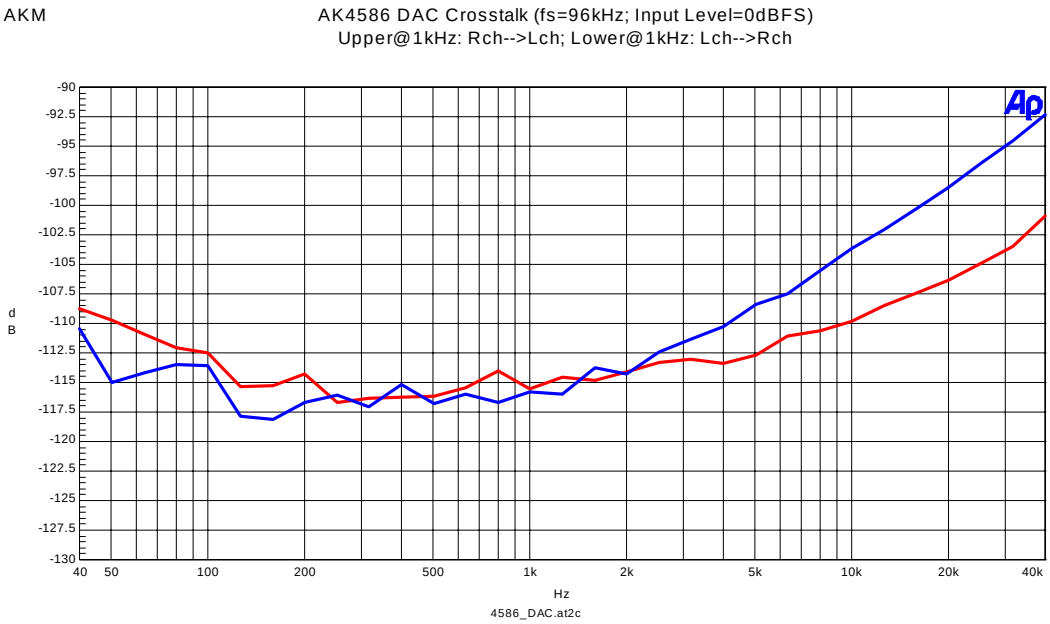


Figure 4-10. Crosstalk (Input Level=0dBFS)

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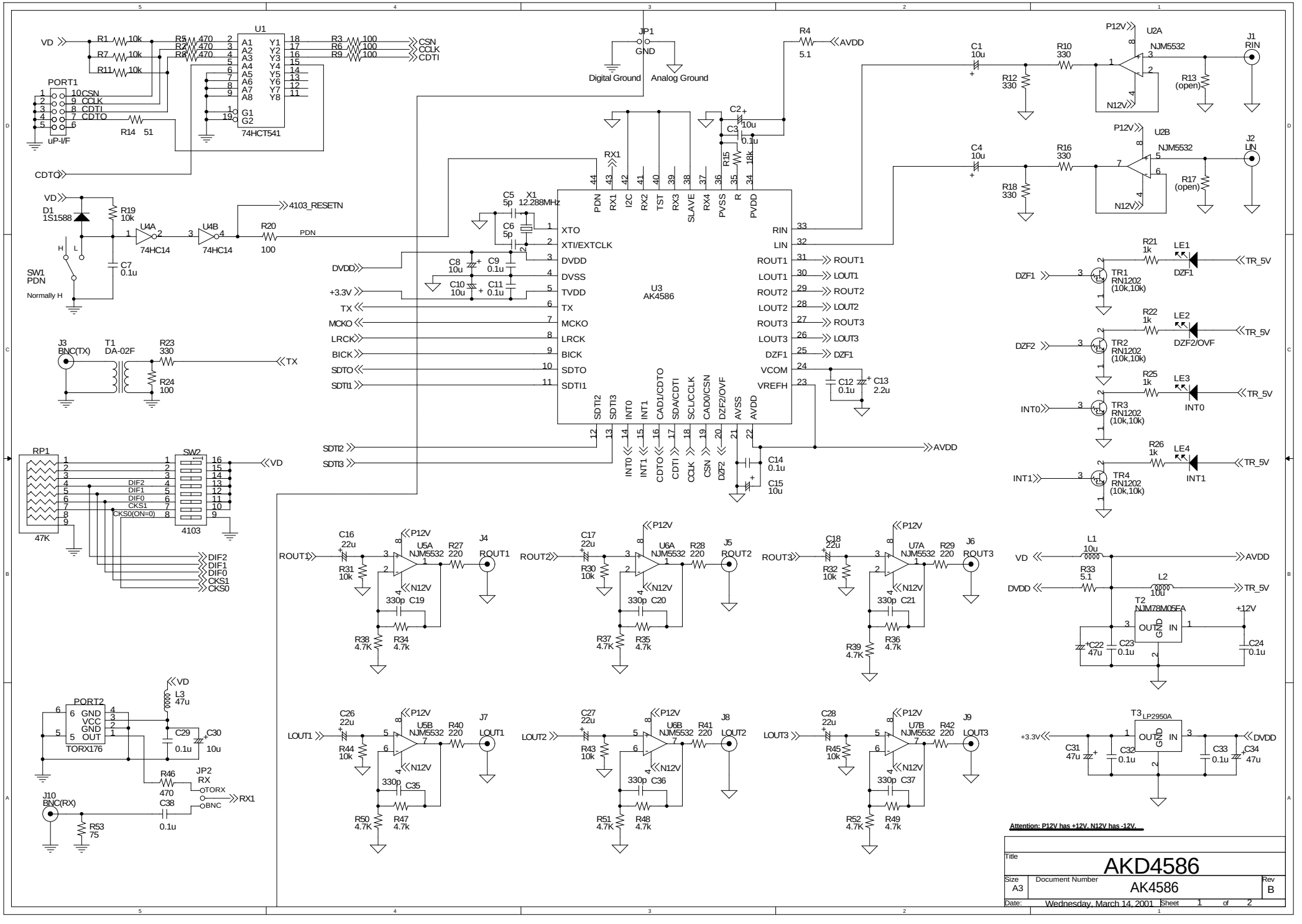
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U6B
U7A
U7B
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DA-02F
T2
NJM78M05FA
T3
LP2950A
RP1
SW1
SW2
4103
47K
JP1
GND
Digital Ground
Analog Ground
JP2
RX
TORX
BNC
J1
RIN
J2
LIN
J3
BNC(TX)
J4
J5
J6
J7
J8
J9
J10
BNC(RX)
X1
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D1
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LE1
LE2
LE3
LE4
TR1
TR2
TR3
TR4
RN1202
(10k,10k)
DZF1
DZF2/OVF
INT0
INT1
TR_5V
4103_RESETN
PDN
Normally H
CSN
CCLK
CDTI
CDTO
VD
AVDD
DVDD
+3.3V
+12V
ROUT1
ROUT2
ROUT3
LOUT1
LOUT2
LOUT3
DIF2
DIF1
DIF0
CKS1
CKS0
CKS0(ON=0)
Attention: P12V has +12V, N12V has -12V.
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Wednesday, March 14, 2001
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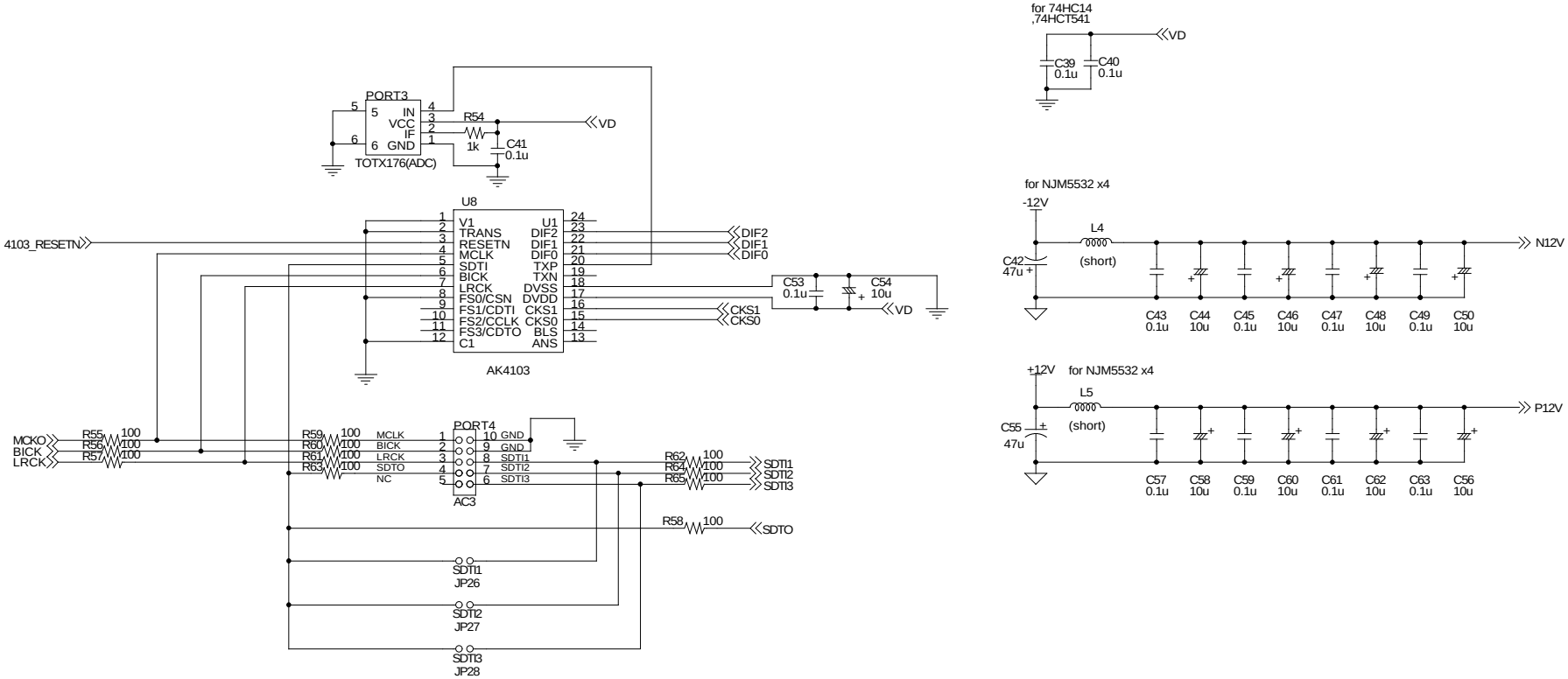

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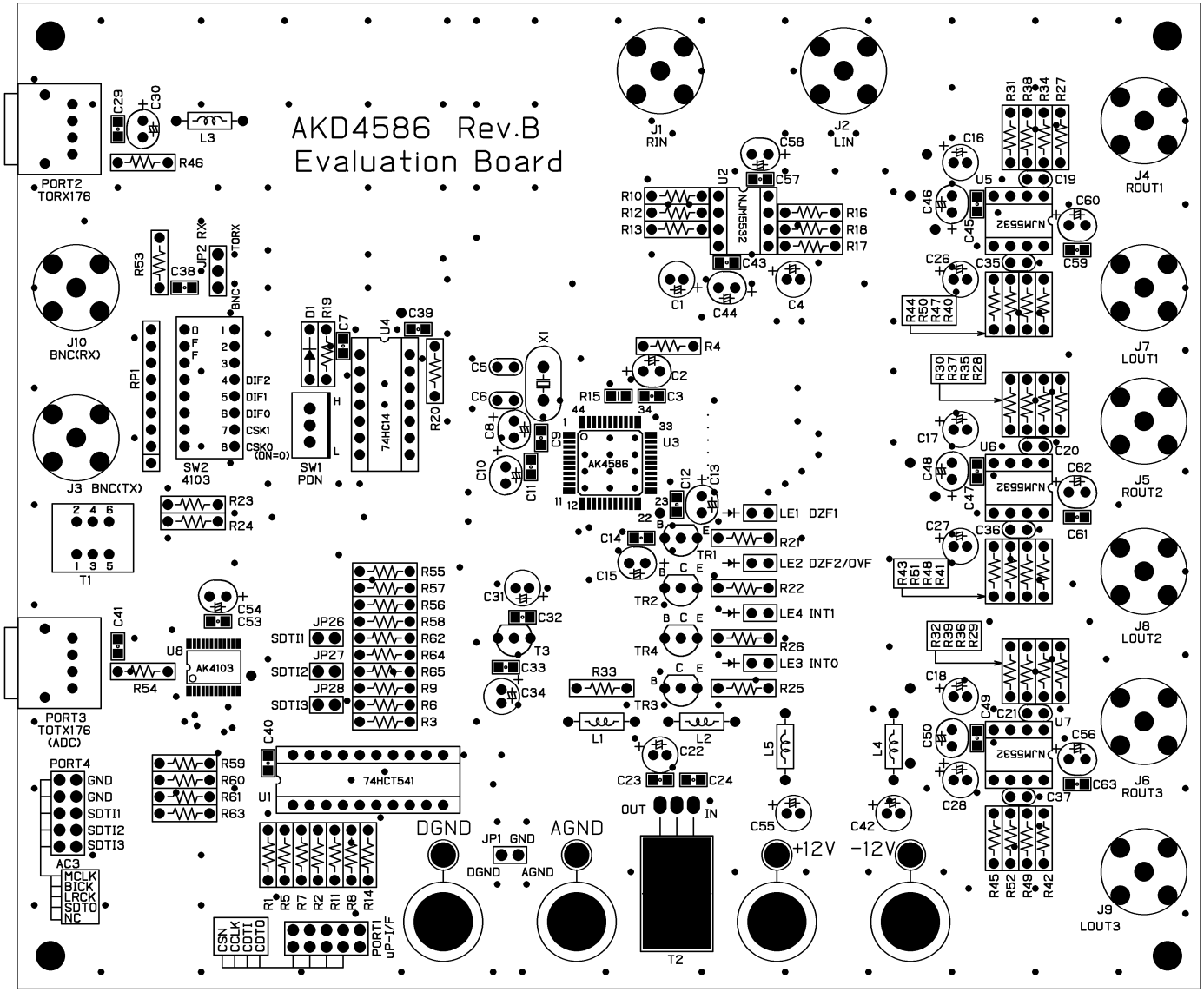
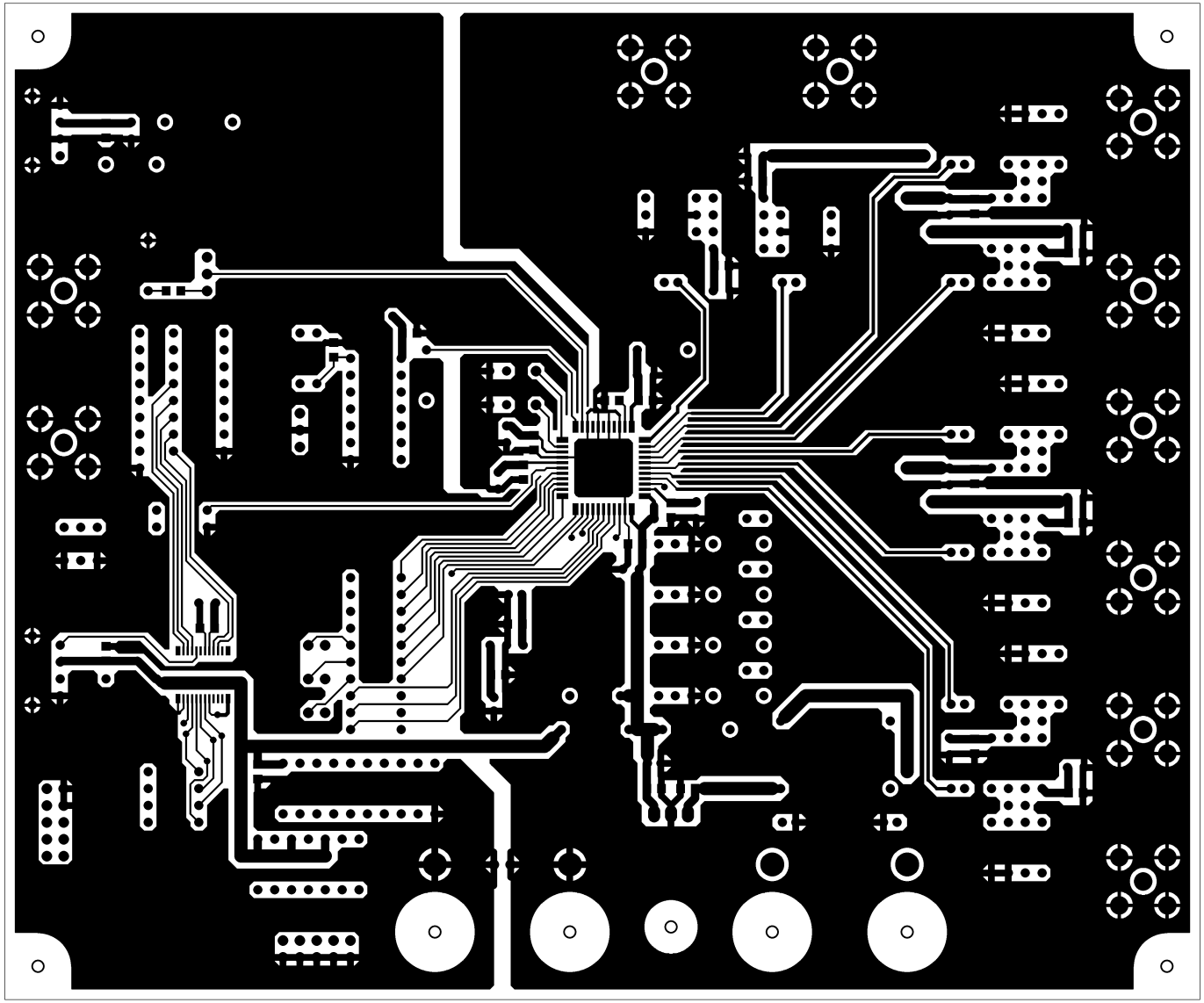
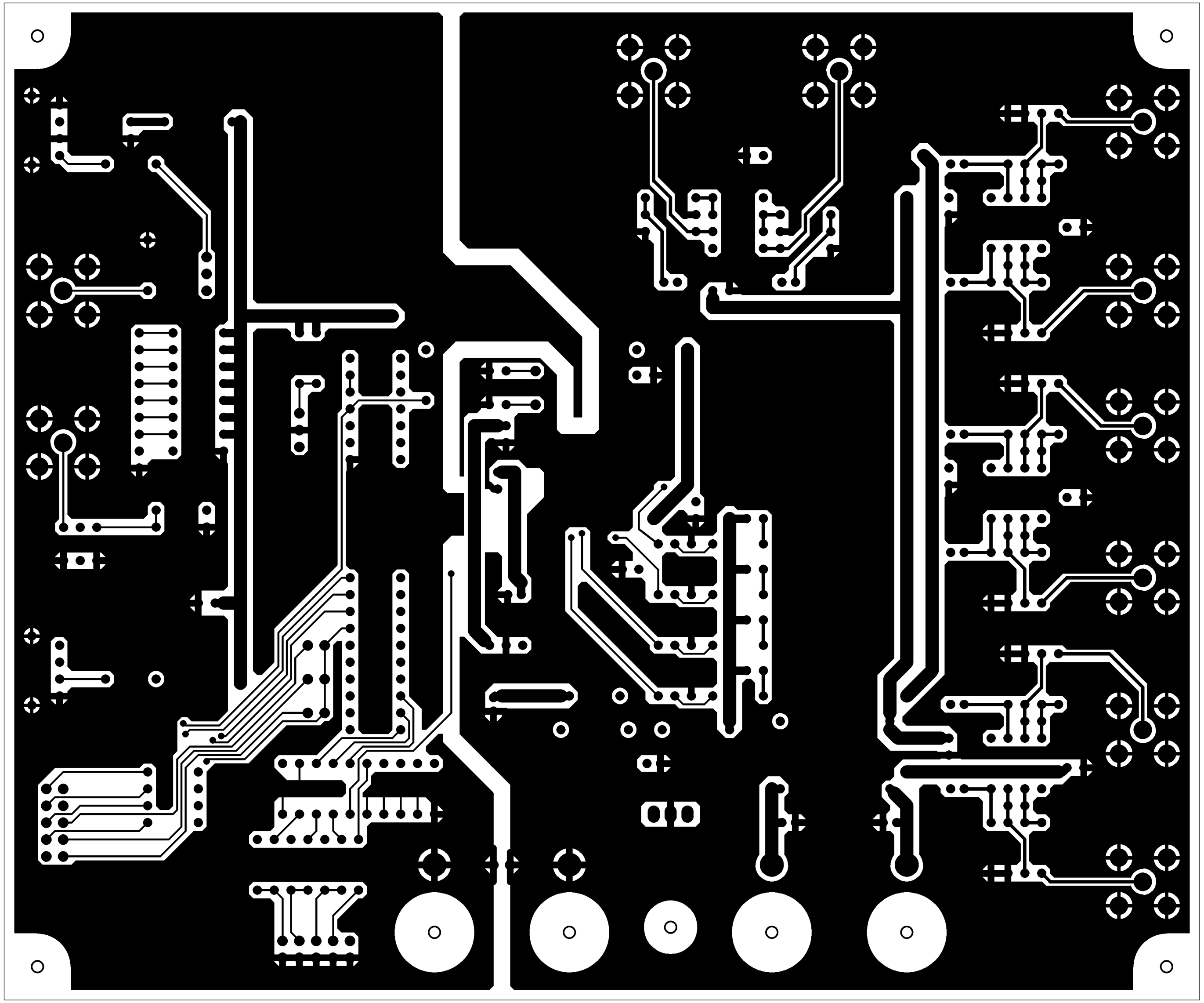
Size A3	Document Number Interface	Rev B
Date: Wednesday, March 14, 2001	Sheet 2 of 2	



L1　　レジスト　シルク　AK4586B



L1 パターン　　AK4586B



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