AKD4683-A
AK4683 Evaluation Board Rev.1

FEATURE

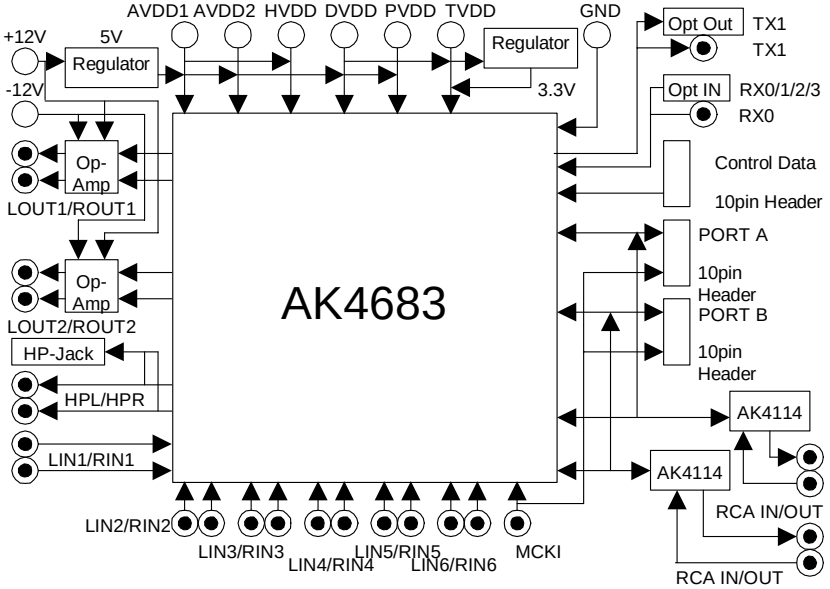
AKD4683-A is an evaluation board for AK4683, a single chip 24bit CODEC that has two channels of ADC and four channels of DAC with internal DIR, DIT. This board has interfaces with AKM's evaluation boards for A/D converter and D/A converter and makes easy to evaluate AK4683. Also this board has the digital audio interface and then achieves the interface with digital audio systems via opt-connector or RCA connector.

■ Ordering guide

AKD4683-A --- AK4683 Evaluation Board
10 wire flat cable for connection with printer port of PC (IBM-AT compatible machine), control software for AK4589, driver for control software on Windows 2000/XP are packed with this.
Control software does not work on Windows NT
Windows 2000/XP needs an installation of driver.
Windows 95/98/ME does not need an installation of driver.
AK4683 supports the standard-mode I^2C-bus (max: 100kHz), and does not support a fast-mode I^2C-bus system (max: 400kHz).

FUNCTION

- ☐ **On-board clock generator (use AK4114, x2)**
- ☐ **Compatible with 2 types of digital audio interface**
  - **Optical output/input and RCA input/output**
  - **10pin header for interface with external data source (x2)**
- ☐ **RCA connector for clock input with external clock source**
- ☐ **10pin header for register control**



(Note) AK4114 has DIR, DIT and X'tal oscillator.
Figure 1. AKD4683-A Block Diagram
(* Circuit diagram and PCB layout are attached at the end of this manual.)

EVALUATION BOARD MANUAL

■ Operation sequence

1. Power supply lines and jumpers for power supply / ground

    1-1. Power supply circuit
    1-2. Power supply lines
    1-3. Jumpers for power supply / ground

2. Register control

    2-1. 10-wire flat cable for register control
    2-2. 4-wire serial control
    2-3. I^2C-bus control

3. 10-wire flat cable for interface with external data source

    3-1. PORT4 (for PORTA)
    3-2. PORT5 (for PORTB)

4. Jumpers of Master Clock: MCKI / MCLK2

    4-1. External Master Clock
    4-2. PORTA: AK4114 (U7)
    4-3. PORTB: AK4114 (U10)

5. Jumpers of Master Clock: MCKO / X'tal

    5-1. PORTA: AK4114 (U7)
    5-2. PORTB: AK4114 (U10)

6. DIP Switches

    6-1. SW2 (PORTA_DIR/4683)
    6-2. SW4 (PORTB_DIR)

7. Evaluation mode

    7-1. DAC with internal DIR
    7-2. ADC with internal DIT
    7-3. DAC with external DIR
        7-3-1. DAC with PORTA: AK4114 (U7) as external DIR
        7-3-2. DAC with PORTB: AK4114 (U10) as external DIR
    7-4. ADC with external DIT
        7-4-1. ADC with PORTA: AK4114 (U7) as external DIT
        7-4-2. ADC with PORTB: AK4114 (U10) as external DIT
    7-5. Internal loop back (Analog input → ADC → DAC → Analog output)
    7-6. Headphone output

8. Power on

    8-1. Toggle switch
    8-2. LED
    8-3. Reset after power on

1. Power supply lines and jumpers for power supply / ground

1-1. Power supply circuit

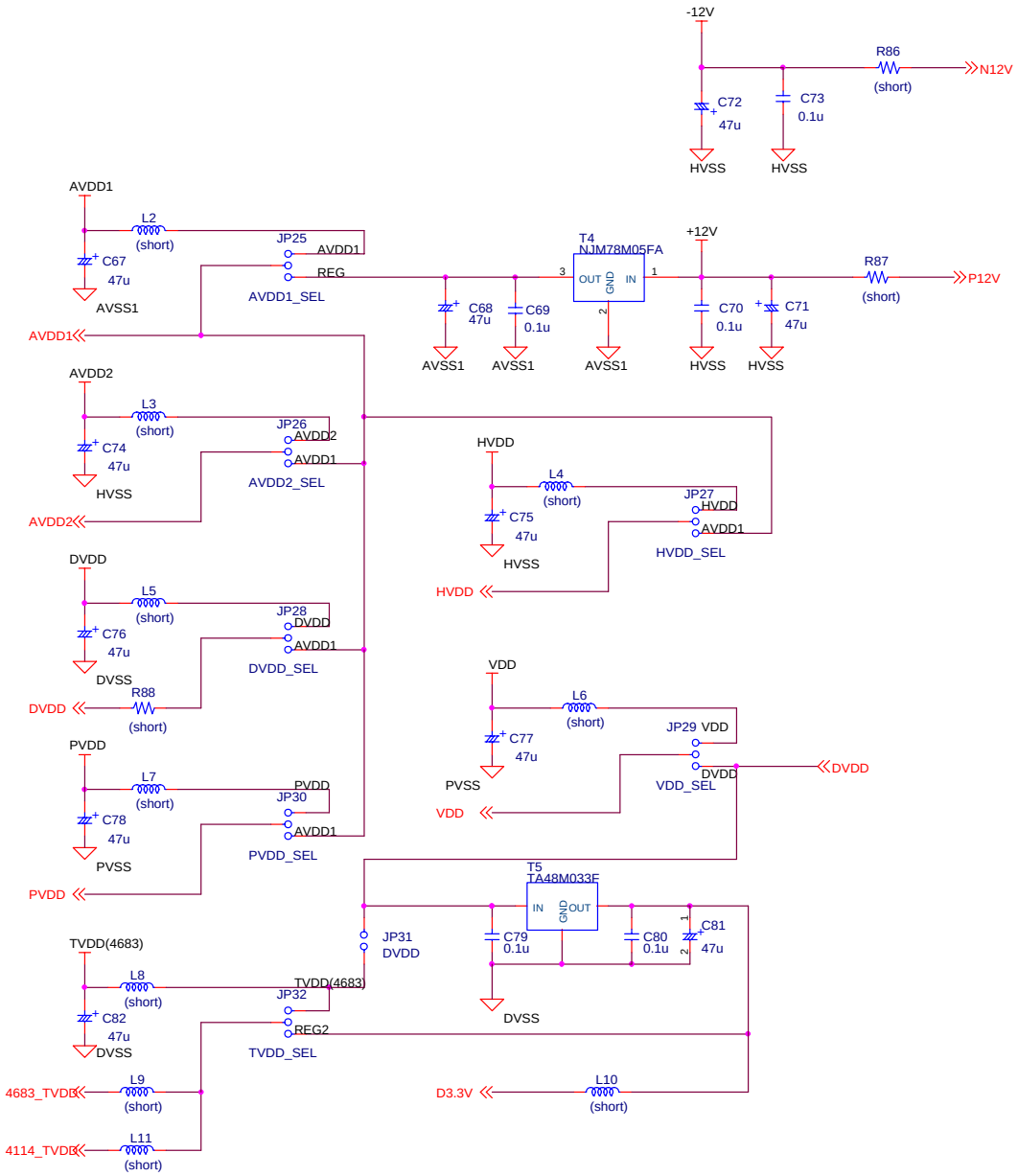


Figure 2. Power supply circuit

1-2. Power supply lines

Name of jack	Color of jack	Voltage	Used for	Comment and attention	Default Setting
AVDD1	Orange	+4.5~+5.5V	AVDD1 of AK4683	Should be always connected when JP25 (AVDD1_SEL) is set to AVDD1 side. Can be open when JP25 (AVDD1_SEL) is set to REG side.	Open
AVDD2	Orange	+4.5~+5.5V	AVDD2 of AK4683	Should be always connected when JP26 (AVDD2_SEL) is set to AVDD2 side. Can be open when JP26 (AVDD2_SEL) is set to AVDD1 side.	Open
DVDD	Orange	+4.5~+5.5V	DVDD of AK4683	Should be always connected when JP28 (DVDD_SEL) is set to DVDD side. Can be open when JP28 (DVDD_SEL) is set to AVDD1 side.	Open
PVDD	Orange	+4.5~+5.5V	PVDD of AK4683	Should be always connected when JP30 (PVDD_SEL) is set to PVDD side. Can be open when JP30 (PVDD_SEL) is set to AVDD1 side.	Open
HVDD	Orange	+4.5~+5.5V	HVDD of AK4683	Should be always connected when JP27 (HVDD_SEL) is set to HVDD side. Can be open when JP27 (HVDD_SEL) is set to AVDD1 side.	+5V
VDD	Orange	+4.5~+5.5V	Logic Parts	Should be always connected when JP29 (VDD_SEL) is set to VDD side. Can be open when JP29 (VDD_SEL) is set to DVDD side.	+5V
TVDD (4683)	Orange	+2.7~+5.5V	TVDD of AK4683, TVDD of AK4114	Should be always connected when JP31 (DVDD) is open, and JP32 (TVDD_SEL) is set to TVDD side. Can be open when JP31 (DVDD) is open, and JP32 (TVDD_SEL) is set to REG2 side, or when JP31 (DVDD) is short, and JP32 (TVDD_SEL) is set to TVDD side.	Open
+12V	Red	+12~+15V	Regulator, Output Buffer (Op-amp)	Power supply for Regulator, Output Buffer (Op-amp). Should be always connected.	+12V
-12V	Blue	-12~-15V	Output Buffer (Op-amp)	Power supply for Output Buffer (Op-amp). Should be always connected.	-12V
AVSS1	Black	0V	Analog Ground	Analog Ground. Should be always connected.	0V
HVSS	Black	0V	Analog Ground	Analog Ground. Should be always connected.	0V
DVSS	Black	0V	Analog Ground	Analog Ground. Should be always connected.	0V
PVSS	Black	0V	Analog Ground	Analog Ground. Should be always connected.	0V
DGND	Black	0V	Digital Ground	Digital Ground. Should be connected when JP1 is open. Can be open when JP1 is short.	0V

Table 1. Power supply lines

(Note) Each supply line should be distributed from the power supply unit.

1-3. Jumpers for power supply / ground

1-3-1. AVDD1

JP25 (AVDD1_SEL) controls AVDD1 source (regulator T4 or jack "AVDD1").

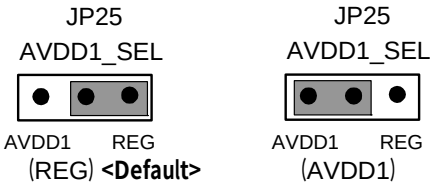


Figure 3. JP25 (AVDD1_SEL)

1-3-2. AVDD2

JP26 (AVDD2_SEL) controls AVDD2 source (AVDD1 line or jack "AVDD2").

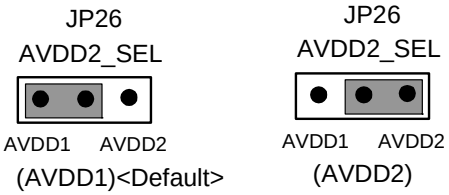


Figure 4. JP26 (AVDD2_SEL)

1-3-3. DVDD

JP28 (DVDD_SEL) controls DVDD source (AVDD1 line or jack "DVDD").

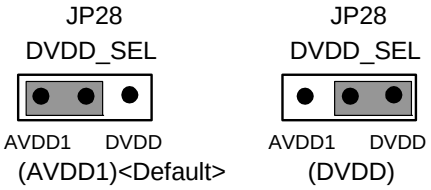


Figure 5. JP28 (DVDD_SEL)

1-3-4. PVDD

JP30 (PVDD_SEL) controls PVDD source (AVDD1 line or jack “PVDD”).

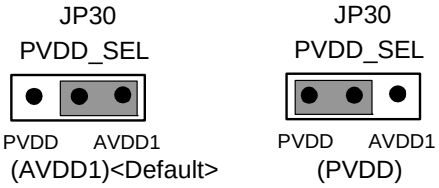


Figure 6. JP30 (PVDD_SEL)

1-3-5. HVDD

JP27 (HVDD_SEL) controls HVDD source (AVDD1 line or jack “HVDD”).

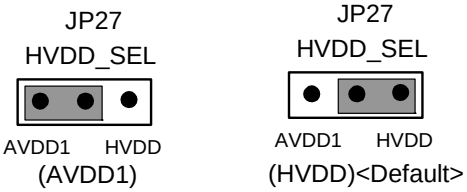


Figure 7. JP27 (HVDD_SEL)

1-3-6. VDD

JP29 (VDD_SEL) controls VDD source (DVDD line or jack “VDD”).

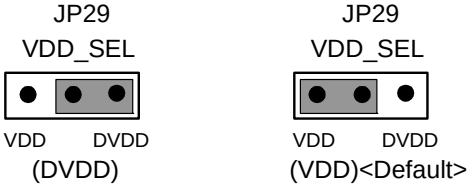


Figure 8. JP29 (VDD_SEL)

1-3-7. TVDD and DVDD

JP31 (DVDD) controls separate (open) or connect (short) of TVDD and DVDD.

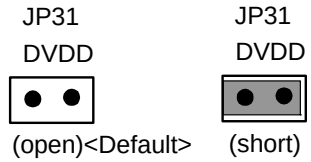


Figure 9. JP31 (DVDD)

1-3-8. TVDD for AK4683 and AK4114

JP32 (TVDD_SEL) controls TVDD source (regulator T5 or jack "TVDD (4683)") for AK4683 and AK4114.

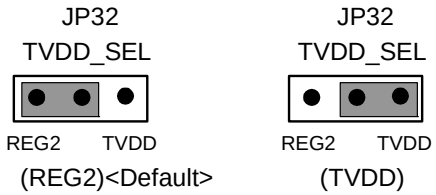


Figure 10. JP32 (TVDD_SEL)

1-3-9. Analog Ground and Digital Ground

JP1 (DGND) controls separate (open) or connect (short) of Analog Ground and Digital Ground.
In this case, jack "DGND" can be open.

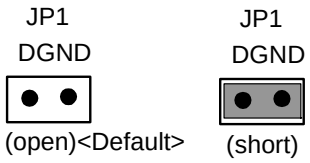


Figure 11. JP1 (DGND)

2. Register control

2-1. 10-wire flat cable for register control

AK4683 can be controlled via printer port (parallel port) of IBM-AT compatible PC. Connect printer port (parallel port) of PC and PORT2 (uP-I/F) of AKD4683-A by 10-wire flat cable (packed with AKD4683-A). Take care of **the direction of 10-pin connector and 10-pin header.** (The red line side of 10-wire flat cable of 10-pin connector should be connected to No.5pin and No.6pin of 10-pin header.)

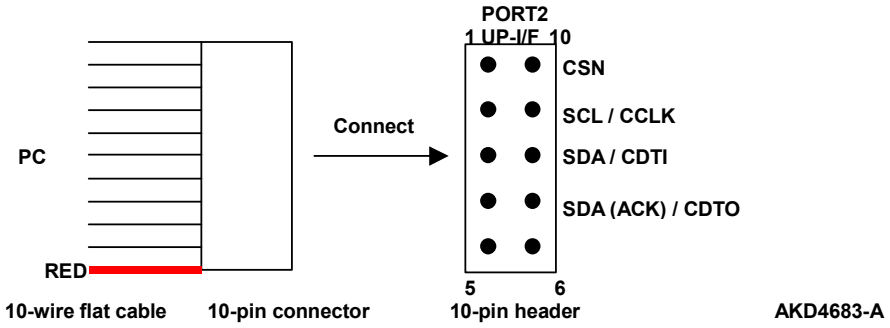


Figure 12. 10-wire flat cable, 10-pin connector and 10-pin header

2-2. 4-wire serial control

(1) Set JP3 (SDA/CDTO) to "CDTO/CM0=H". <Default>

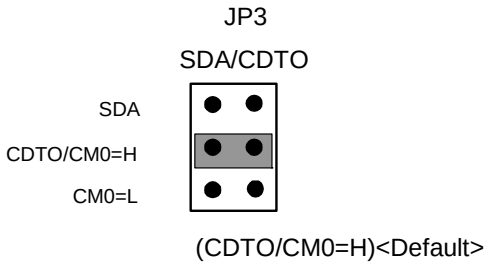


Figure 13. JP3 (SDA/CDTO)

(2) Set SW2 (PORT A_DIR/4683): No.8 pin (I2C) to "OFF". <Default>

2-3. I²C-bus control

(1) Set JP3 (SDA/CDTO) to “SDA”.

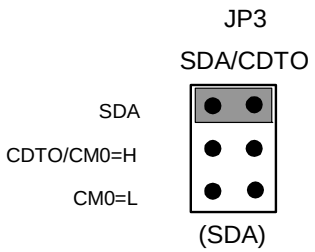


Figure 14. JP3 (SDA/CDTO)

(2) Set SW2 (PORT A_DIR/4683): No.8 pin (I2C) to “ON”.

3. 10-wire flat cable for interface to external

AK4683 can achieve the interface with external data source via PORT4 (PORTA), PORT5 (PORTB).
Connect PORT4 (PORTA) and external port or PORT5 (PORTB) and external port by 10-wire flat cable.
Take care of **the direction of 10-pin connector and 10-pin header.** (The red line side of 10-wire flat cable of 10-pin connector should be connected to No.5pin and No.6pin of 10-pin header.)

3-1. PORT4 (for PORTA)

Pin layout of PORT4 (for PORTA) is shown in Figure 15.

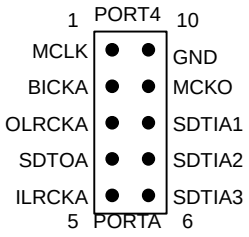


Figure 15. PORT4 (for PORTA)

3-2. PORT5 (for PORTB)

Pin layout of PORT5 (for PORTB) is shown in Figure 16.

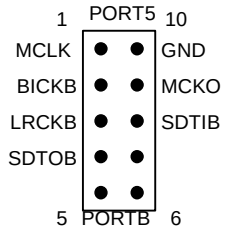


Figure 16. PORT5 (for PORTB)

4. Jumpers of Master Clock: MCKI / MCLK2

4-1. External Master Clock

JP19 (MCLK_SEL) controls External Master Clock source (MCKI / MCLK2) for AK4683.
In these two cases above, JP16 (MCLKA_SEL) and JP22 (MCLKB_SEL) should be open.

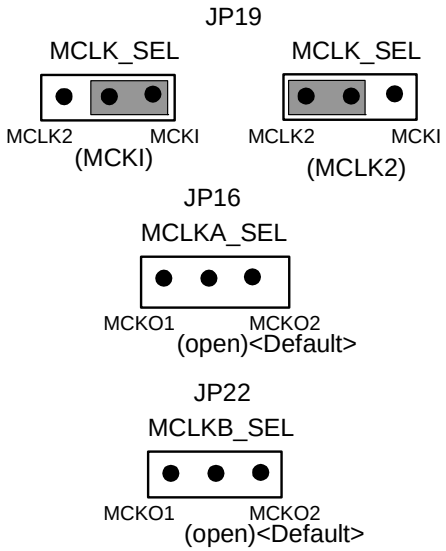


Figure 17. JP19 (MCLK_SEL)

4-2. PORTA: AK4114 (U7)

JP16 (MCLKA_SEL) controls PORTA: AK4114 (U7): Master Clock source (MCKO1 / MCKO2) for AK4683: MCLK2.
In these two cases above, JP19 (MCLK_SEL) and JP22 (MCLKB_SEL) should be open.

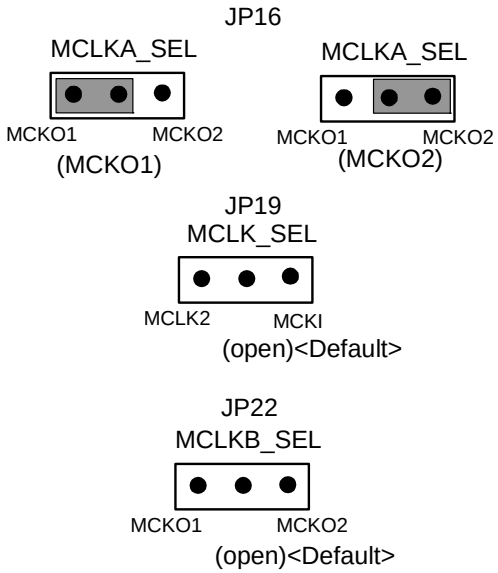


Figure 18. JP16 (MCLKA_SEL)

4-3. PORTB: AK4114 (U10)

JP22 (MCLKB_SEL) controls PORTB: AK4114 (U10): Master Clock source (MCKO1 / MCKO2) for AK4683: MCLK2.
In these two cases above, JP19 (MCLK_SEL) and JP16 (MCLKA_SEL) should be open.

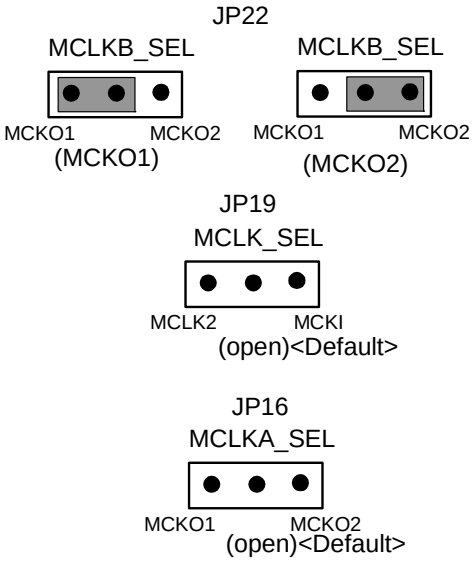


Figure 19. JP22 (MCLKB_SEL)

5. Jumpers of Master Clock: MCKO / X'tal

5-1.PORTA: AK4114 (U7)

JP10 (XTIA) controls Master Clock source (AK4683: MCKO (short) / X2: X'tal (open)) for PORTA: AK4114 (U7):XTI.

Figure 20. JP10 (XTIA)

5-2. PORTB: AK4114 (U10)

JP20 (XTIB) controls Master Clock source (AK4683: MCKO (short) / X3: X'tal (open)) for for PORTB: AK4114 (U10):XTI.

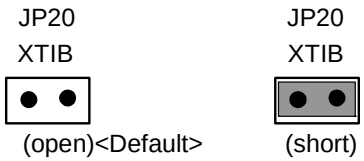


Figure 21. JP20 (XTIB)

6. DIP Switches

6-1. SW2 (PORT A_DIR/4683)

Setting for AK4683 and PORT A: AK4114 (U7)

No.	Name	ON (“H”)	OFF (“L”)	Default
1	DIF0	Setting of Audio Format of AK4114 (Refer Table 2.)		OFF (“L”, “0”)
2	DIF1			ON (“H”, “1”)
3	DIF2			ON (“H”, “1”)
4	CM0	Selection of Clock Mode (Clock Source) (Refer Table 3.)		OFF (“L”, “0”)
5	CM1			OFF (“L”, “0”)
6	OCKS0	Selection of frequency of Master Clock Output (ReferTable4.)		OFF (“L”, “0”)
7	OCKS1			OFF (“L”, “0”)
8	I2C	I^2C-bus control mode	4-wire serial control mode	OFF (“L”, “0”)

Table 2. SW2 (PORT A_DIR / 4683)

(Note) ON: “H” (“1”), OFF: “L” (“0”)

6-2. SW4 (PORT B_DIR)

Setting for PORT B: AK4114 (U10)

No.	Name	ON (“H”)	OFF (“L”)	Default
1	DIF0	Setting of Audio Format of AK4114 (Refer Table 2.)		OFF (“L”, “0”)
2	DIF1			ON (“H”, “1”)
3	DIF2			ON (“H”, “1”)
4	CM0	Selection of Clock Mode (Clock Source) (Refer Table 3.)		OFF (“L”, “0”)
5	CM1			OFF (“L”, “0”)
6	OCKS0	Selection of frequency of Master Clock Output (Refer Table4.)		OFF (“L”, “0”)
7	OCKS1			OFF (“L”, “0”)
8	NC	Un-used		OFF (“L”, “0”)

Table 3. SW4 (PORT B_DIR)

(Note) ON: “H” (“1”), OFF: “L” (“0”)

Mode	DIF2	DIF1	DIF0	DAUX	SDTO	LRCK		BICK		
							I/O		I/O	
0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
1	0	0	1	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
2	0	1	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
3	0	1	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
4	1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	
5	1	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	
6	1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I	<Default>
7	1	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I	

Table 4. Audio Interface Format of AK4114

Mode	CM1	CM0	UNLOCK	PLL	X'tal	Clock source	SDTO	
0	0	0	-	ON	ON (Note1)	PLL	RX	<Default>
1	0	1	-	OFF	ON	X'tal	DAUX	
2	1	0	0	ON	ON	PLL	RX	
			1	ON	ON	X'tal	DAUX	
3	1	1	-	ON	ON	X'tal	DAUX	

Table 5. Clock Mode (Clock Source)

(Note1) When X'tal is not used on reference clock (XTL0, 1= "1, 1"), this setting is "OFF"

(Note2) Normally, use "Default" setting.

No.	OCKS1	OCKS0	MCKO1	MCKO2	X'tal	fs (max)	
0	0	0	256fs	256fs	256fs	96 kHz	<Default>
1	0	1	256fs	128fs	256fs	96 kHz	
2	1	0	512fs	256fs	512fs	48 kHz	
3	1	1	128fs	64fs	128fs	192 kHz	

Table 6. Frequency of Master Clock Output

7. Evaluation mode

7-1. DAC with internal DIR

7-1-1. Connection of connector

In case of input through RX0, optical connector PORT3 (TORX176) or RCA connector J14 (RX0) are available. In case of input through RX1, RX2 or RX3, only the optical connector PORT3 is available.

7-1-2. Setting of jumper pin

In case of input through RX0, JP4 (RX0) controls digital input (optical connector PORT3 or RCA connector J14).

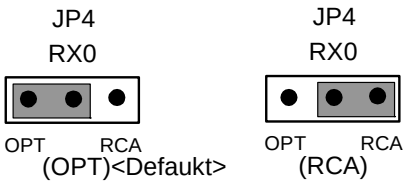


Figure 22. JP4 (RX0)

In case of input through RX1, RX2 or RX3, jumpers JP5 (RX1), JP6 (RX2) or JP7 (RX3) control digital input channels (RX1, RX2 or RX3) from PORT3.
About only input channels, set some of jumpers JP5 (RX1), JP6 (RX2) or JP7 (RX3) to OPT.
About no-input channels, set other of jumpers JP5 (RX1), JP6 (RX2) or JP7 (RX3) to GND.

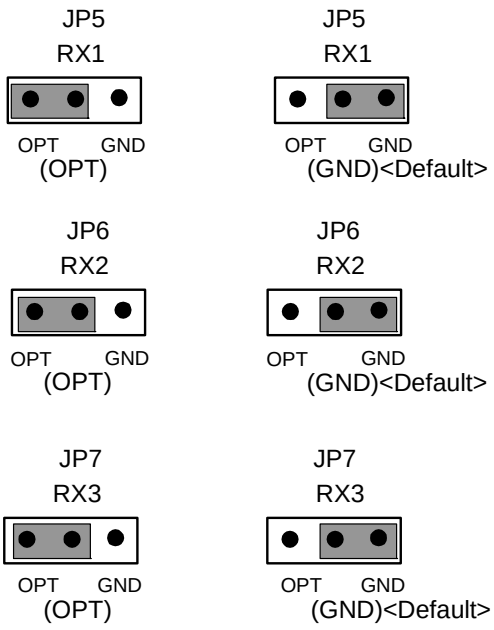


Figure 23. JP5 (RX1), JP6 (RX2), JP7 (RX3)

Setting of interface signal of PORTA: AK4114 (U7) is as follows.

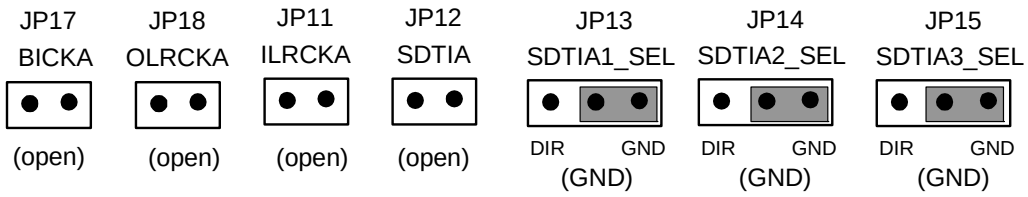


Figure 24. JP17 (BICKA), JP18 (OLRCKA), JP11 (ILRCKA), JP12 (SDTIA), JP13 (SDTIA1_SEL), JP14 (SDTIA2_SEL), JP15 (SDTIA3_SEL)

Setting of interface signal of PORTB: AK4114 (U10) is as follows.

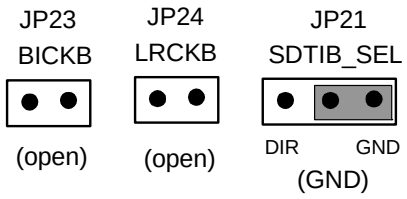


Figure 25. JP23 (BICKB), JP24 (LRCKB), JP21 (SDTIB_SEL)

7-1-3. Setting of DIP switch

SW2 (PORTA_DIR/4683) and SW4 (PORTB_DIR) are “Don’t care”.

7-1-4. Setting of toggle switch

Set SW3 (DIR PORTA) to OFF.
Set SW5 (DIR PORTB) to OFF.
Set SW1 (PDN) to OFF→ON.

7-2. ADC with internal DIT

7-2-1. Connection of connector

For output, optical connector PORT1 (TOTX176) or RCA connector J13 (TX1) are available.

7-2-2. Setting of jumper pin

JP2 (TX1) controls digital output (optical connector PORT1 or RCA connector J13).

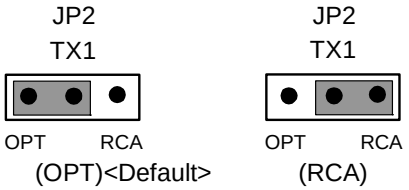


Figure 26. JP2 (TX1)

Setting of interface signal of PORTA: AK4114 (U7) is as follows.

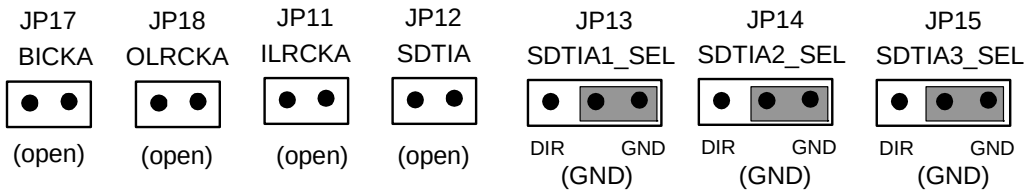


Figure 27. JP17 (BICKA), JP18 (OLRCKA), JP11 (ILRCKA), JP12 (SDTIA), JP13 (SDTIA1_SEL), JP14 (SDTIA2_SEL), JP15 (SDTIA3_SEL)

Setting of interface signal of PORTB: AK4114 (U10) is as follows.

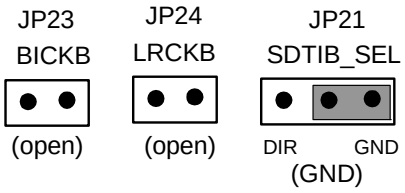


Figure 28. JP23 (BICKB), JP24 (LRCKB), JP21 (SDTIB_SEL)

7-2-3. Setting of DIP switch

SW2 (PORTA_DIR/4683) and SW4 (PORTB_DIR) are “Don’t care”.

7-2-4. Setting of toggle switch

Set SW3 (DIR PORTA) to OFF.
Set SW5 (DIR PORTB) to OFF.
Set SW1 (PDN) to OFF→ON.

7-3. DAC with external DIR

7-3-1. DAC with PORT A: AK4114 (U7) as external DIR

7-3-1-1. Connection of connector

For digital input, RCA connector J22 (PORTA_RX0) is available.

7-3-1-2. Setting of jumper pin

Setting of interface signal of PORTA: AK4114 (U7) is as follows.

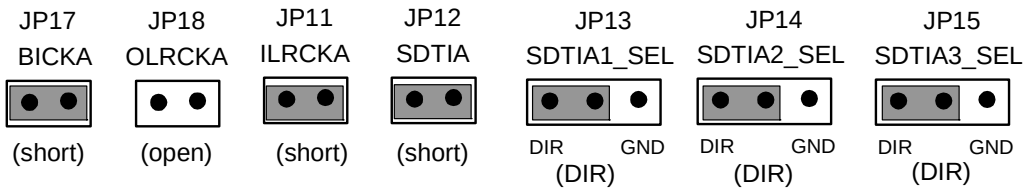


Figure 29. JP17 (BICKA), JP18 (OLRCKA), JP11 (ILRCKA), JP12 (SDTIA), JP13 (SDTIA1_SEL), JP14 (SDTIA2_SEL), JP15 (SDTIA3_SEL)

Setting of interface signal of PORTB: AK4114 (U10) is as follows.

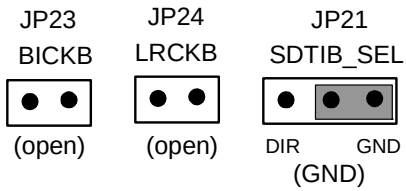


Figure 30. JP23 (BICKB), JP24 (LRCKB), JP21 (SDTIB_SEL)

When master clock of PORTA: AK4114 (U7): MCKO1 is supplied to AK4683: MCLK2, setting of master clock is as follows.

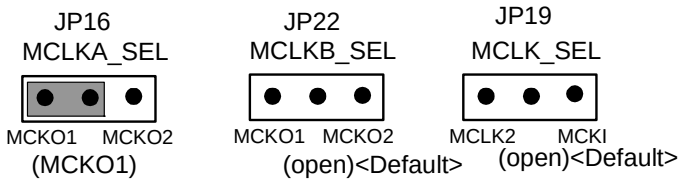


Figure 31. JP16 (MCLKA_SEL), JP22 (MCLKB_SEL), JP19 (MCLK_SEL)

7-3-1-3. Setting of DIP switch

Set SW2 (PORTA_DIR/4683): 5pin (CM1) to OFF.
Set SW2 (PORTA_DIR/4683): 4pin (CM0) to OFF.

7-3-1-4. Setting of toggle switch

Set SW3 (DIR PORTA) to ON.
Set SW5 (DIR PORTB) to OFF.
Set SW1 (PDN) to OFF→ON.

7-3-2. DAC with PORT B: AK4114 (U10) as external DIR

7-3-2-1. Connection of connector

For digital input, RCA connector J25 (PORTB_RX0) is available.

7-3-2-2. Setting of jumper pin

Setting of interface signal of PORTA: AK4114 (U7) is as follows.

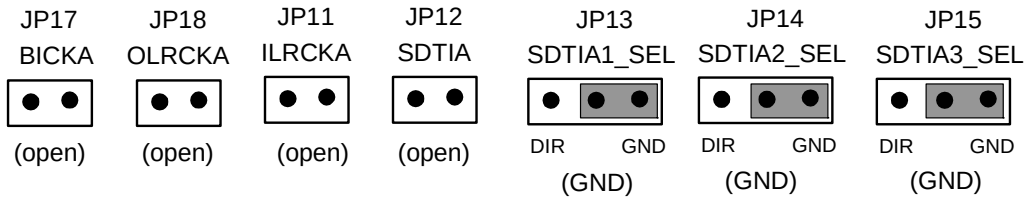


Figure 32. JP17 (BICKA), JP18 (OLRCKA), JP11 (ILRCKA), JP12 (SDTIA), JP13 (SDTIA1_SEL), JP14 (SDTIA2_SEL), JP15 (SDTIA3_SEL)

Setting of interface signal of PORTB: AK4114 (U10) is as follows.

Figure 33. JP23 (BICKB), JP24 (LRCKB), JP21 (SDTIB_SEL)

When master clock of PORTB: AK4114 (U10): MCKO1 is supplied to AK4683: MCLK2, setting of master clock is as follows.

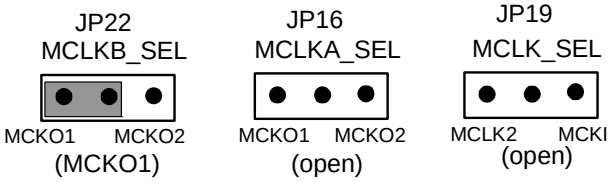


Figure 34. JP22 (MCLKB_SEL), JP16 (MCLKA_SEL), JP19 (MCLK_SEL)

7-3-2-3. Setting of DIP switch

Set SW4 (PORTB_DIR): 5pin (CM1) to OFF.
Set SW4 (PORTB_DIR): 4pin (CM0) to OFF.

7-3-2-4. Setting of toggle switch

Set SW3 (DIR PORTA) to OFF.
Set SW5 (DIR PORTB) to ON.
Set SW1 (PDN) to OFF→ON.

7-4. ADC with external DIT

7-4-1. ADC with PORT A: AK4114 (U7) as external DIT

7-4-1-1. Connection of connector

For digital output, RCA connector J23 (PORTA_TX1) is available.

7-4-1-2. Setting of jumper pin

Setting of interface signal of PORTA: AK4114 (U7) is as follows.

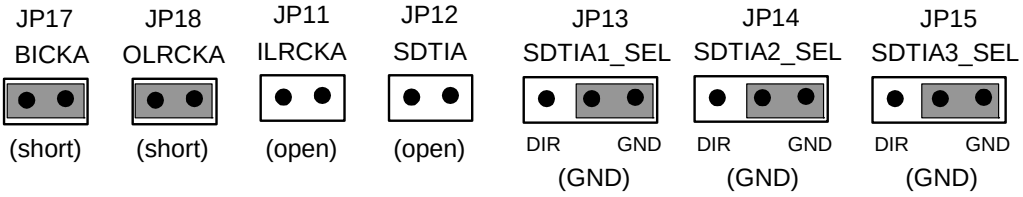


Figure 35. JP17 (BICKA), JP18 (OLRCKA), JP11 (ILRCKA), JP12 (SDTIA), JP13 (SDTIA1_SEL), JP14 (SDTIA2_SEL), JP15 (SDTIA3_SEL)

Setting of interface signal of PORTB: AK4114 (U10) is as follows.

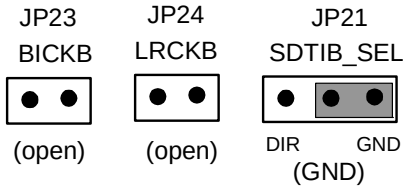


Figure 36. JP23 (BICKB), JP24 (LRCKB), JP21 (SDTIB_SEL)

When master clock of AK4683: MCKO is supplied to PORTA: AK4114 (U7): XTI, setting of master clock is as follows.

Figure 37. JP10 (XTIA)

7-4-1-3. Setting of DIP switch

Set SW2 (PORTA_DIR/4683): 5pin (CM1) to OFF.
Set SW2 (PORTA_DIR/4683): 4pin (CM0) to ON.

7-4-1-4. Setting of toggle switch

Set SW3 (DIR PORTA) to ON.
Set SW5 (DIR PORTB) to OFF.
Set SW1 (PDN) to OFF→ON.

7-4 -2. ADC with PORT B: AK4114 (U10) as external DIT

7-4-2-1. Connection of connector

For digital output, RCA connector J26 (PORTB_TX1) is available.

7-4-2-2. Setting of jumper pin

Setting of interface signal of PORTA: AK4114 (U7) is as follows.

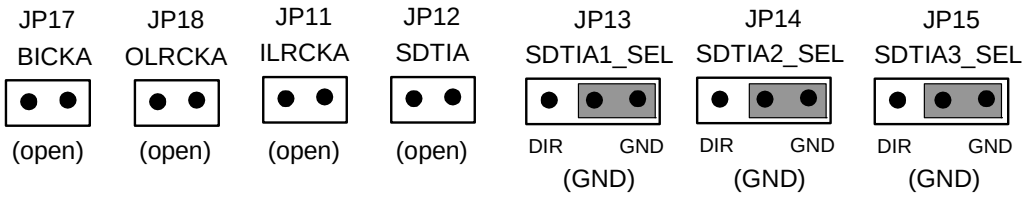


Figure 38. JP17 (BICKA), JP18 (OLRCKA), JP11 (ILRCKA), JP12 (SDTIA), JP13 (SDTIA1_SEL), JP14 (SDTIA2_SEL), JP15 (SDTIA3_SEL)

Setting of interface signal of PORTB: AK4114 (U10) is as follows.

Figure 39. JP23 (BICKB), JP24 (LRCKB), JP21 (SDTIB_SEL)

When master clock of AK4683: MCKO is supplied to PORTB: AK4114 (U10): XTI, setting of master clock is as follows.

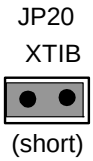


Figure 40. JP20 (XTIB)

7-4-2-3. Setting of DIP switch

Set SW4 (PORTB_DIR): 5pin (CM1) to OFF.
Set SW4 (PORTB_DIR): 4pin (CM0) to ON.

7-4-2-4. Setting of toggle switch

Set SW3 (DIR PORTA) to OFF.
Set SW5 (DIR PORTB) to ON.
Set SW1 (PDN) to OFF→ON.

7-5. Internal loop back (Analog input → ADC → DAC → Analog output)

7-5-1. Connection of connector

For analog input, RCA connector J1 (LIN1)/ J4 (RIN1), J2 (LIN2)/ J5 (RIN2), J3 (LIN3)/ J6 (RIN3), J7 (LIN4)/ J10 (RIN4), J8 (LIN5)/ J11 (RIN5), J9 (LIN6)/ J12 (RIN6) are available.
For analog output, RCA connector J15 (LOUT1)/ J17 (ROUT1), J16 (LOUT2)/ J18 (ROUT2) are available.

7-5-2. Setting of jumper pin

Setting of interface signal of PORTA: AK4114 (U7) is as follows.

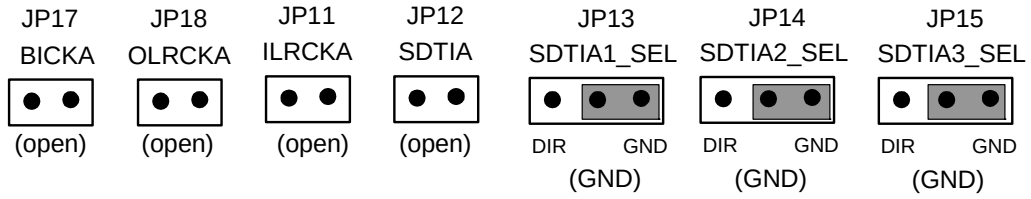


Figure 41. JP17 (BICKA), JP18 (OLRCKA), JP11 (ILRCKA), JP12 (SDTIA), JP13 (SDTIA1_SEL), JP14 (SDTIA2_SEL), JP15 (SDTIA3_SEL)

Setting of interface signal of PORTB: AK4114 (U10) is as follows.

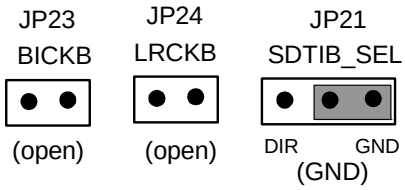


Figure 42. JP23 (BICKB), JP24 (LRCKB), JP21 (SDTIB_SEL)

7-5-3. Setting of DIP switch

SW2 (PORTA_DIR/4683) and SW4 (PORTB_DIR) are “Don’t care”.

7-5-4. Setting of toggle switch

Set SW3 (DIR PORTA) to OFF.
Set SW5 (DIR PORTB) to OFF.
Set SW1 (PDN) to OFF→ON.

7-6. Headphone output

7-6-1. Connection of connector

For headphone output, RCA connector J19 (HPL) and J21 (HPR) or stereo mini jack J20 (HP) are available.

7-6-2. Setting of jumper pin

JP8 (HPL) and JP9 (HPR) control headphone output (RCA connector J19 and J21 or stereo mini jack J20).

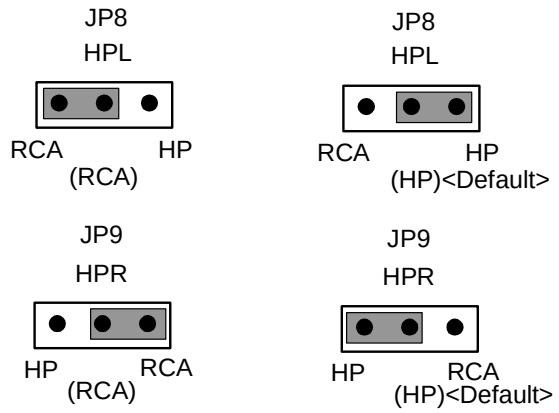


Figure 43. JP8 (HPL), JP9 (HPR)

7-6-3. Setting of DIP switch

In case of evaluation mode of DAC using external DIR, settings of DIP switches: SW2 (PORTA_DIR/4683) and SW4 (PORTB_DIR) should be done following to the setting of the evaluation mode.
In case of evaluation mode of DAC using internal DIR, settings of DIP switches: SW2 (PORTA_DIR/4683) and SW4 (PORTB_DIR) are "Don't care".

7-6-4. Setting of toggle switch

In case of evaluation mode of DAC using external DIR, settings of toggle switches: SW3 (DIR PORTA) and SW5 (DIR PORTB) should be done following to the setting of the evaluation mode.
In case of evaluation mode of DAC using internal DIR, settings of toggle switches: SW3 (DIR PORTA) and SW5 (DIR PORTB) are OFF.
Set SW1 (PDN) to OFF→ON.

8. Power on

8-1. Toggle switch

[SW1] (PDN): Switch for power down reset of AK4589.
Power down reset of AK4589 will be done by setting SW1 (PDN) to "L" once, after power on.
Keep "H" during operation of AK4589.
[SW3] (DIR PORTA): Switch for power down reset of PORTA: AK4114 (U7).
Power down reset of PORTA: AK4114 (U7) will be done by setting SW3 (DIR PORTA) to "L" once, after power on.
Keep "H" during operation of PORTA: AK4114 (U7) .
[SW5] (DIR PORTB): Switch for power down reset of PORTB: AK4114 (U10).
Power down reset of PORTB: AK4114 (U10) will be done by setting SW5 (DIR PORTB) to "L" once, after power on.
Keep "H" during operation of PORTB: AK4114 (U10).

8-2. LED

[LE1] (INT): LED for output of AK4683: INT.
It turns on when output of AK4683: INT is "H".
[LED1] (ERF): LED for output of PORTA: AK4114 (U7): INT0.
It turns on when output of PORTA: AK4114 (U7): INT0 is "H".
[LED2] (ERF): LED for output of PORTB: AK4114 (U10): INT0.
It turns on when output of PORTB: AK4114 (U10): INT0 is "H".

8-3. Reset after power on

AK4683, PORTA: AK4114 (U7), PORTB: AK4114 (U10) should be reset by setting SW1 (PDN), SW3 (DIR PORTA), SW5 (DIR PORTB) to "L" once, after power on.

■ Analog Input Circuit

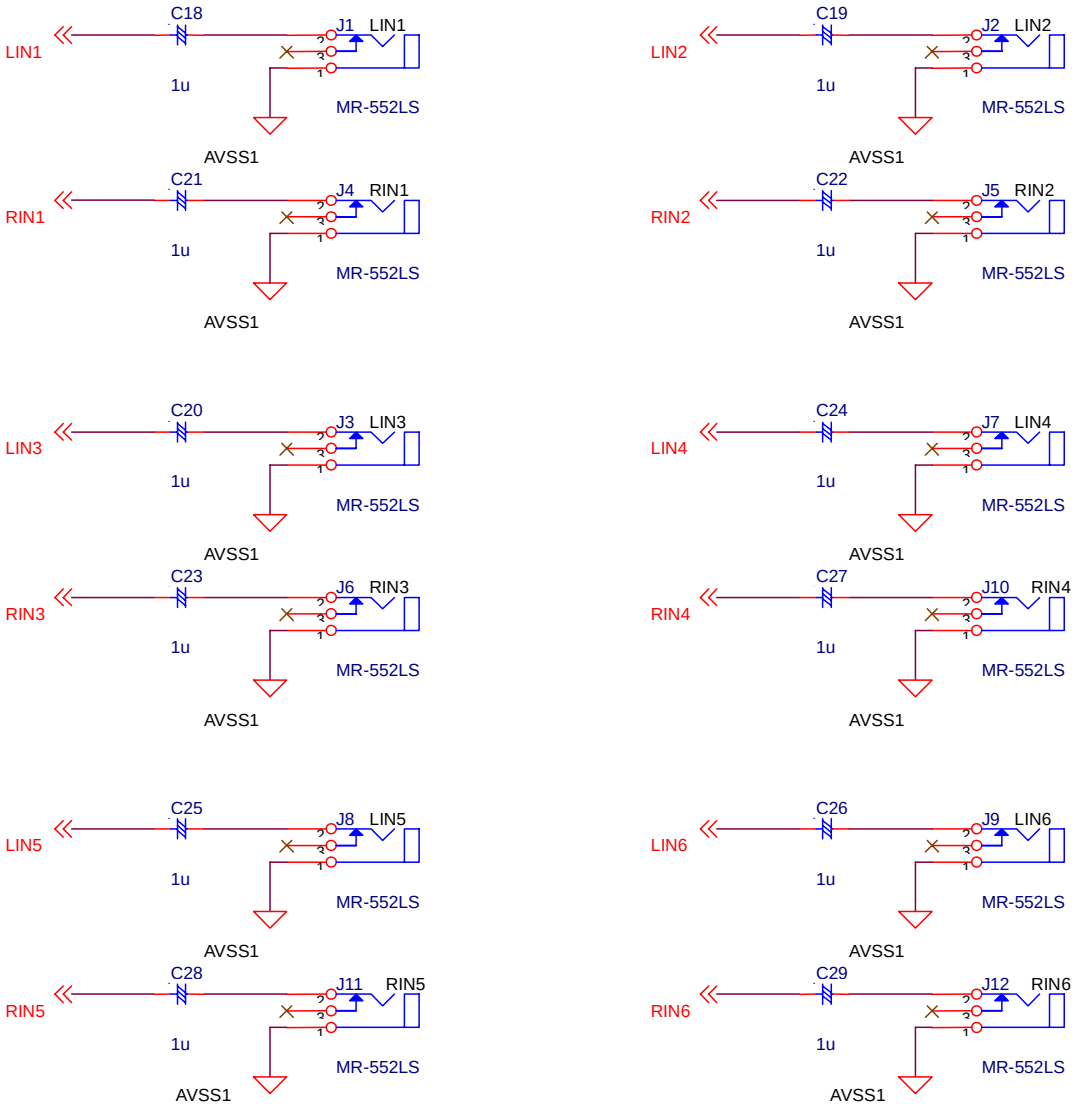


Figure 44. Analog Input Circuit

For analog input, RCA connector: J1 (LIN1)/ J4 (RIN1), J2 (LIN2)/ J5 (RIN2), J3 (LIN3)/ J6 (RIN3), J7 (LIN4)/ J10 (RIN4), J8 (LIN5)/ J11 (RIN5), J9 (LIN6)/ J12 (RIN6) are available to use.
Analog inputs are single-ended and input ranges of each channel are nominally 6.1Vpp@5V.
Input range: AIN is proportional to AVDD1 (AIN=1.22 x AVDD1=1.22 x 5=6.1).

■ Analog Output Circuit

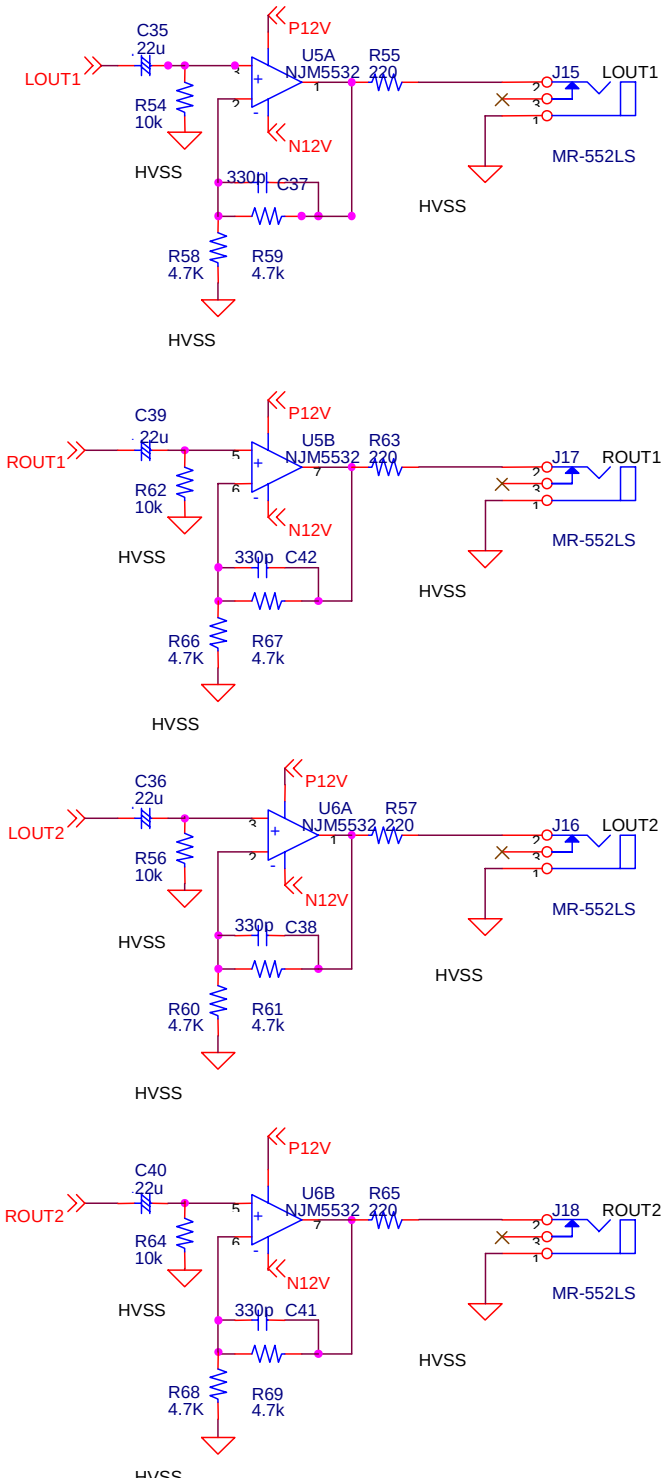


Figure 45. Analog Output Circuit

For analog output, RCA connector: J15 (LOUT1)/ J17 (ROUT1), J16 (LOUT2)/ J18 (ROUT2) are available to use.
Analog outputs are single-ended and output ranges of each channel are nominally 3.0Vpp@5V.
Output range: AOUT is proportional to AVDD2 (AOUT=0.6 x AVDD2=0.6 x 5=3.0).

■ Digital Input Circuit (Internal DIR)

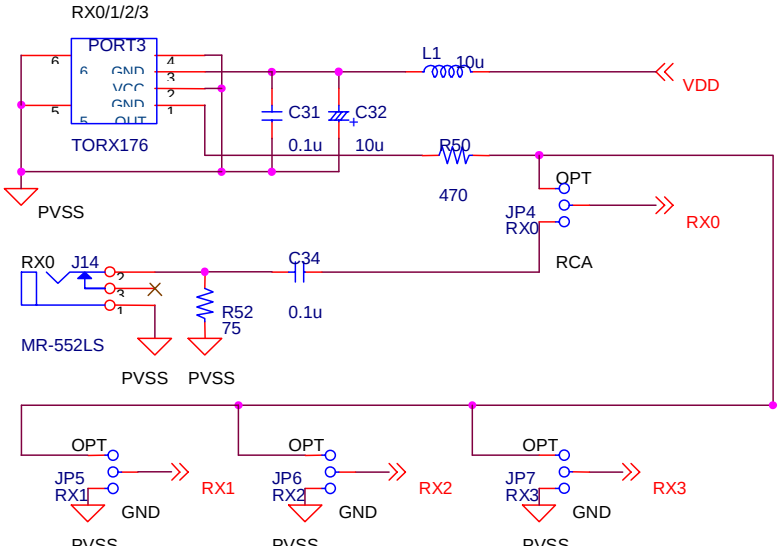


Figure 46. Digital Input Circuit (Internal DIR)

In case of input through RX0, optical connector PORT3 (TORX176) or RCA connector J14 (RX0) are available.
In case of input through RX1, RX2 or RX3, only the optical connector PORT3 is available.
In case of input through RX0, JP4 (RX0) controls digital input (optical connector PORT3 or RCA connector J14).
In case of input through RX1, RX2 or RX3, jumpers JP5 (RX1), JP6 (RX2) or JP7 (RX3) control digital input channels (RX1, RX2 or RX3) from PORT3.
About only input channels, set some of jumpers JP5 (RX1), JP6 (RX2) or JP7 (RX3) to OPT.
About no-input channels, set other of jumpers JP5 (RX1), JP6 (RX2) or JP7 (RX3) to GND.
Digital input: RX0, RX1, RX2 and RX3 is available to select overwriting IPS10 bit of control register (Addr=03H) of AK4683: DIR/DIT part by control software.

■ Digital Input Circuit (External DIR: PORT A)

Figure 47. Digital Input Circuit (External DIR: PORT A)

For digital input, RCA connector: J22 (PORTA_RX0) is available.

■ Digital Input Circuit (External DIR: PORT B)

Figure 48. Digital Input Circuit (External DIR: PORT B)

For digital input, RCA connector: J25 (PORTB_RX0) is available.

■ Digital Output Circuit (Internal DIT)

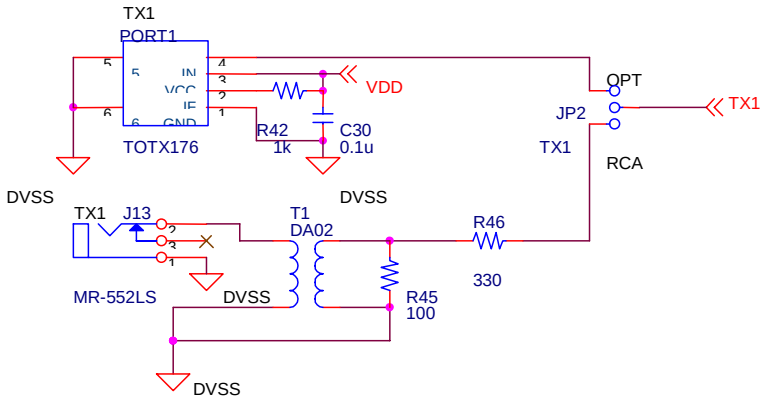


Figure 49. Digital Output Circuit (Internal DIT)

For digital output, optical connector PORT1 (TOTX176) or RCA connector J13 (TX1) are available. JP2 (TX1) controls digital output (optical connector PORT1 or RCA connector J13).

■ Digital Output Circuit (External DIT: PORT A)

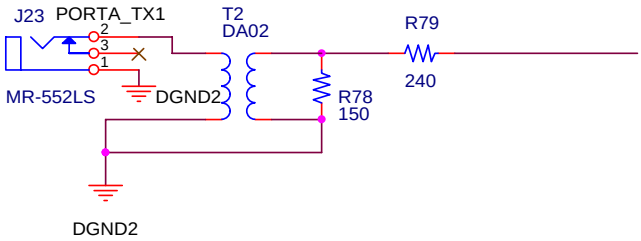


Figure 50. Digital Output Circuit (External DIT: PORT A)

For digital output, RCA connector: J23 (PORTA_TX1) is available.

■ Digital Output Circuit (External DIT: PORT B)

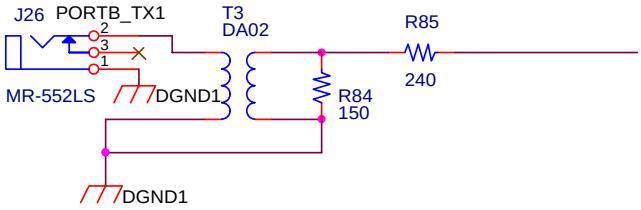


Figure 51. Digital Output Circuit (External DIT: PORT B)

For digital output, RCA connector: J26 (PORTB_TX1) is available.

■ Headphone Output Circuit

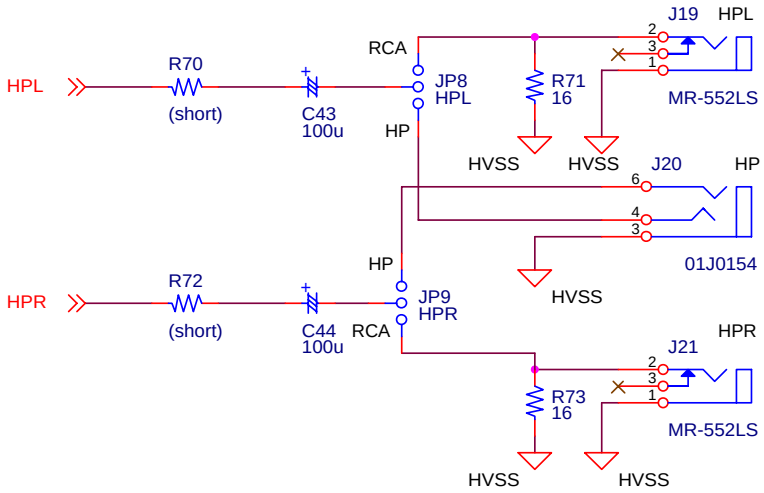


Figure 52. Headphone Output Circuit

For headphone output, RCA connector J19 (HPL), J21 (HPR) or stereo mini jack J20 (HP) are available. JP8 (HPL) and JP9 (HPR) control headphone output (RCA connector J19 and J21 or stereo mini jack J20).

AKD4683 (DIR/DIT) part Control Program operation manual

■ Set-up of evaluation board and control software

(Note) **Control software does not work on Windows NT**
Windows 2000/XP needs an installation of driver.
Windows 95/98/ME does not need an installation of driver.
Please refer to "Installation Manual of Control Software Driver by AKM device control software", about the method of installation of driver.
AK4683 supports the standard-mode I^2C-bus (max: 100kHz), and does not support a fast-mode I^2C-bus system (max: 400kHz).

1. Set up the AKD4683-A according to above mentioned setting.

2. Connect printer port (parallel port) of PC and PORT1 (up-I/F) of AKD4683-A by 10-wire flat cable packed with AKD4683-A. Then take care of the direction of 10pin connector and 10-pin header.

3. Insert the CD-ROM labeled "AKD4683-A Control Program ver. 2.0" into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of "akd4683-a_dir_dit_2.exe", and set up the control program.

5. Then evaluate AK4683 (DIR/DIT) part according to the follows.

(Note) Chip Address of DIR/DIT: CAD1, CAD0 is 0(L), 0(L) fixed. (CAD10=00)

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click Write default button.
3. Then set up the dialog and input data and evaluate AK4683 (DIR/DIT) part.

■ Explanation of each buttons

1. [Write default]: Write default data into all registers.
   Default data is indicated on the register map of all registers.
   Red letter indicates "H" or "1" and blue letter indicates "L" or "0".
   Blank is the part that is not defined in the datasheet.
2. [All Read]: Read data of all registers.
   Read data is indicated on the register map of all register.
   Red letter indicates "H" or "1" and blue letter indicates "L" or "0".
   Blank is the part that is not defined in the datasheet.
3. [Function1]: Set up dialog to write data by keyboard operation.
4. [Write]: It exists on each register corresponding to all registers.
   Set up dialog to write data to each register by mouse operation.
   Set ON/OFF by clicking each bits.
   Click "OK" button if you write input data to register.
   Click "Cancel" button if you don't write input data to register.
5. [Read]: It exists on each register corresponding to some registers.
   Read data from one of each register.
   Read data is indicated on the register map of the register.
   Red letter indicates "H" or "1" and blue letter indicates "L" or "0".
   Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Function1 Dialog]: Dialog to write data by keyboard operation

   Address Input Box: Input address of register which data should be written into, in 2 figures of hexadecimal.
   Data Input Box: Input data which should be written into the register, in 2 figures of hexadecimal.
   Click “OK” button, if you write input data into register.
   Click “Cancel” button, if you don’t write input data into register.

2. [Write Dialog]: Dialog to write data by mouse operation

   There are dialogs corresponding to each register.
   Click the “Write” button corresponding to each register to set up the dialog.
   If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.
   Click “OK” button, if you write input data into register.
   Click “Cancel” button, if you don’t write input data into register.

■ Indication of data

Input data is indicated on the register map.
Red letter indicates “H” or “1” and blue letter indicates “L” or “0”.
Blank is the part that is not defined in the datasheet.

■ Attention on the operation

Input data to all boxes when you have set up “Function1 dialog”. An “attention dialog” is indicated if you input data or address that is not specified in the datasheet or you click “OK” button before you input data. In that case set up the dialog and input data once more again. These operations does not need if you click “Cancel” button or check the check box.

AK4683 (ADC/DAC) part Control Program Operation Manual

■ Set-up of evaluation board and control software

(Note) Control software does not work on Windows NT.
Windows 2000/XP needs an installation of driver.
Windows 95/98/ME does not need an installation of driver.
Please refer to "Installation Manual of Control Software Driver by AKM device control software", about the method of installation of driver.
AK4683 supports the standard-mode I^2C-bus (max: 100kHz), and does not support a fast-mode I^2C-bus system (max: 400kHz).

1. Set up the AKD4683-A according to above mentioned setting.

2. Connect printer port (parallel port) of PC and PORT1 (up-I/F) of AKD4683-A by 10-wire flat cable packed with AKD4683-A. Then take care of **the direction of 10pin connector and 10-pin header.**

3. Insert the CD-ROM-disk labeled "AKD4683-A Control Program ver. 2.0" into the CD-ROM-disk drive.

4. Access the CD-ROM-disk drive and double-click the icon of "akd4683-a_adc_dac_2.exe" and set up the control program.

5. Then evaluate AK4683 (ADC/DAC) part according to the followings.

(Note) Chip Address of ADC/DAC: CAD1, CAD0 is 1(H), 0(L) fixed, (CAD10=10)
Register of ADC/DAC part is "write only", and it cannot be read.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above
2. Click Write default button.
3. Then set up the dialog and input data and evaluate AK4683 (ADC/DAC) part.

■ Explanation of each buttons

1. [Write default]: Write default data into all register.
   Default data is indicated on the register map of all registers.
   Red letter indicates "H" or "1" and blue letter indicates "L" or "0".
   Blank is the part that is not defined in the datasheet.
2. [Function1]: Set up dialog to write data by keyboard operation.
3. [Function2]: Set up dialog to write data by keyboard operation.
4. [Write]: It exists corresponding to each register.
   Set up dialog to write data to each register by mouse operation.
   Set ON/OFF by clicking each bits.
   Click "OK" button if you write input data into register.
   Click "Cancel" button if you don't write input data into register.

■ Explanation of each dialog

1. [Function1 Dialog]: Dialog to write data by keyboard operation

   Address Input Box: Input address of register which data should be written into, in 2 figures of hexadecimal.
   Data Input Box: Input data which should be written into the register, in 2 figures of hexadecimal.
   Click "OK" button, if you write input data into register.
   Click "Cancel" button, if you don't write input data into register.

2. [Function2 Dialog]: Dialog to evaluate ATT of LIN/RIN/LOUT1/ROUT1/LOUT2/ROUT2 Volume Control.

   This dialog corresponds to addr:0CH, 0DH, 0EH, 0FH, 10H, and 11H.
   Address Input Box: Input address of register which data should be written into, in 2 figures of hexadecimal.
   Start Data Input Box: Input first data (start data) which should be written into the register, in 2 figures of hexadecimal.
   End Data Input Box: Input last data (end data) which should be written into the register, in 2 figures of hexadecimal.
   Interval Input Box: Input time distance (interval time) between write and write when data is written into the register, in decimal. Unit of time is ms.
   Step Input Box: Input value distance (step of data) between data and data when data is written into the register, in decimal.
   Mode Select Check Box: Select mode of data flow, "Data returns to start data after data reached end data." Or "Data flow is end when data reached end data."
   Set mode of data flow by checked or no into this check box.
   When you checked into this: Data returns to start data after data reached end data.
   When you did not check into this: Data flow is end when data reached end data.
   [Example when you checked into this] Start Data = 00, End Data = 09
   Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00
   [Example when you did not check into this] Start Data = 00, End Data = 09
   Data flow: 00 01 02 03 04 05 06 07 08 09
   Click "OK" button, if you write input data into register.
   Click "Cancel" button, if you don't write input data into register.

3. [Write Dialog]: Dialog to write data by mouse operation

   There are dialogs corresponding to each register.
   Click the "Write" button corresponding to each register to set up the dialog.
   If you check the check box, data becomes "H" or "1". If not, "L" or "0".
   Click "OK" button, if you write input data into register.
   Click "Cancel" button, if you don't write input data into register.

■ Indication of data

Input data is indicated on the register map.
Red letter indicates "H" or "1" and blue letter indicates "L" or "0".
Blank is the part that is not defined in the datasheet.

■ Attention on the operation

Input data to all boxes when you have set up "Function1 dialog" or "Function2 dialog". An "attention dialog" is indicated if you input data or address that is not specified in the datasheet or you click "OK" button before you input data. In that case set up the dialog and input data once more again. These operations does not need if you click "Cancel" button or check the check box.

Measure Result

1) ADC part

[Measurement condition]

- Measurement unit: Audio Precision System two Cascade (AP2)
- MCLK : 256fs (fs=48kHz), 256fs (fs=96kHz)
- BICK : 64fs
- fs : 48kHz, 96kHz
- BW : 20Hz~20kHz (fs=48kHz), 20Hz~40kHz (fs=96kHz)
- Bit : 24bit
- Power Supply : AVDD=PVDD=DVDD=5V, TVDD=3.3V
- Interface : Internal DIT (fs=48kHz, 96kHz)
- Temperature : Room Temp

fs=48kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, -0.5dB	20kLPF	93.1 dB
DR	1kHz, -60dB	20kLPF	97.1 dB
DR	1kHz, -60dB	20kLPF, A-weighted	100.6 dB
S/N	No signal	20kLPF	98.2 dB
S/N	No signal	20kLPF, A-weighted	101.1 dB

fs=96kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, -0.5dB	fs/2	92.0 dB
DR	1kHz, -60dB	fs/2	96.3 dB
DR	1kHz, -60dB	20kLPF, A-weighted	102.7 dB
S/N	No signal	fs/2	96.3 dB
S/N	No signal	20kLPF, A-weighted	102.9 dB

2) DAC part

[Measurement condition]

- Measurement unit: Audio Precision System two Cascade (AP2)
- MCLK : 256fs (fs=48kHz, 96kHz), 128fs (fs=192kHz)
- BICK : 64fs
- fs : 48kHz, 96kHz, 192kHz
- BW : 20Hz~20kHz (fs=48kHz), 20Hz~40kHz (fs=96kHz), 20Hz~40kHz (fs=192kHz)
- Resolution : 24bit
- Power Supply : AVDD=PVDD=DVDD=5V, TVDD=3.3V
- Interface : Internal DIR (48kHz, 96kHz, 192kHz)
- Temperature : Room Temp

fs=48kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, 0dB	20kLPF	94.3 dB
DR	1kHz, -60dB	20kLPF	105.0 dB
DR	1kHz, -60dB	22kLPF, A-weighted	105.6 dB
S/N	“0” data	20kLPF	103.4 dB
S/N	“0” data	22kLPF, A-weighted	106.0 dB

fs=96kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, 0dB	40kLPF	92.3 dB
DR	1kHz, -60dB	40kLPF	102.0 dB
DR	1kHz, -60dB	22kLPF, A-weighted	105.6 dB
S/N	“0” data	40kLPF	101.0 dB
S/N	“0” data	22kLPF, A-weighted	106.2 dB

fs=192kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, 0dB	40kLPF	88.8 dB
DR	1kHz, -60dB	40kLPF	102.5 dB
DR	1kHz, -60dB	22kLPF, A-weighted	106.2 dB
S/N	“0” data	40kLPF	101.3 dB
S/N	“0” data	22kLPF, A-weighted	106.2 dB

■ Plots

1) ADC

[Measurement condition]

- Measurement Unit : Audio Precision System two Cascade
- MCLK : 256fs(fs=48kHz), 256fs(fs=96kHz)
- BICK : 64fs
- fs : 48kHz, 96kHz
- BW : 20Hz~20kHz (fs=48kHz), 40Hz~40kHz (fs=96kHz)
- Resolution : 24bit
- Power Supply : AVDD=PVDD=DVDD=5V, TVDD=3.3V
- Interface : Internal DIT (fs=48kHz, 96kHz)
- Temperatur : Room Temp

fs=48kHz

Figure 7. FFT (Input Frequency =1kHz, Input Level =-0.5dBFS)
Figure 8. FFT (Input Frequency =1kHz, Input Level =-60dBFS)
Figure 9. FFT (noise floor)
Figure 10. THD+N vs Input Level (Input Frequency =1kHz)
Figure 11. THD+N vs Input Frequency (Input Level=-0.5dBFS)
Figure 12. Linearity (Input Frequency =1kHz)
Figure 13. Frequency Response (Input Level=-0.5dBFS)
Figure 14. Cross-talk (Input Level=-0.5dBFS)

fs=96kHz

Figure 15. FFT (Input Frequency =1kHz, Input Level =-0.5dBFS)
Figure 16. FFT (Input Frequency =1kHz, Input Level =-60dBFS)
Figure 17. FFT (noise floor)
Figure 18. THD+N vs Input Level (Input Frequency =1kHz)
Figure 19. THD+N vs fin (Input Level=-0.5dBFS)
Figure 20. Linearity (Input Frequency =1kHz)
Figure 21. Frequency Response (Input Level=-0.5dBFS)
Figure 22. Cross-talk (Input Level=-0.5dBFS)

FFT point=16384, Avg=8, Window=Equirriple

2) DAC

[Measurement Condition]

- Measurement Unit : Audio Precision System two Cascade
- MCLK : 256fs(fs=48kHz, 96kHz), 128fs(fs=192kHz)
- BICK : 64fs
- fs : 48kHz, 96kHz, 192kHz
- BW : 20Hz~20kHz (fs=48kHz), 40Hz~40kHz (fs=96kHz), 40Hz~80kHz (fs=192kHz)
- Resolution : 24bit
- Power Supply : AVDD=PVDD=DVDD=5V, TVDD=3.3V
- Interface : Internal DIR (48kHz, 96kHz, 192kHz)
- Temperature : Room Temp

fs=48kHz

Figure 23. FFT (Input Frequency =1kHz, Input Level =0dBFS)
Figure 24. FFT (Input Frequency =1kHz, Input Level =-60dBFS)
Figure 25. FFT (noise floor)
Figure 26. FFT (out-of-band noise)
Figure 27. THD+N vs Input Level (Input Frequency =1kHz)
Figure 28. THD+N vs Input Frequency (Input Level=0dBFS)
Figure 29. Linearity (Input Frequency =1kHz)
Figure 30. Frequency Response (Input Level=0dBFS)
Figure 31. Cross-talk (Input Level=0dBFS)

fs=96kHz

Figure 32. FFT (Input Frequency =1kHz, Input Level =0dBFS)
Figure 33. FFT (Input Frequency =1kHz, Input Level =-60dBFS)
Figure 34. FFT (noise floor)
Figure 35. FFT (out-of-band noise)
Figure 36. THD+N vs Input Level (Input Frequency =1kHz)
Figure 37. THD+N vs fin (Input Level=0dBFS)
Figure 38. Linearity (Input Frequency =1kHz)
Figure 39. Frequency Response (Input Level=0dBFS)
Figure 40. Cross-talk (Input Level=0dBFS)

fs=192kHz

Figure 41. FFT (Input Frequency =1kHz, Input Level =0dBFS)
Figure 42. FFT (Input Frequency =1kHz, Input Level =-60dBFS)
Figure 43. FFT (noise floor)
Figure 44. FFT (out-of-band noise)
Figure 45. THD+N vs Input Level (Input Frequency =1kHz)
Figure 46. THD+N vs fin (Input Level=0dBFS)
Figure 47. Linearity (Input Frequency =1kHz)
Figure 48. Frequency Response (Input Level=0dBFS)
Figure 49. Cross-talk (Input Level=0dBFS)

FFT point=16384, Avg=8, Window=Equirriple

1.ADC

(ADC fs=48kHz)

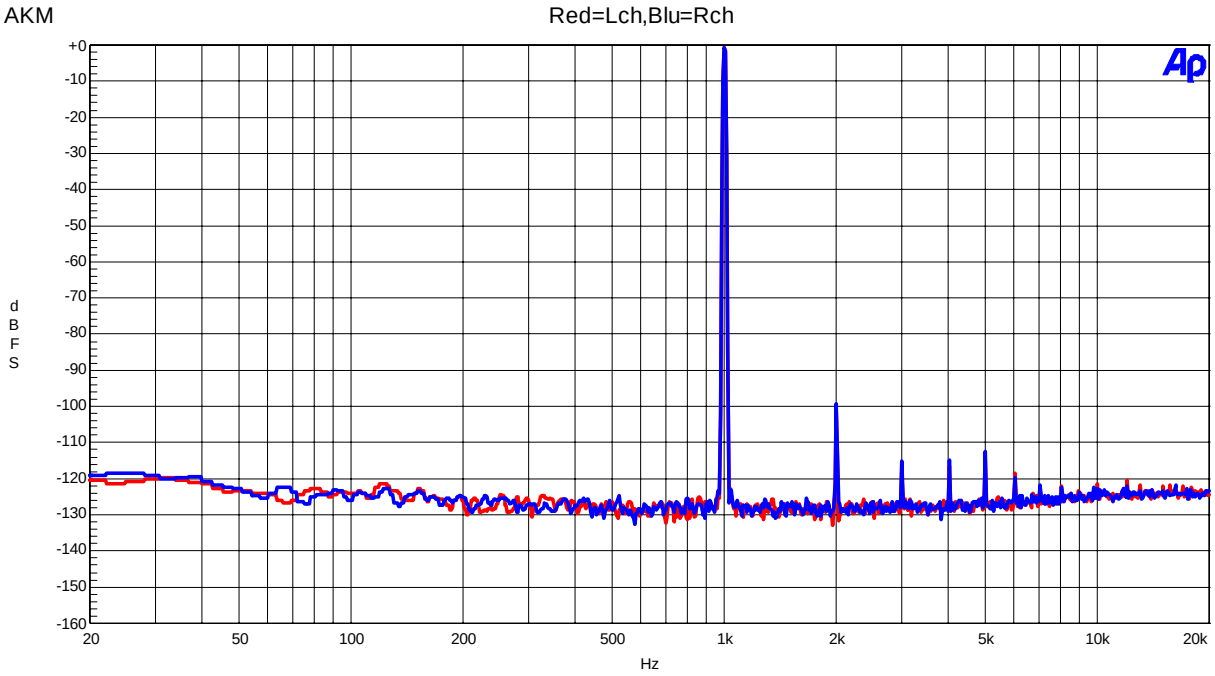


Figure 1. FFT(Input Frequency=1kHz,Input Level=-0.5dBFS)

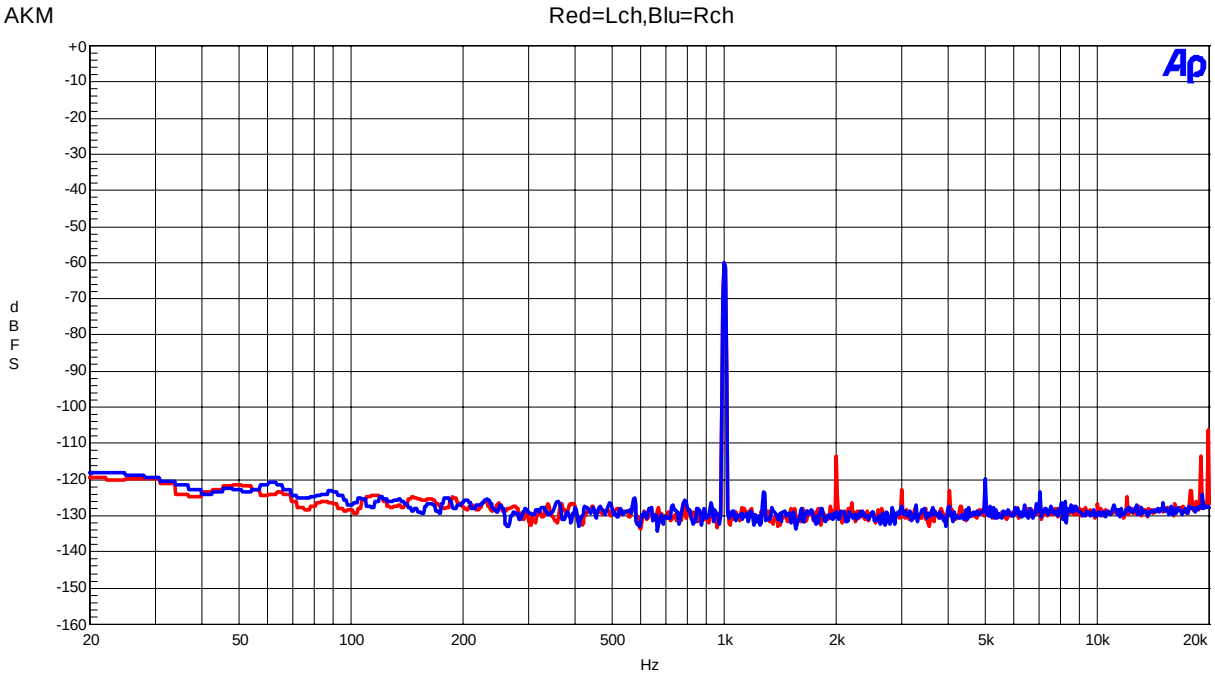


Figure 2. FFT(Input Frequency=1kHz,Input Level=-60dBFS)

(ADC fs=48kHz)

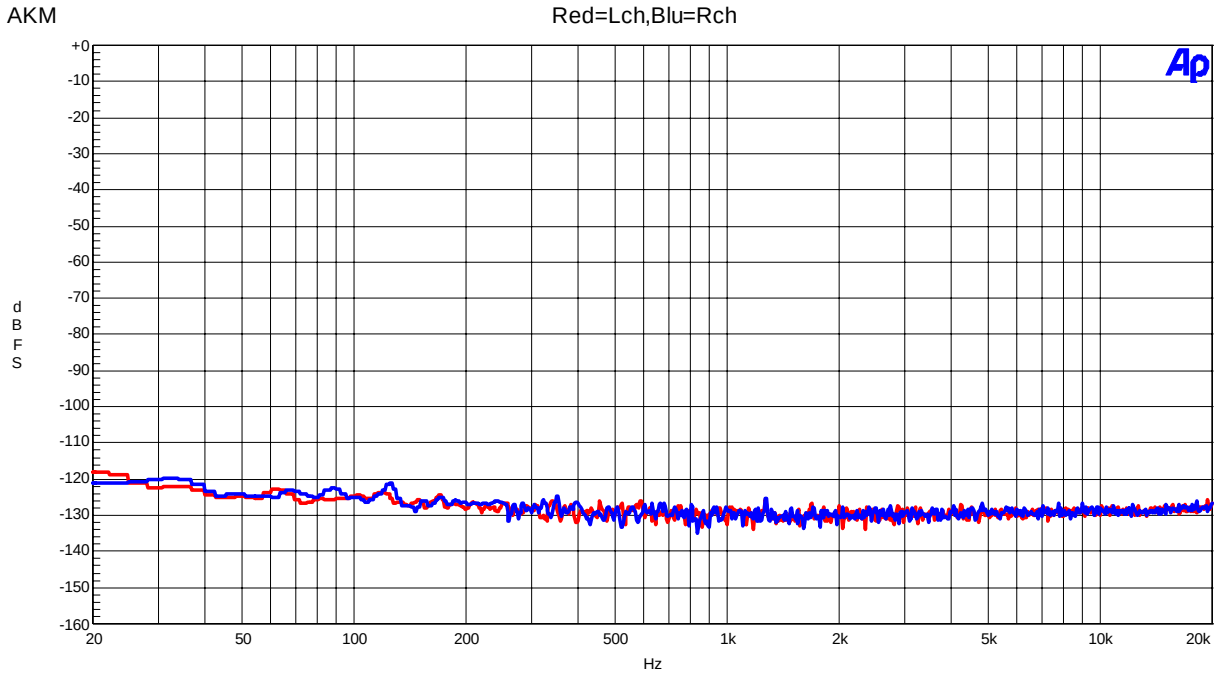


Figure 3. FFT(noise floor)

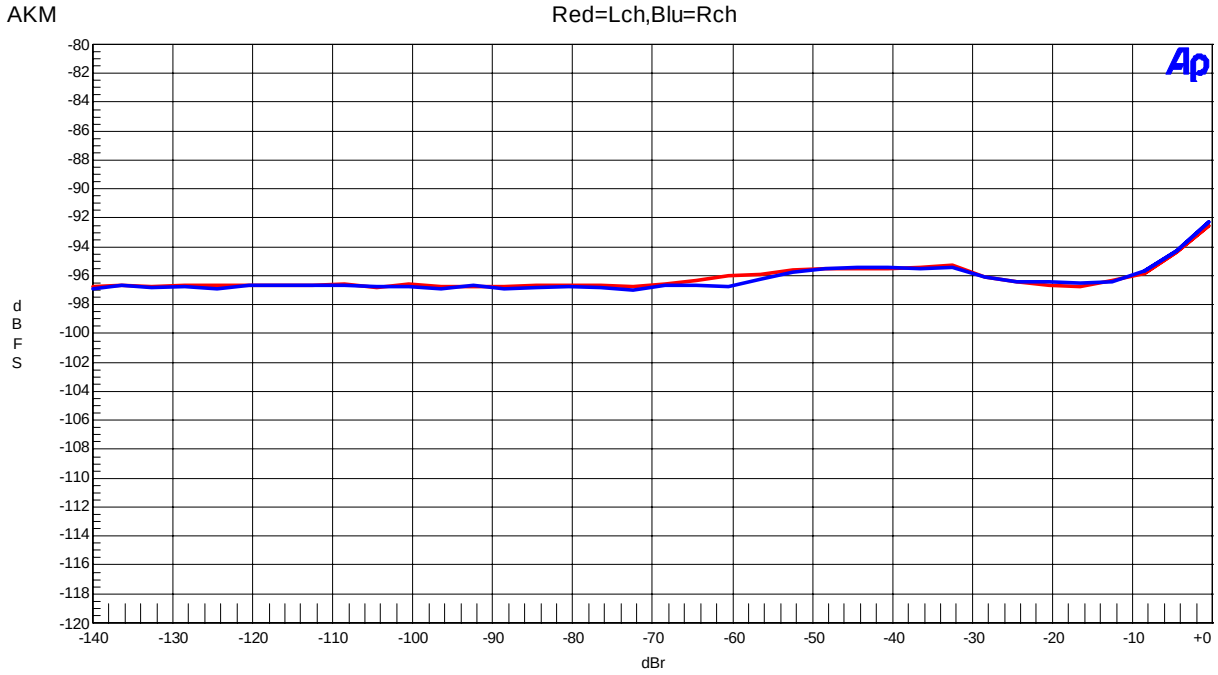


Figure 4. THD + N vs Input Level(Input Frequency=1kHz)

(ADC fs=48kHz)

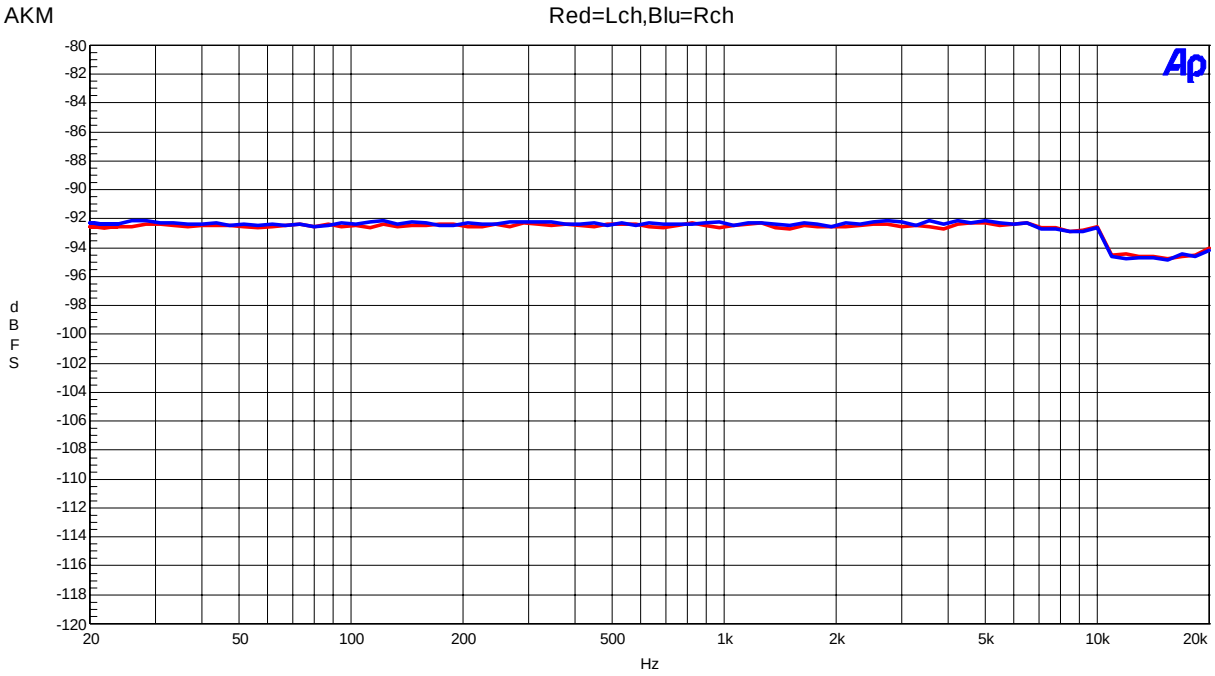


Figure 5. THD + N vs Input Frequency (Input Level=-0.5dBFS)

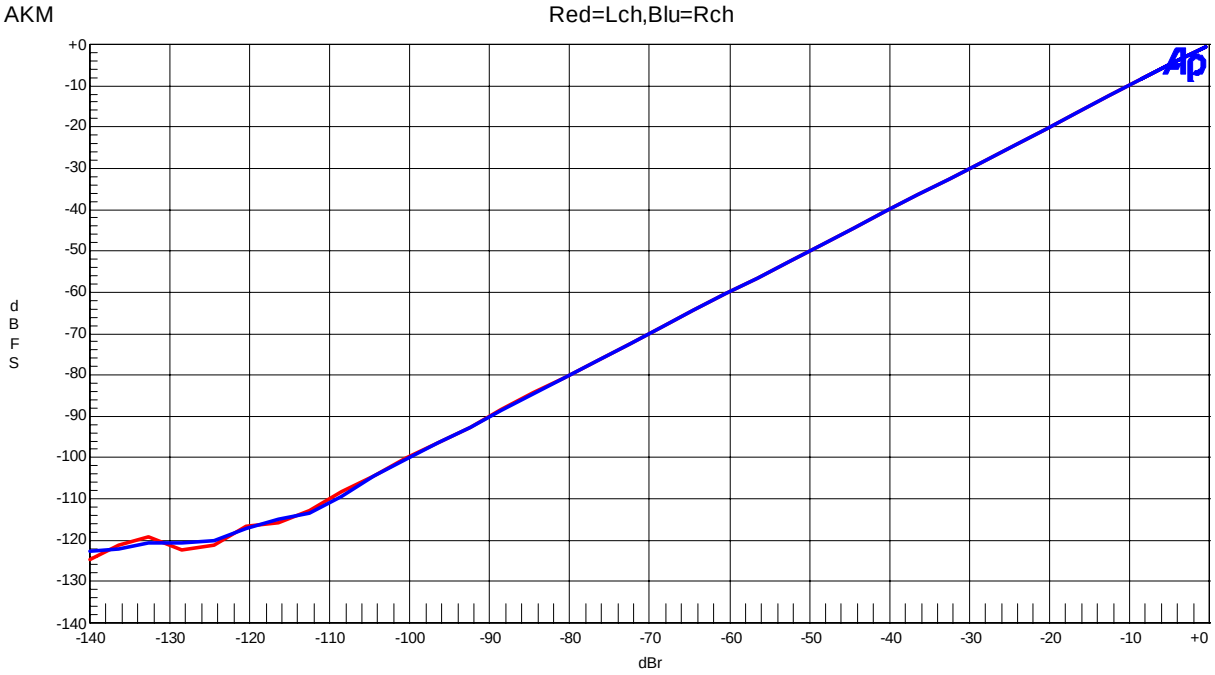


Figure 6. Linearity (Input Frequency=1kHz)

(ADC fs=48kHz)

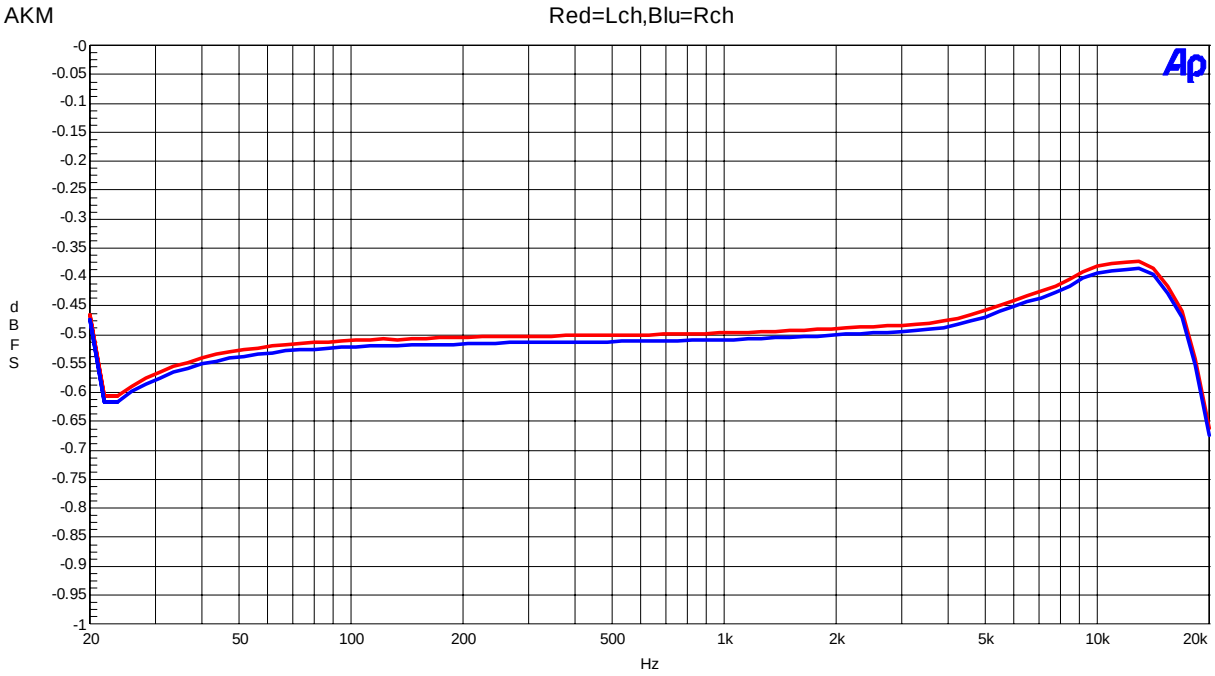


Figure 7. Frequency Response (Input Level=-0.5dBFS)

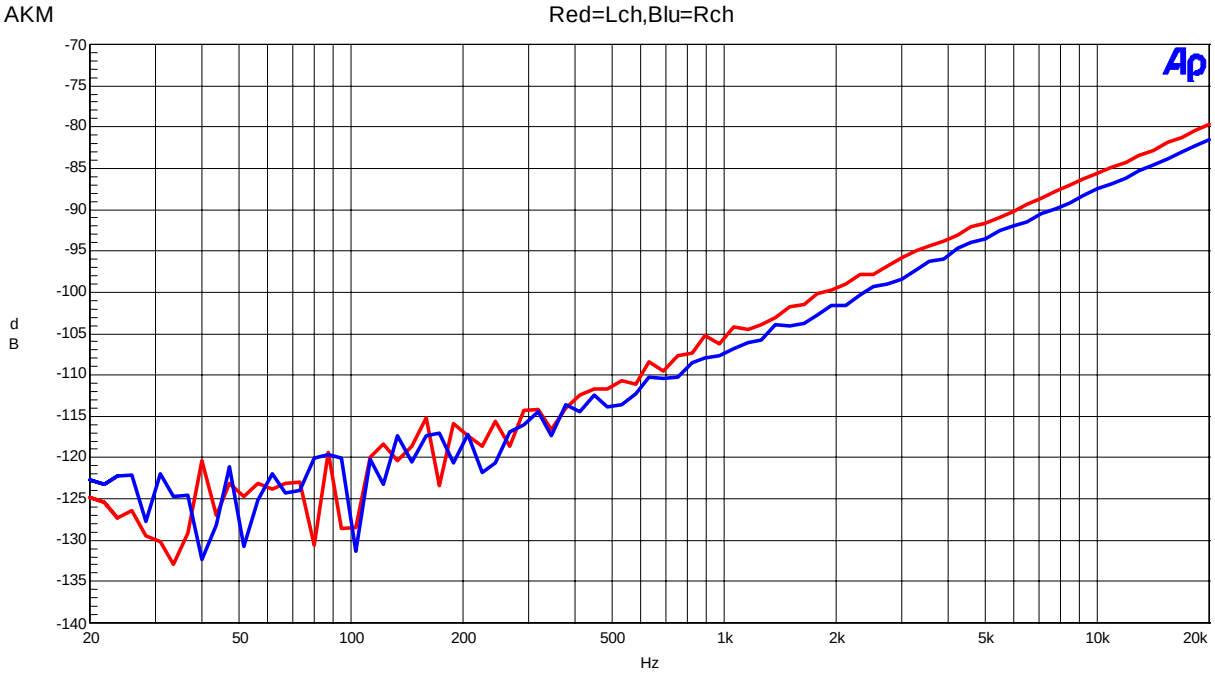


Figure 8. Crosstalk (Input Level=-0.5dBFS)

(ADC fs=96kHz)

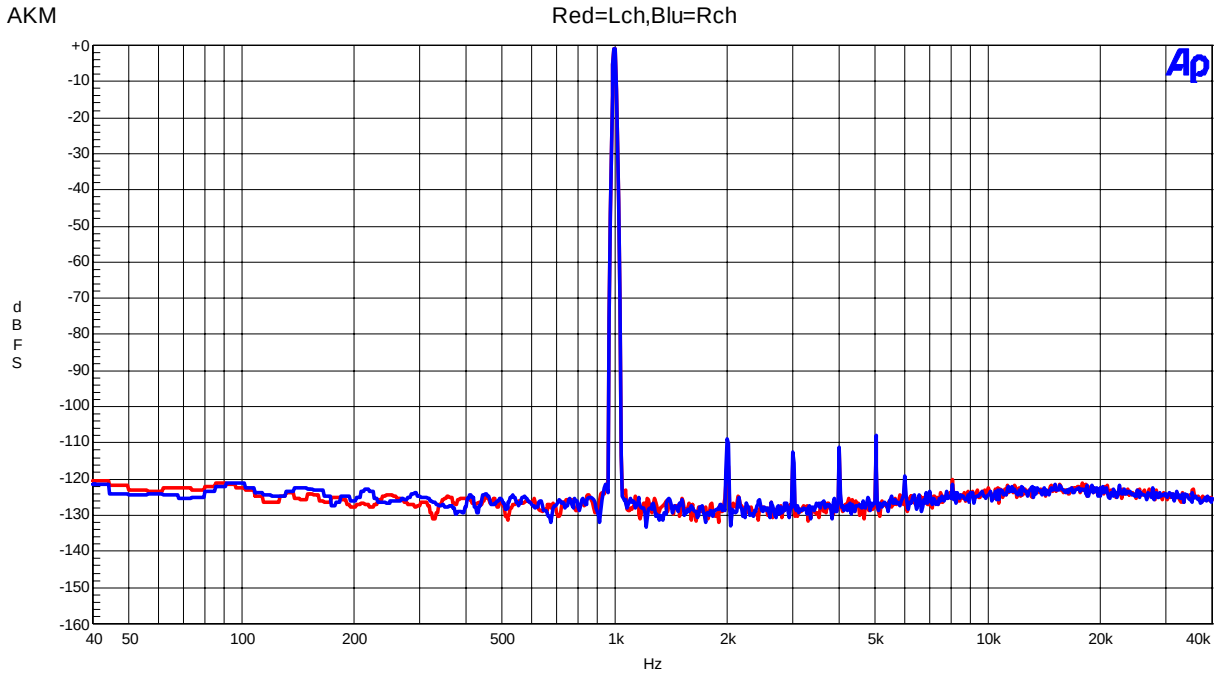


Figure 9. FFT(Input Frequency=1kHz,Input Level=-0.5dBFS)

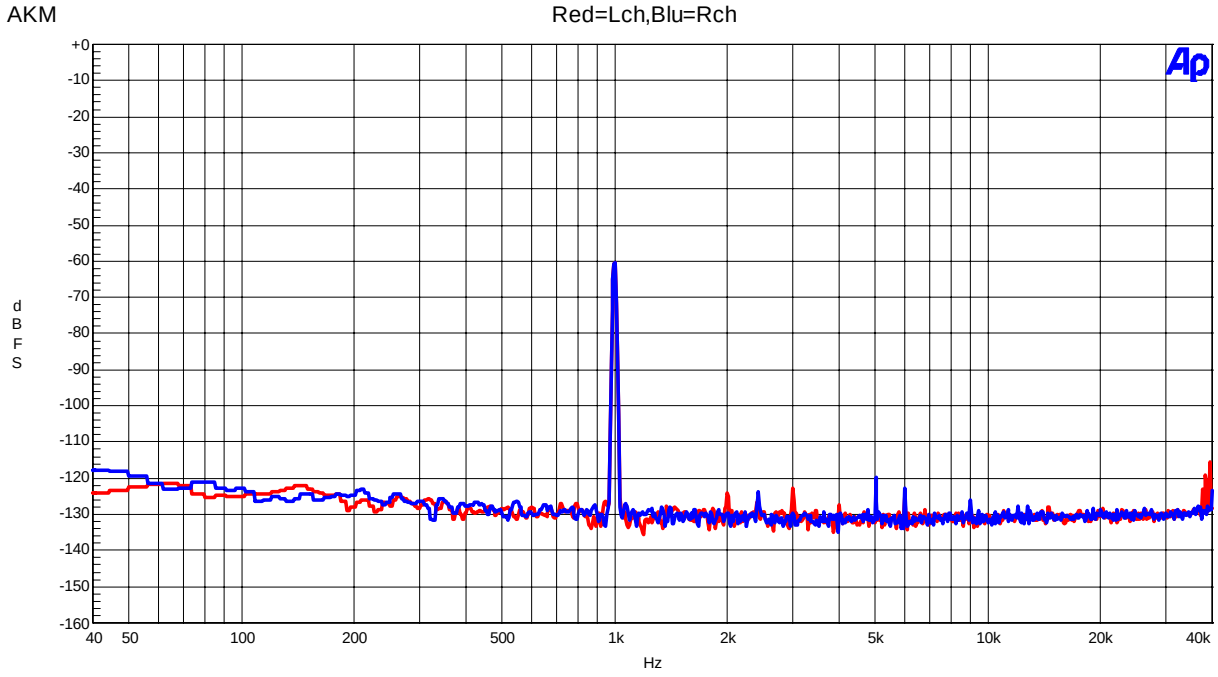


Figure 10. FFT(Input Frequency=1kHz,Input Level=-60dBFS)

(ADC fs=96kHz)

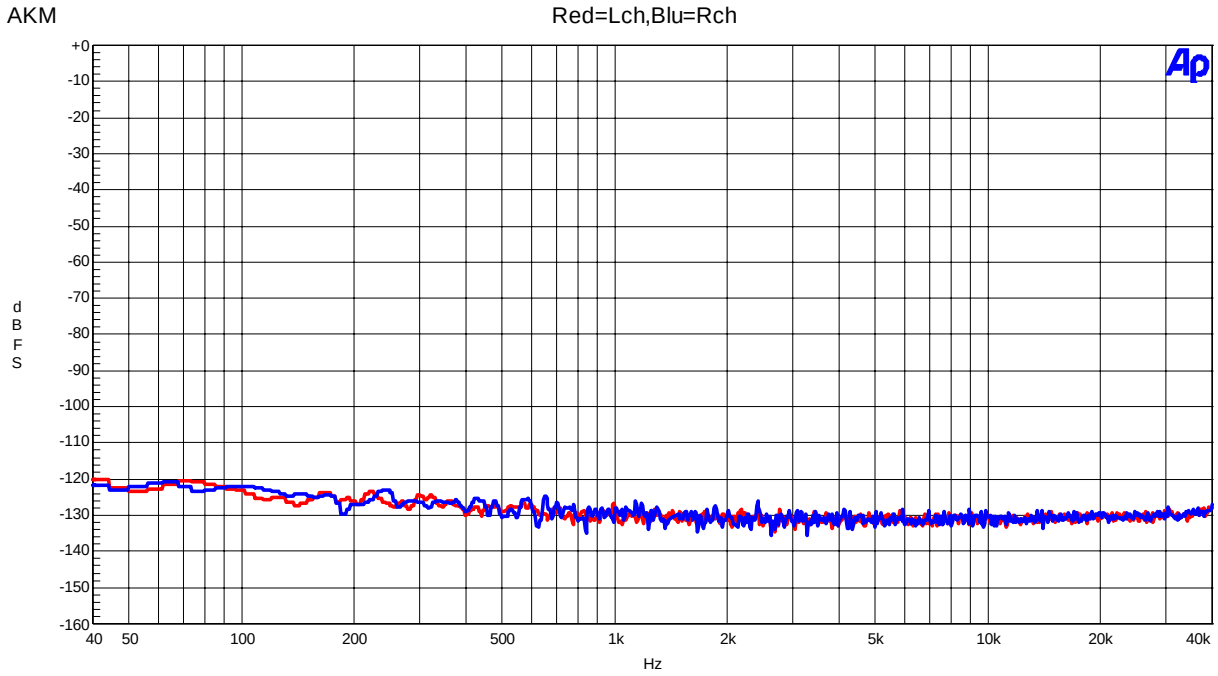


Figure 11. FFT(Noise floor)

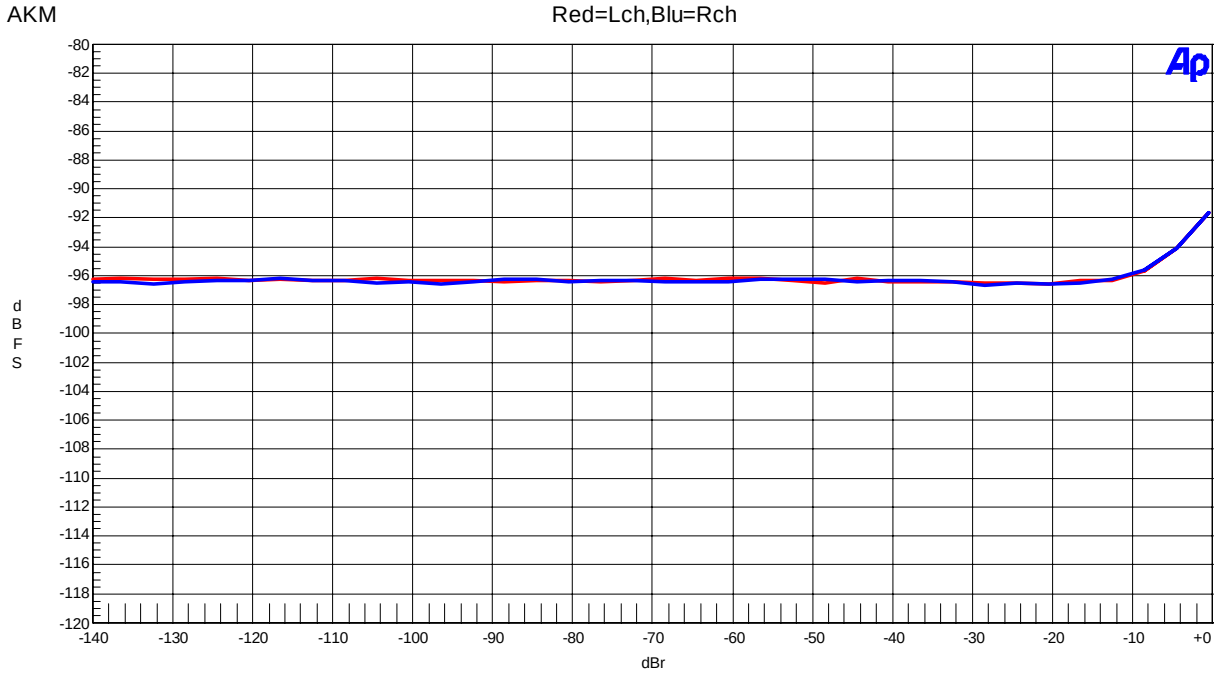


Figure 12. THD + N vs Input Level (Input Frequency=1kHz)

(ADC fs=96kHz)

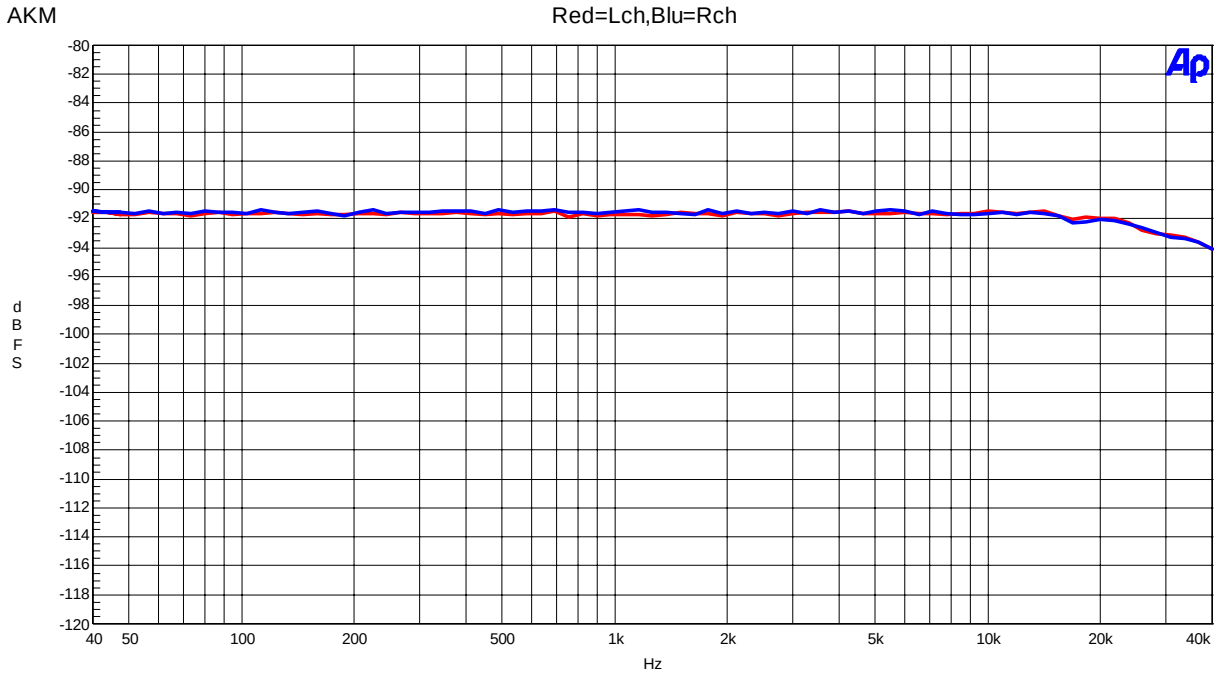


Figure 13. THD + N vs Input Frequency (Input Level=-0.5dBFS)

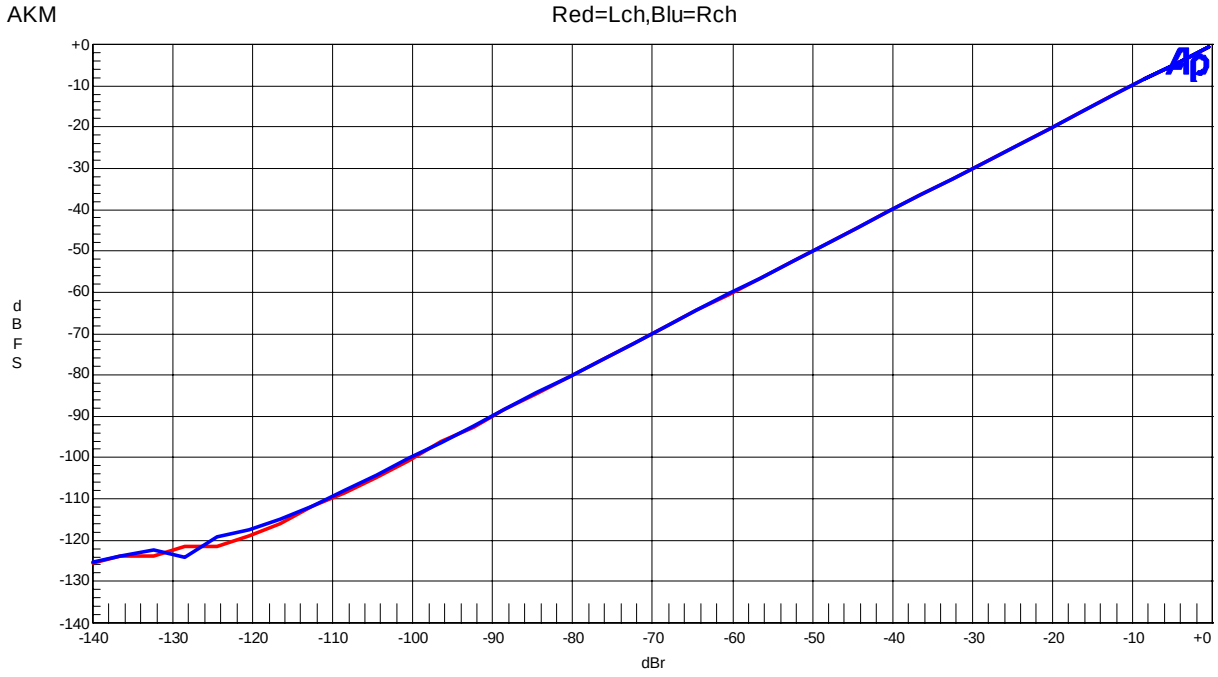


Figure 14. Linearity (Input Frequency=1kHz)

(ADC fs=96kHz)

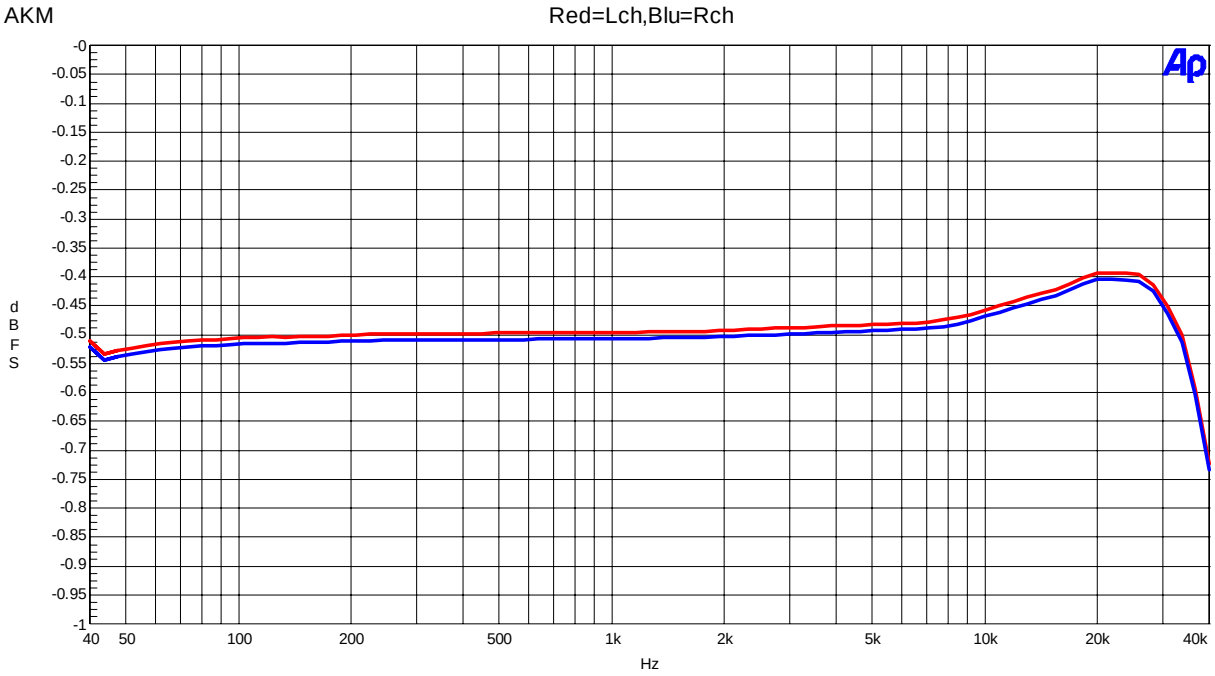


Figure 15. Frequency Response (Input Level=-0.5dBFS)

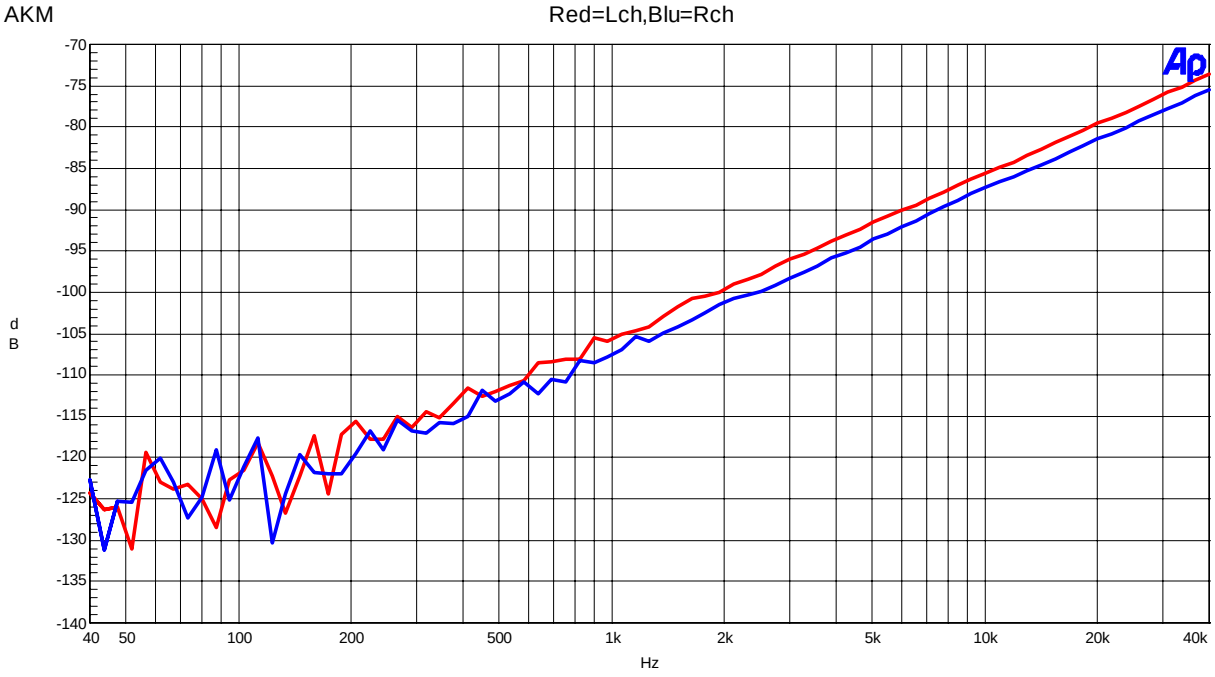


Figure 16. Crosstalk (Input Level=-0.5dBFS)

2.DAC

(DAC fs=48kHz)

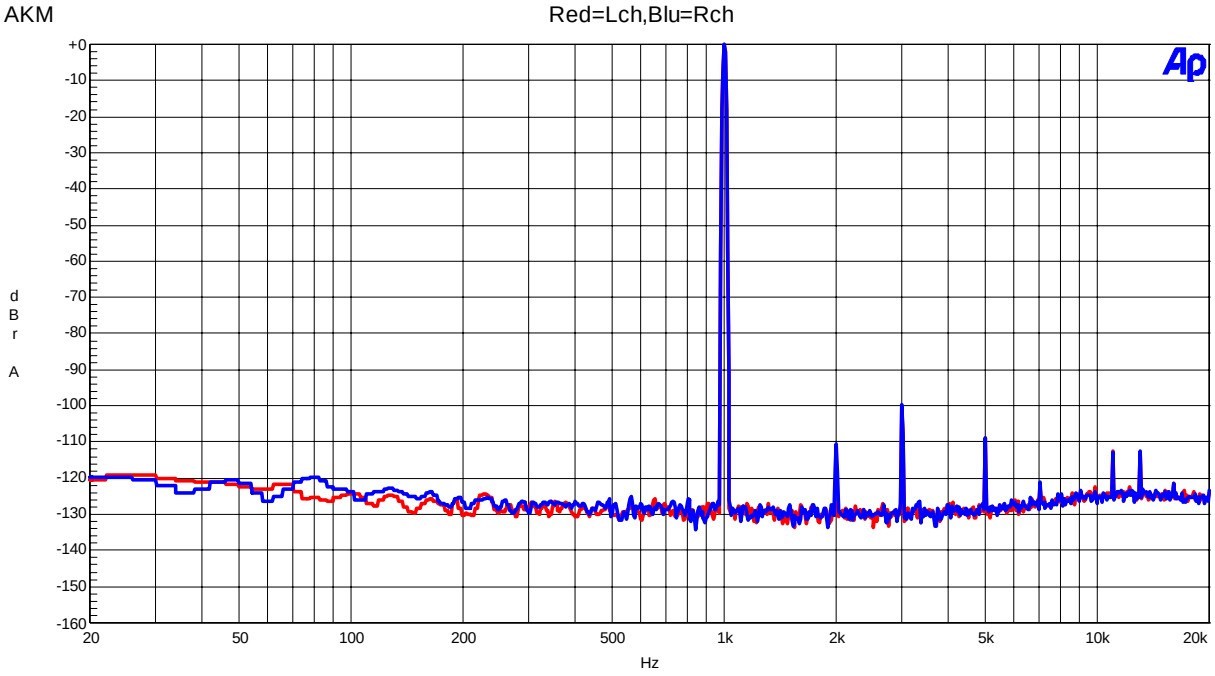


Figure 17. FFT(Input Frequency=1kHz, Input Level=0dBFS)

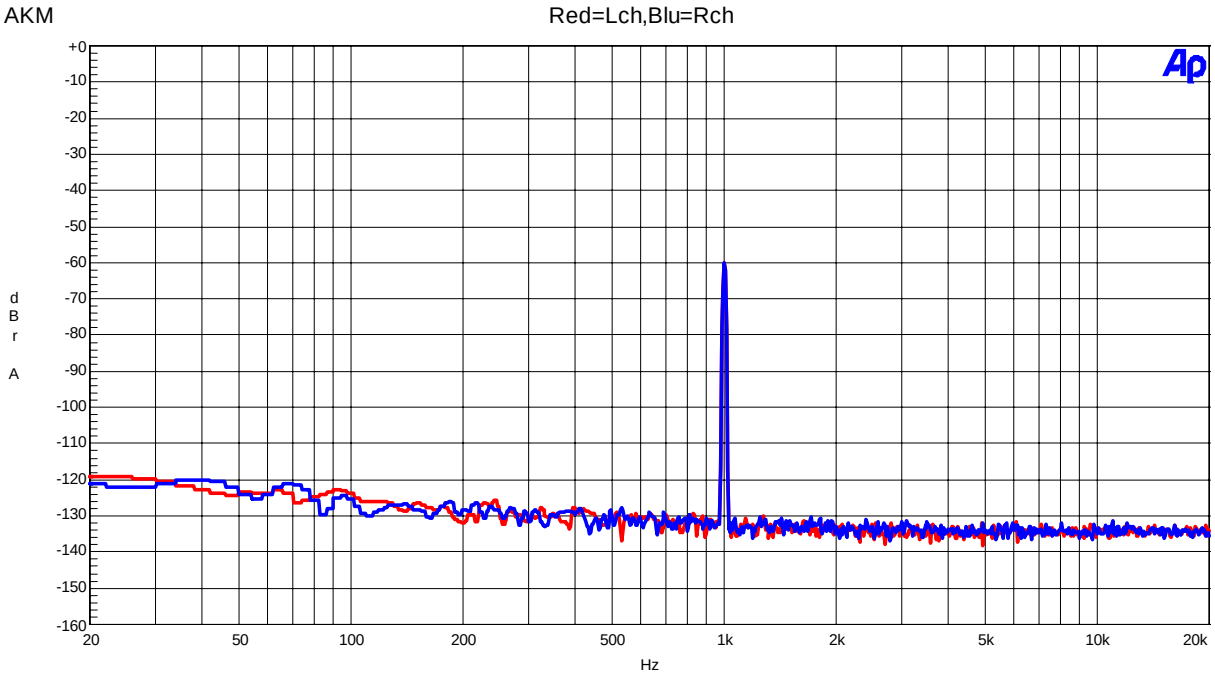


Figure 18. FFT(Input Frequency=1kHz, Input Level=-60dBFS)

(DAC fs=48kHz)

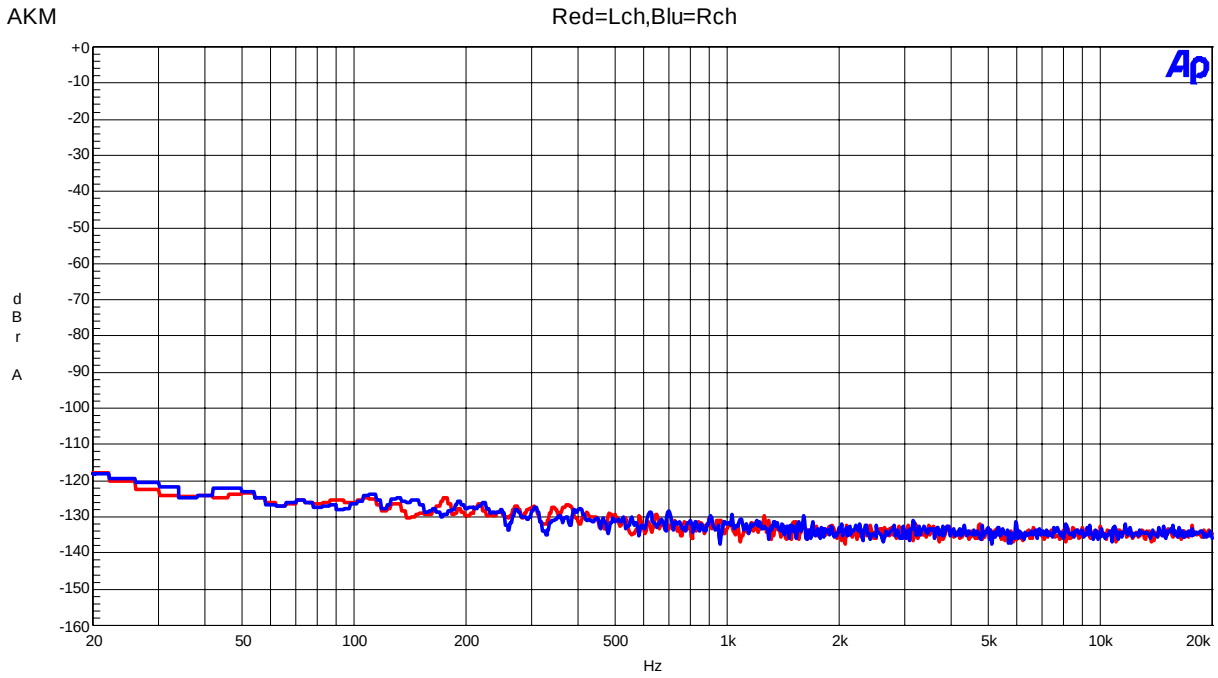


Figure 19. FFT(noise floor)

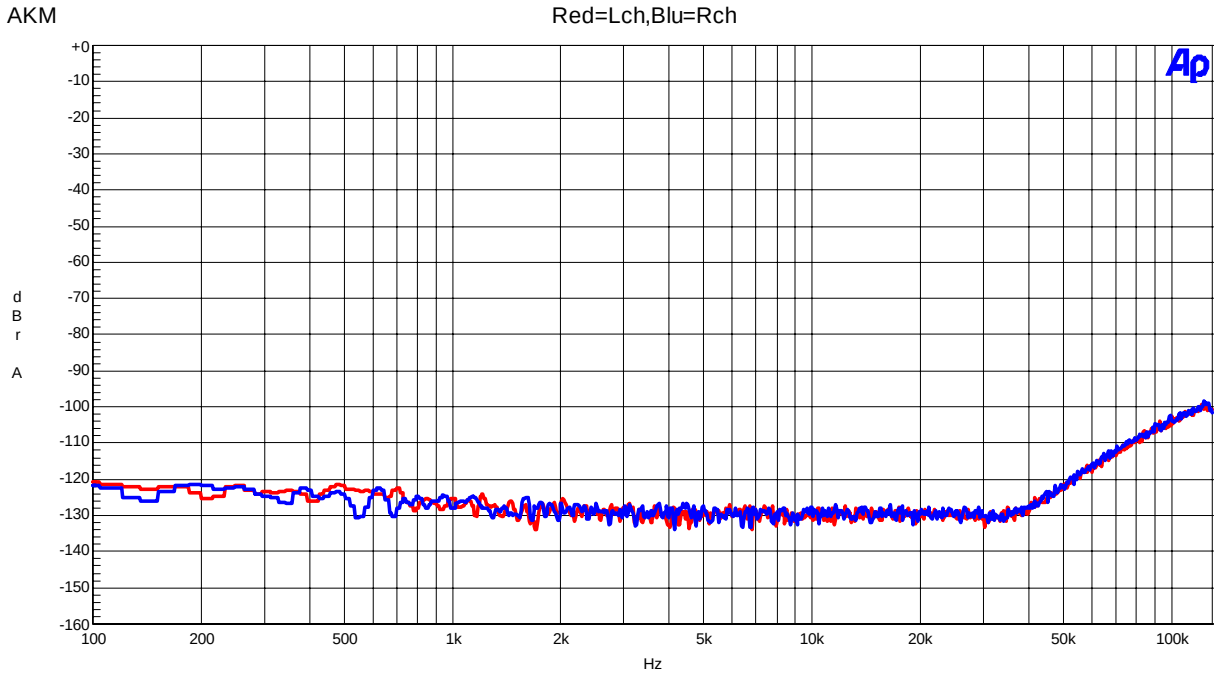


Figure 20. FFT(out-of-band noise)

(DAC fs=48kHz)

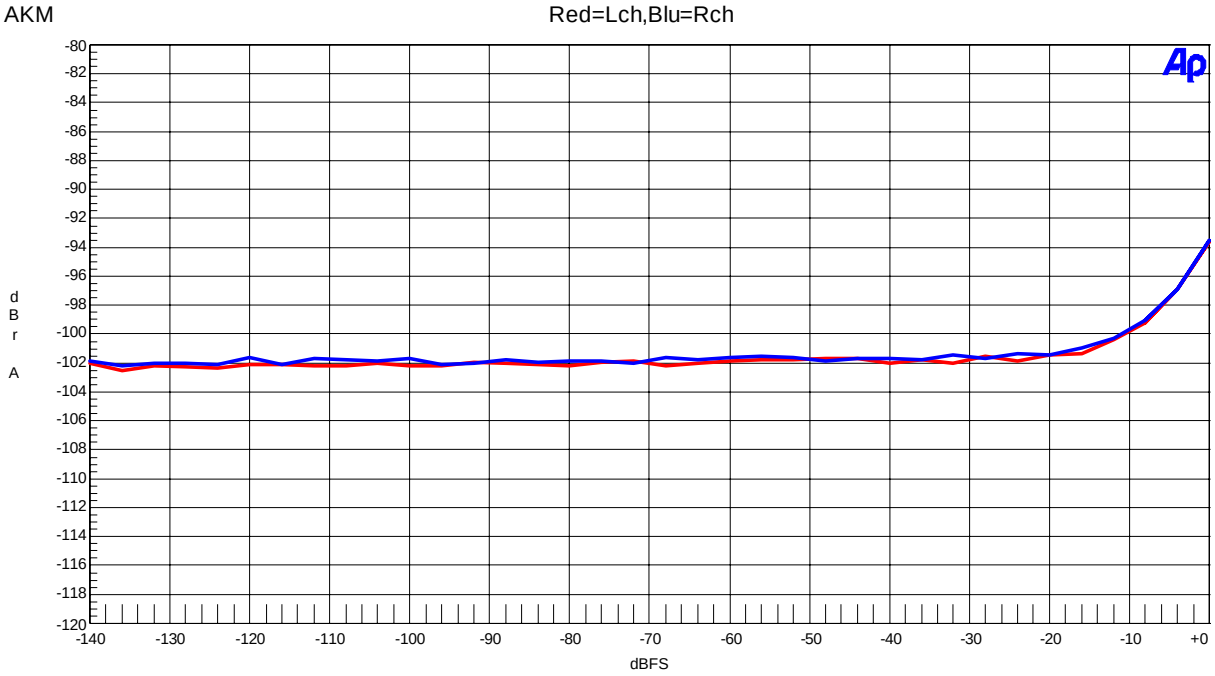


Figure 21. THD+N vs Input Level (Input Frequency=1kHz)

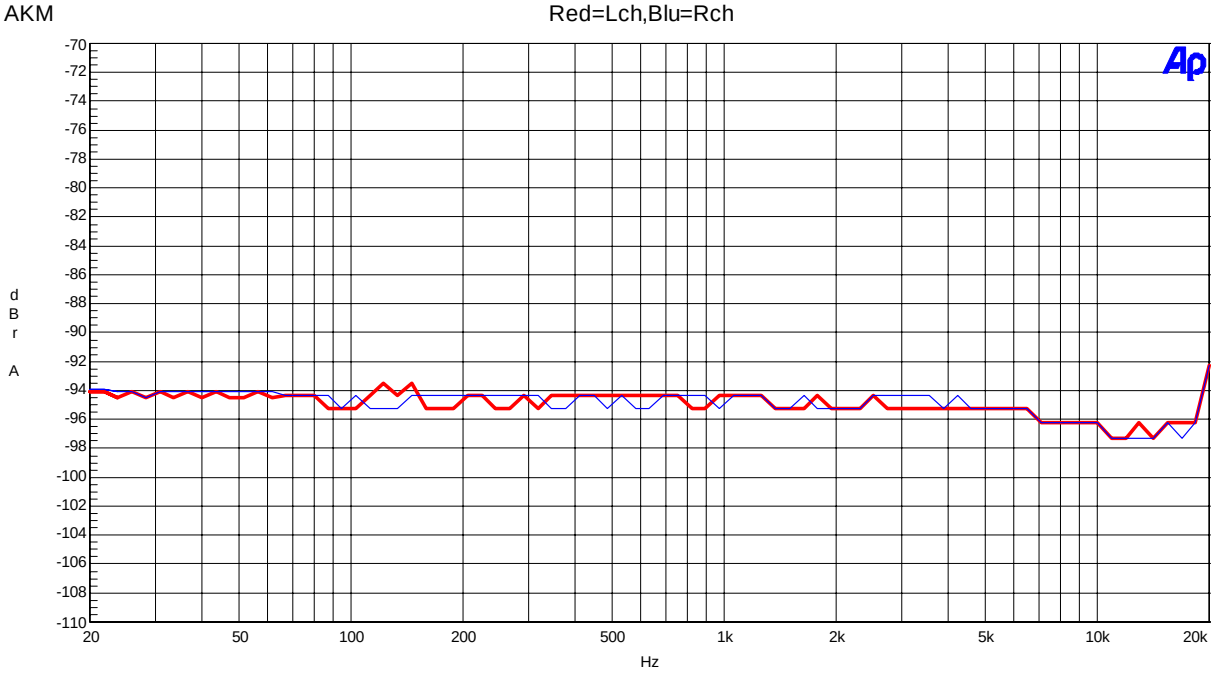


Figure 22. THD+N vs Input Frequency (Input Level=0dBFS)

(DAC fs=48kHz)

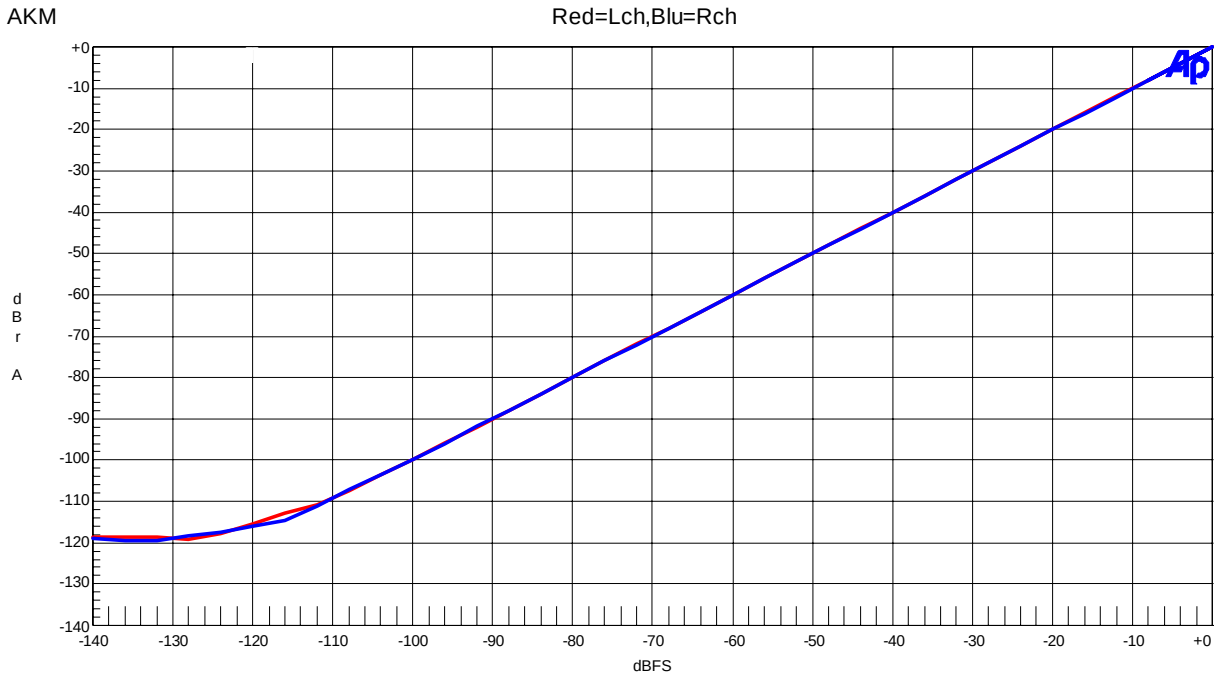


Figure 23. Linearity (Input Frequency=1kHz)

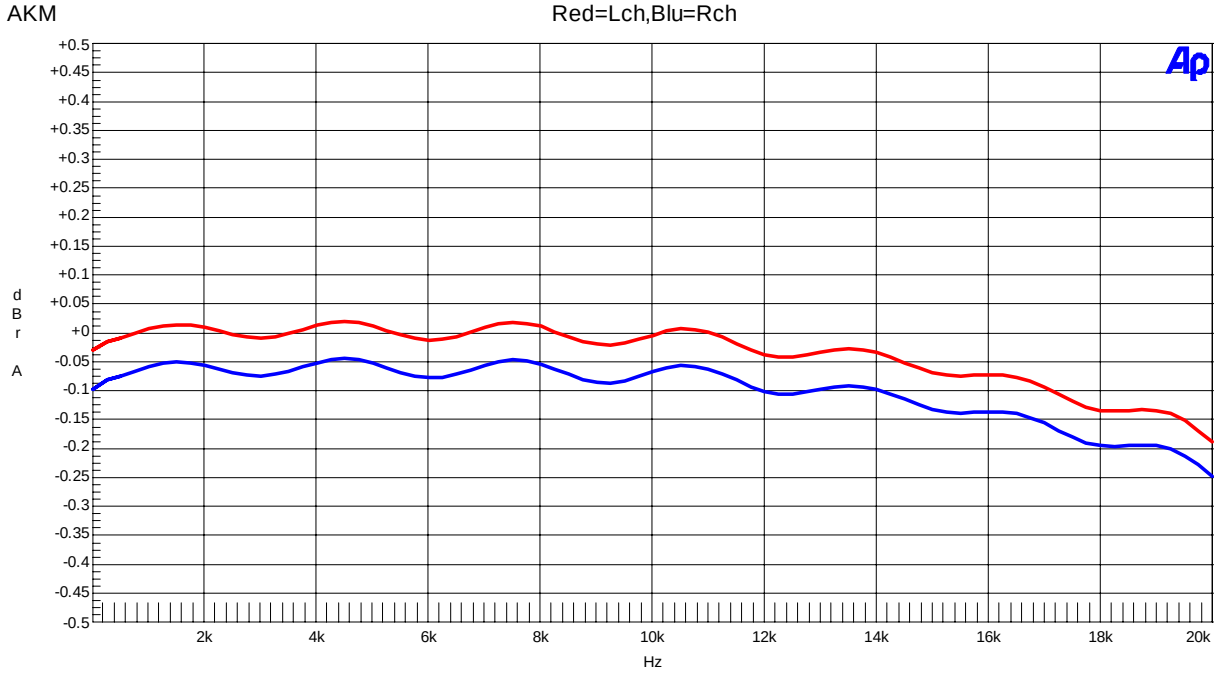


Figure 24. Frequency Response (Input Level=0dBFS)

(DAC fs=48kHz)

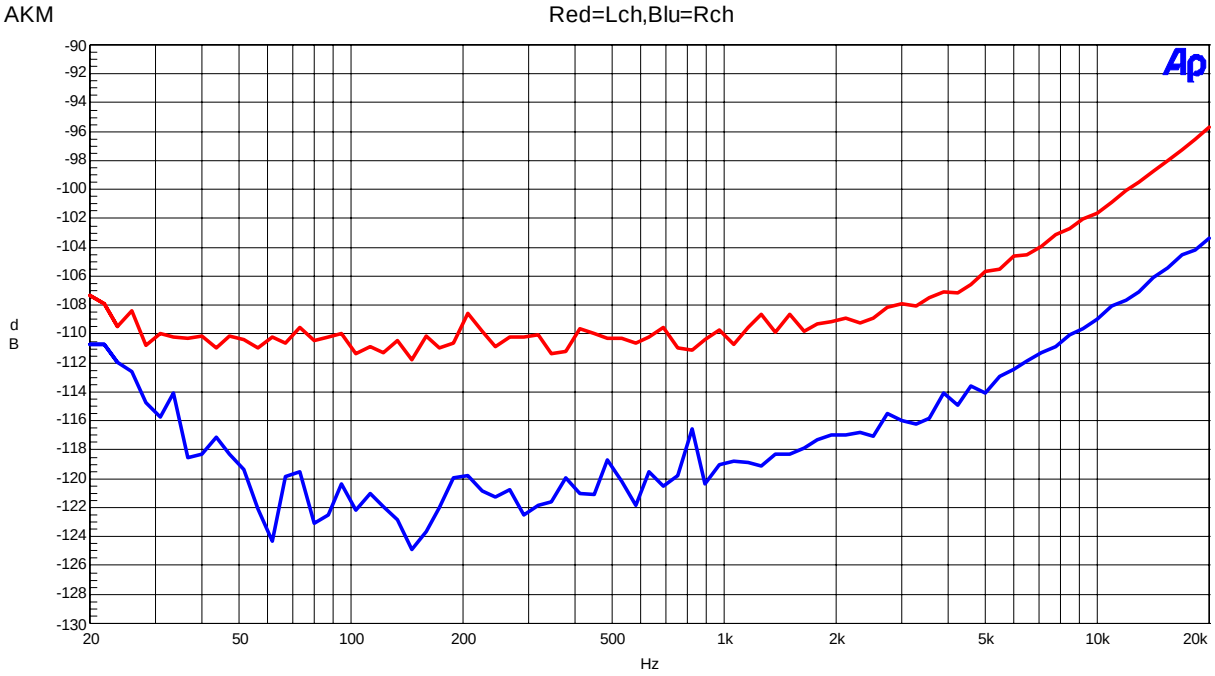


Figure 25. Cross-talk (Input Level=0dBFS)

(DAC fs=96kHz)

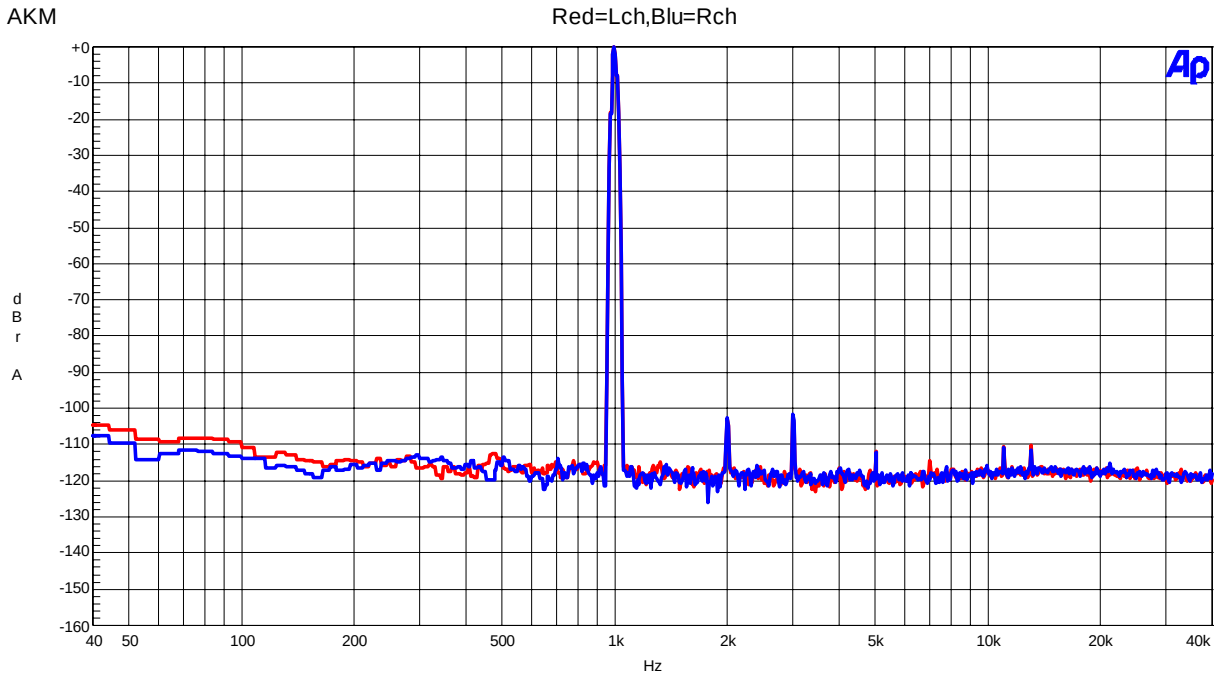


Figure 26. FFT(Input Frequency=1kHz, Input Level=0dBFS)

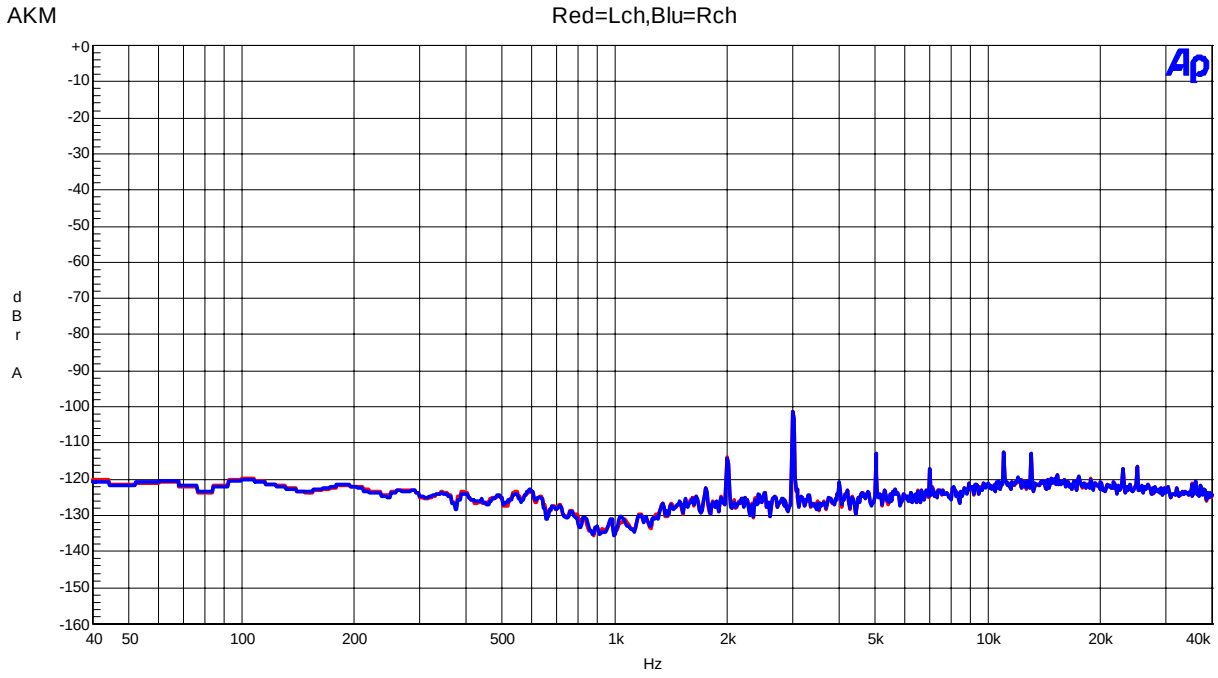


Figure 27. FFT(Input Frequency=1kHz, Input Level=0dBFS,Notch-on)

(DAC fs=96kHz)

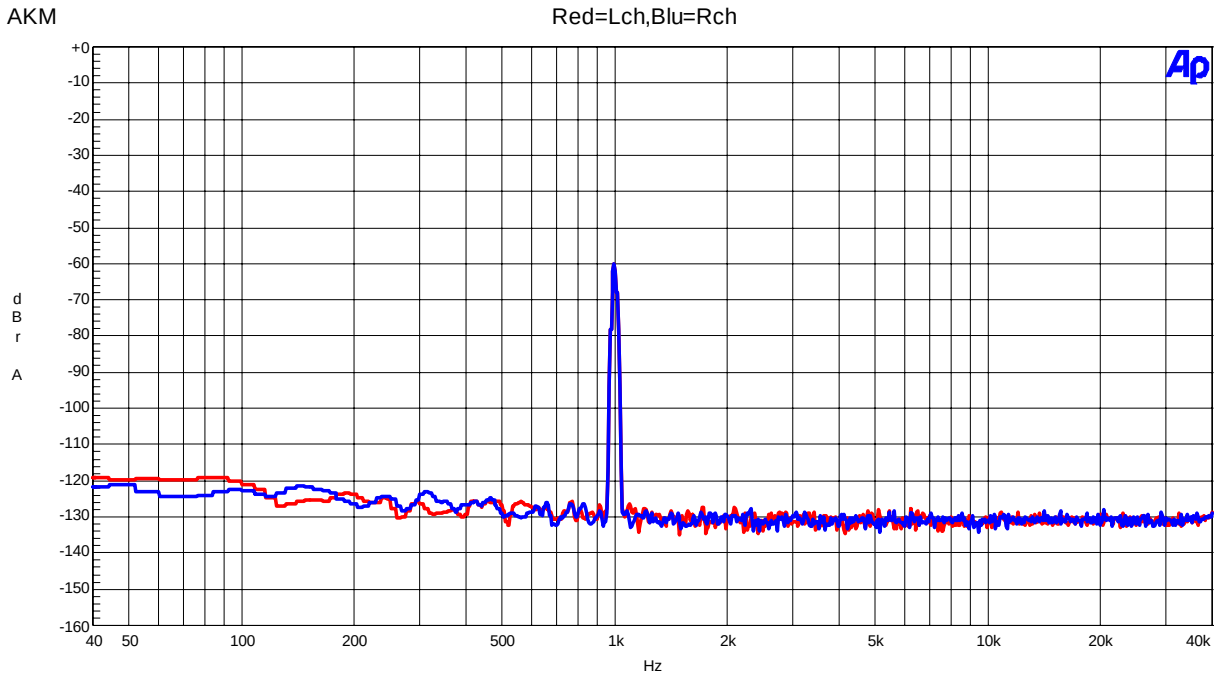


Figure 28. FFT(Input Frequency=1kHz, Input Level=-60dBFS)

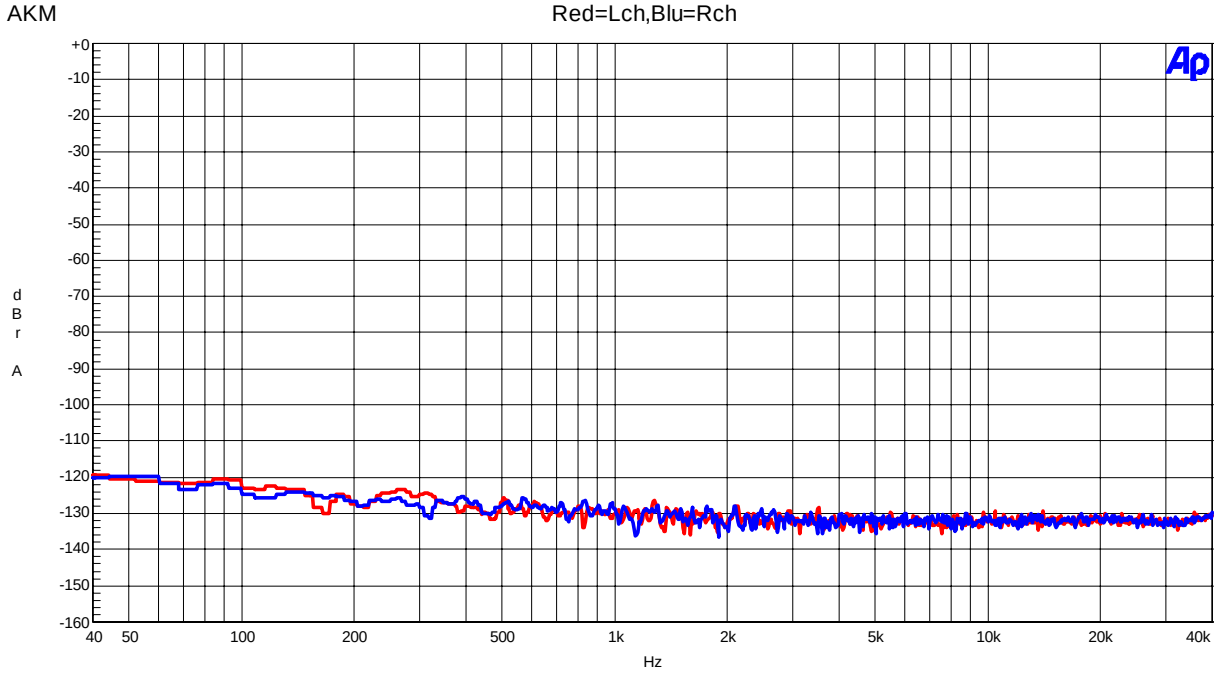


Figure 29. FFT(noise floor)

(DAC fs=96kHz)

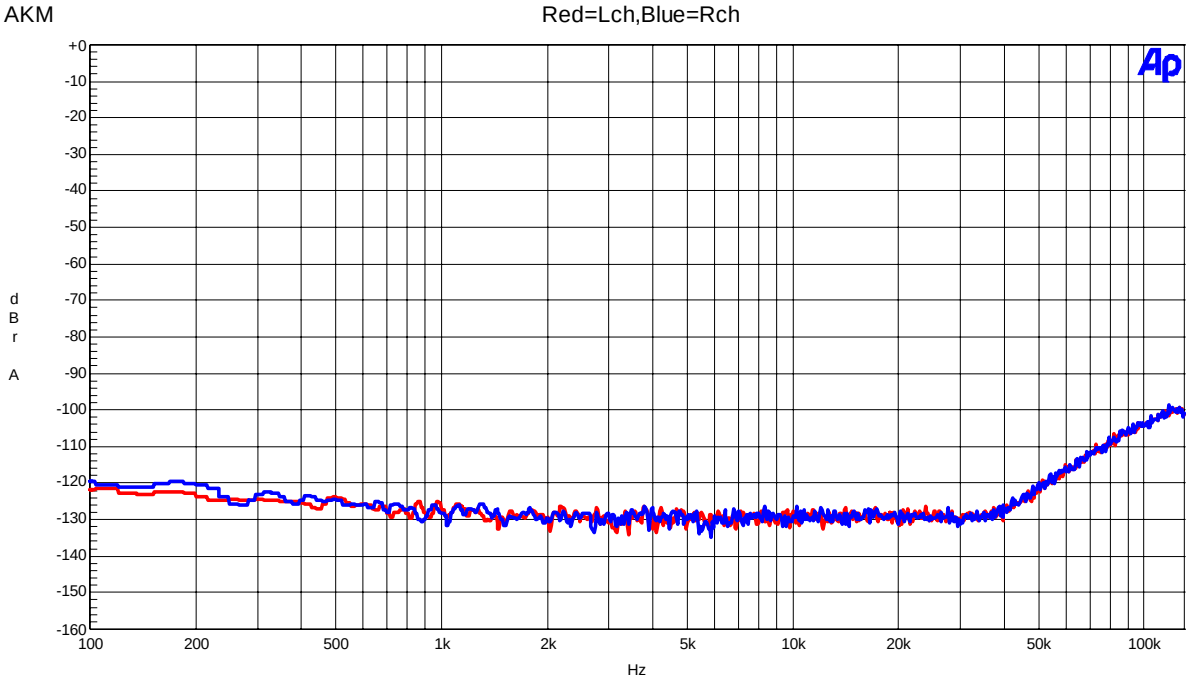


Figure 30. FFT (out-of-band noise)

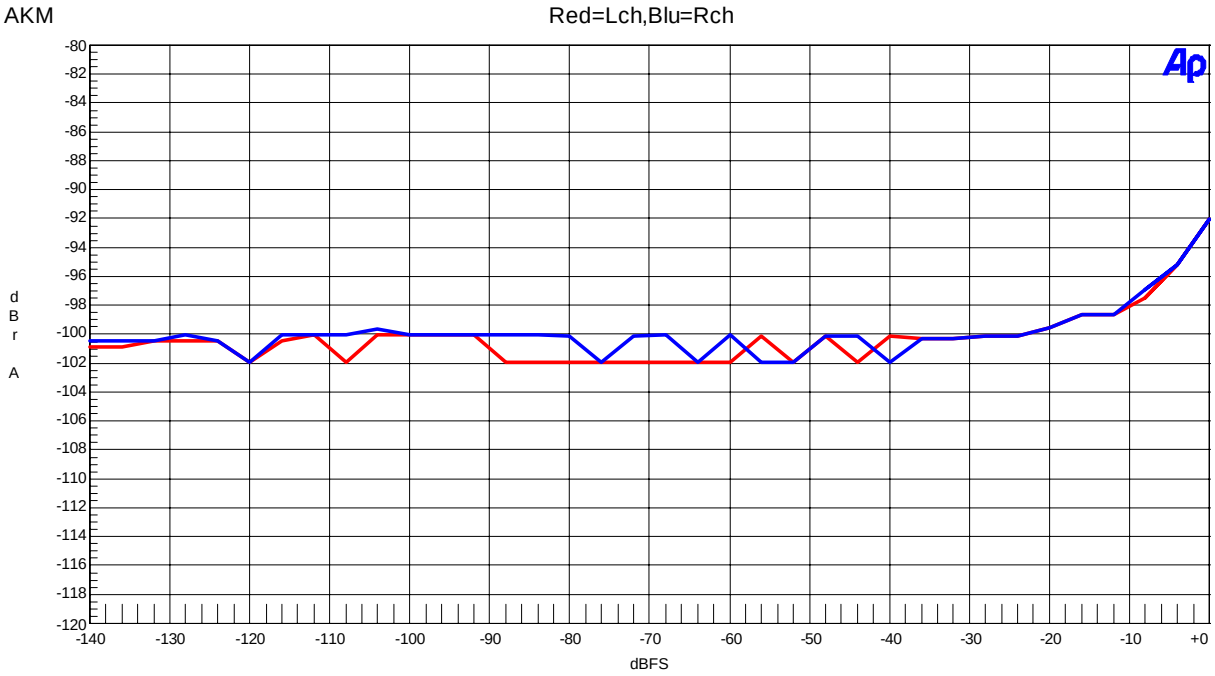


Figure 31. THD+N vs Input Level (Input Frequency=1kHz)

(DAC fs=96kHz)

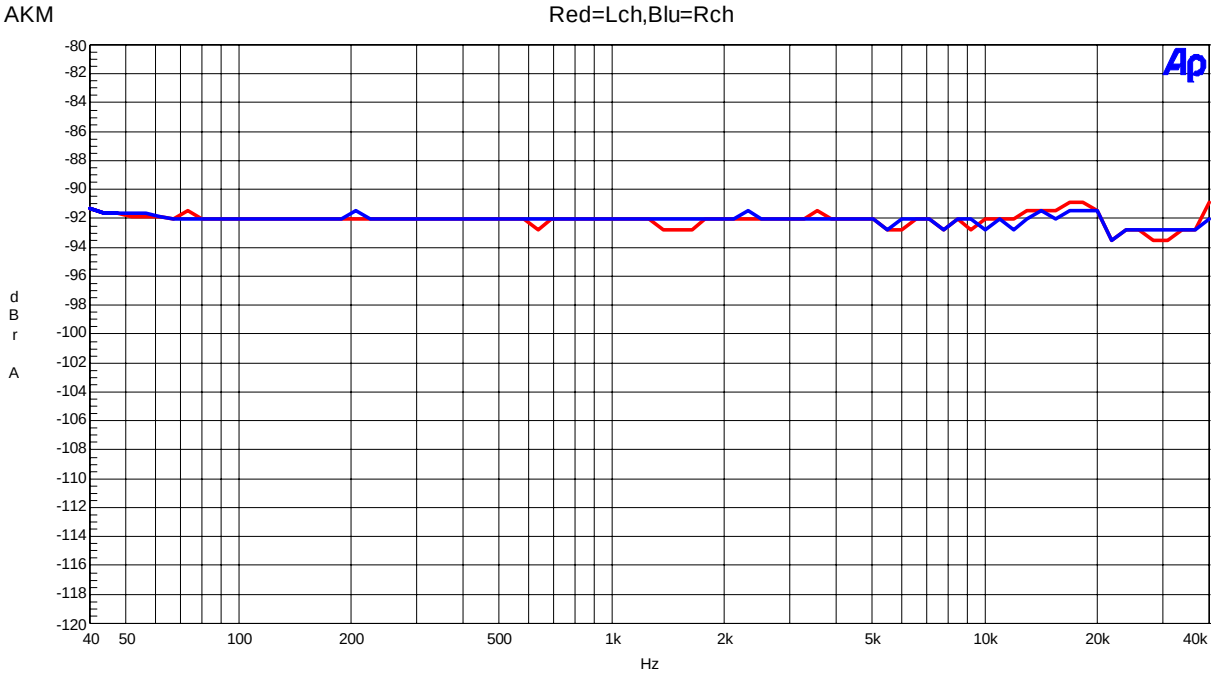


Figure 32. THD+N vs Input Frequency (Input Level=0dBFS)

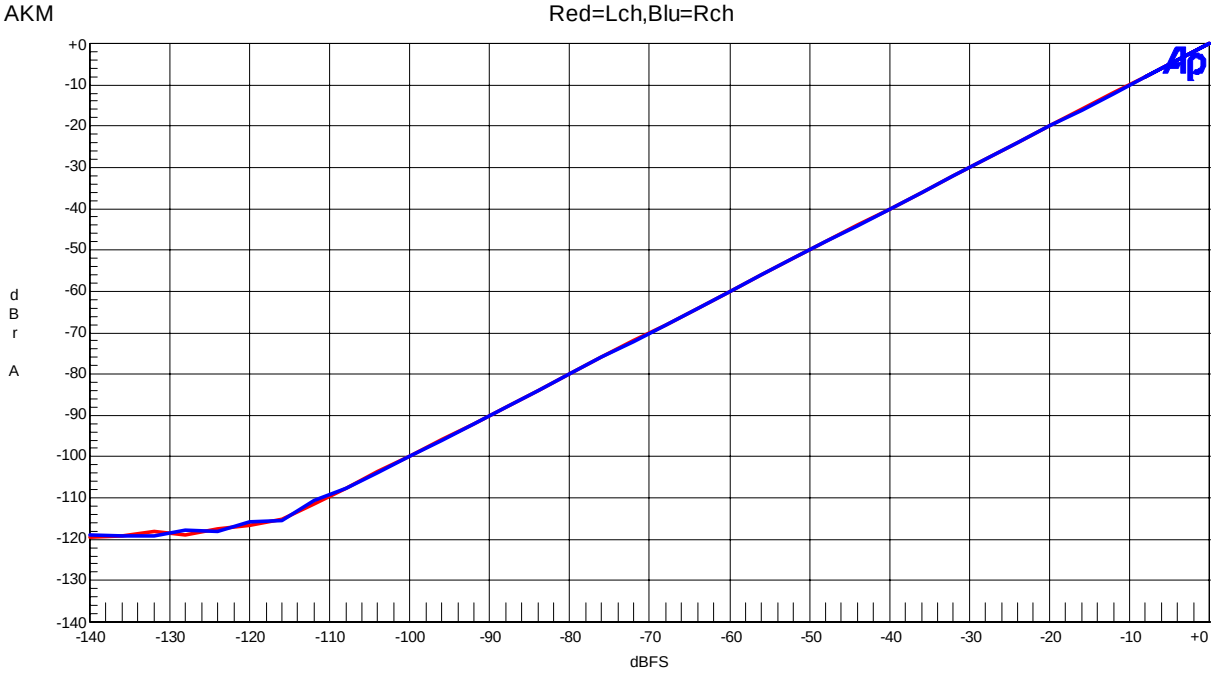


Figure 33. Linearity (Input Frequency=1kHz)

(DAC fs=96kHz)

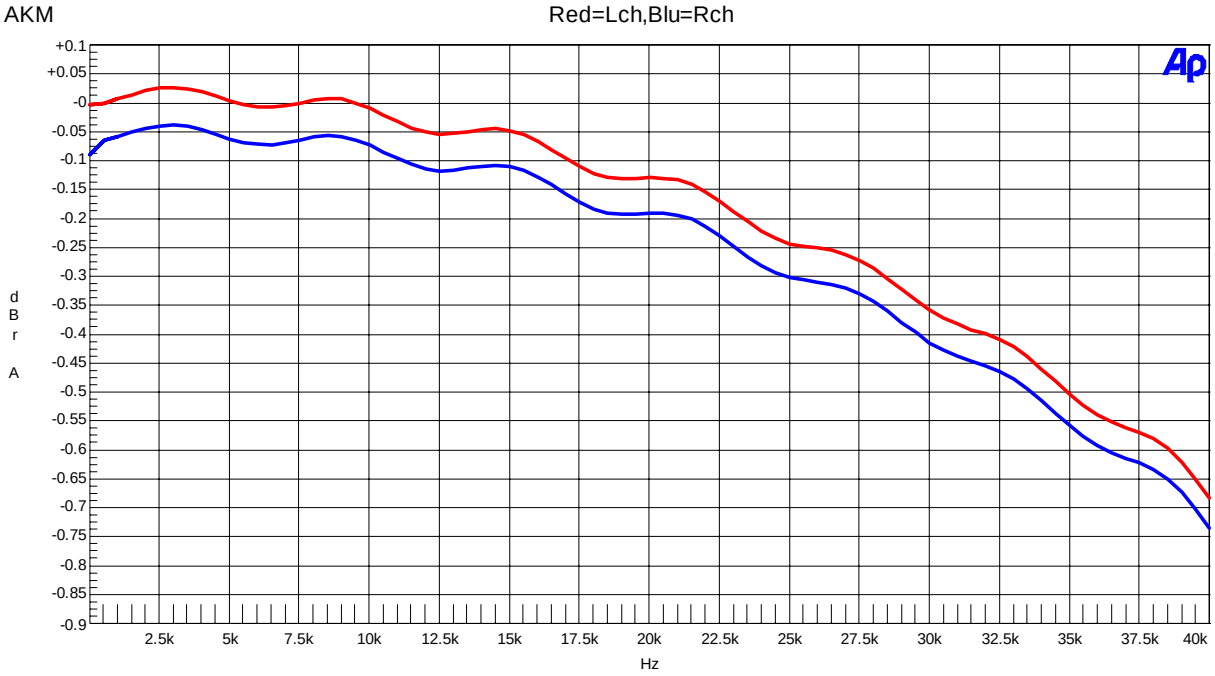


Figure 34. Frequency Response (Input Level=0dBFS)

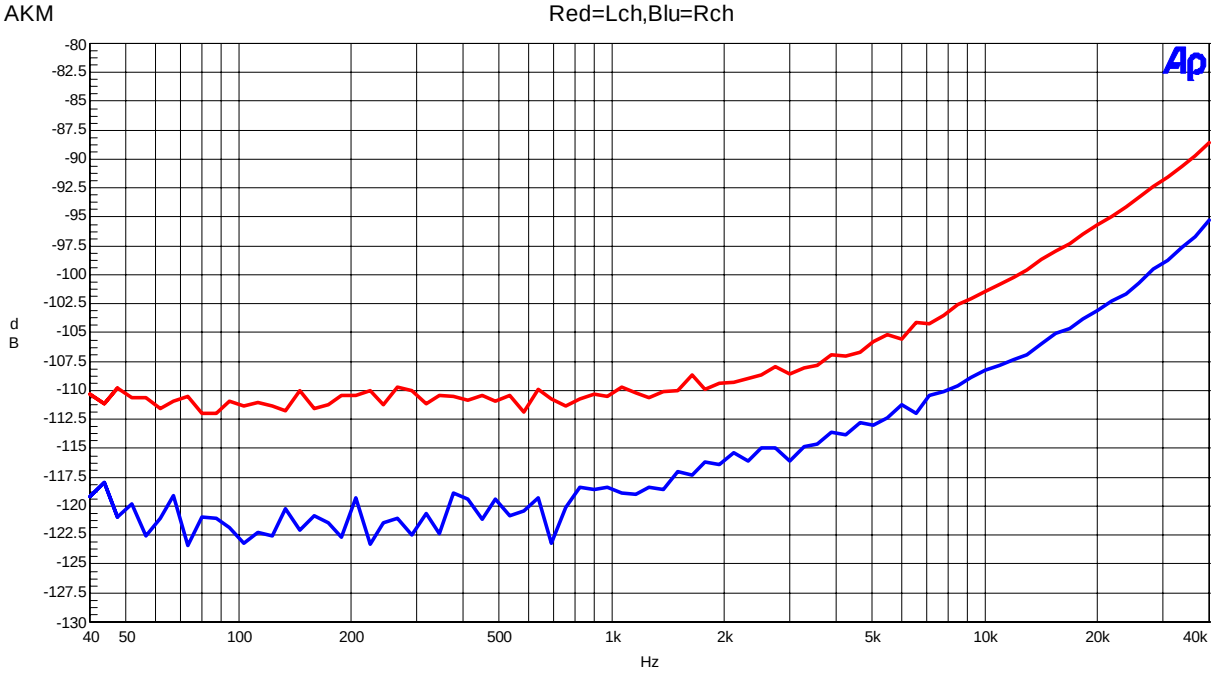


Figure 35. Cross-talk (Input Level=0dBFS)

(DAC fs=192kHz)

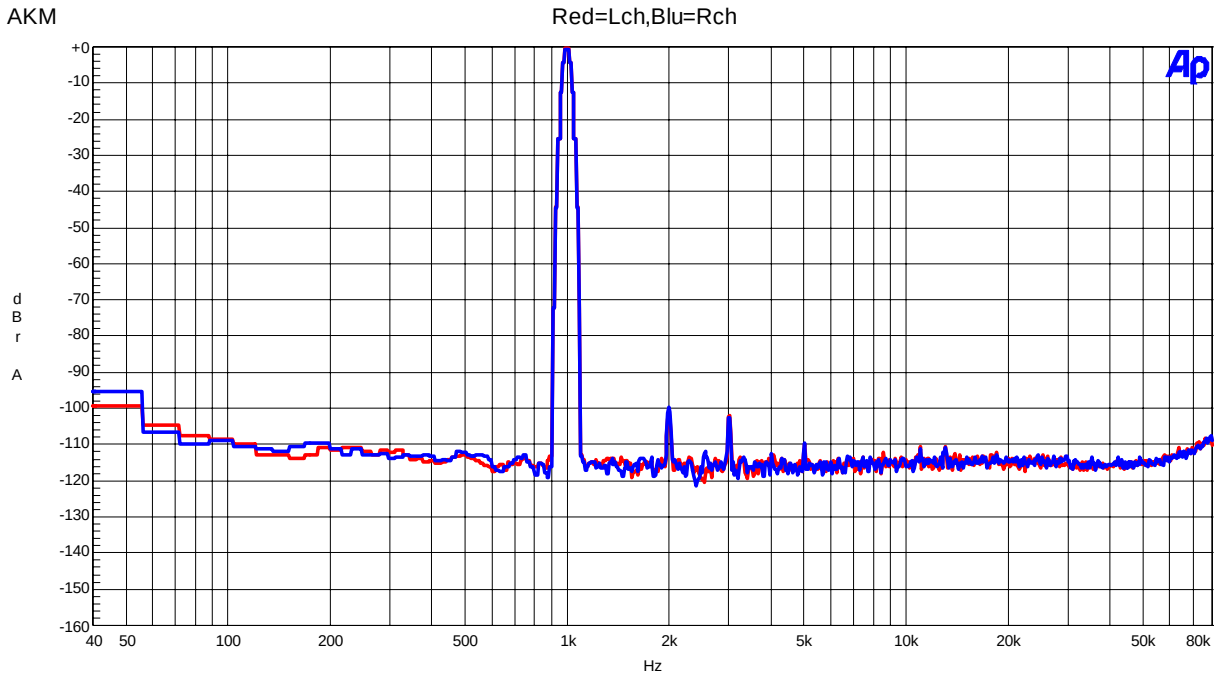


Figure 36. FFT(Input Frequency=1kHz, Input Level=0dBFS)

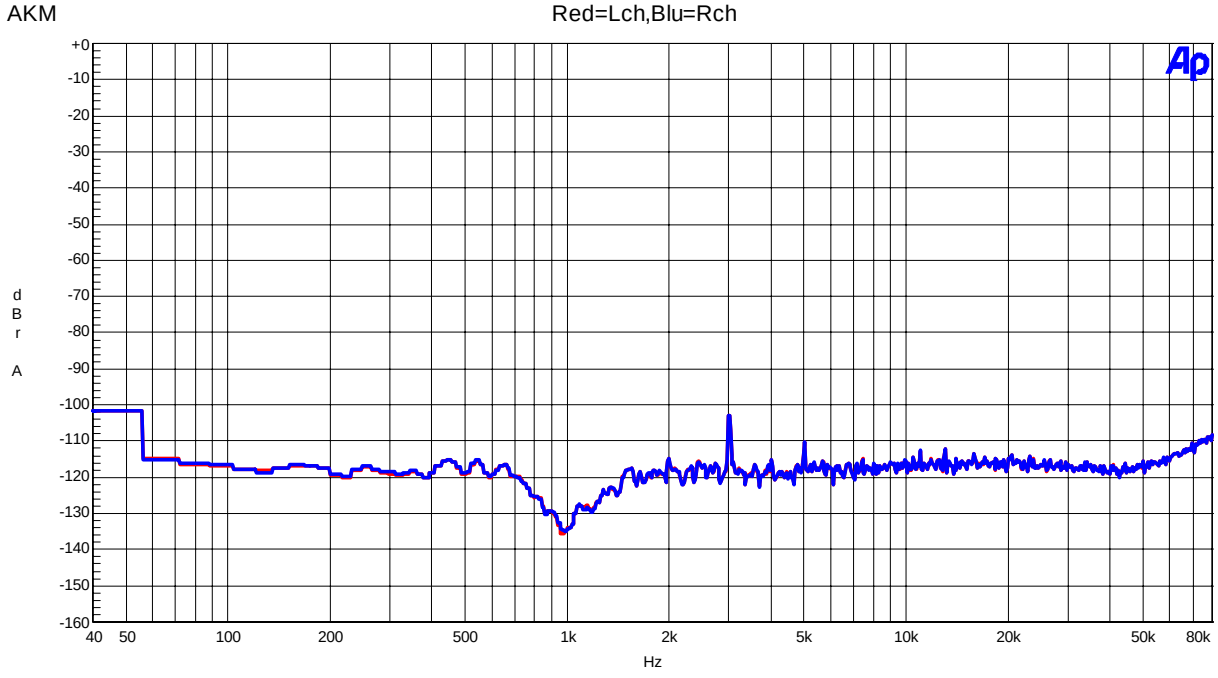


Figure 37. FFT(Input Frequency=1kHz, Input Level=0dBFS,Notch-on)

(DAC fs=192kHz)

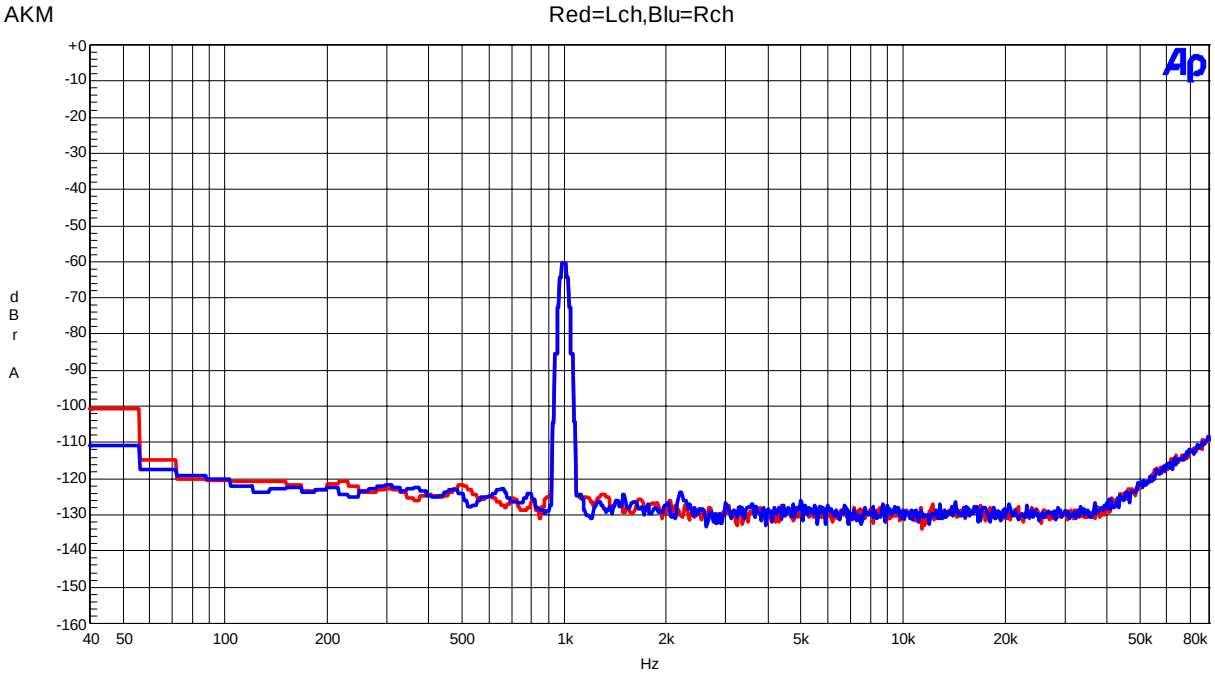


Figure 38. FFT(Input Frequency=1kHz, Input Level=-60dBFS)

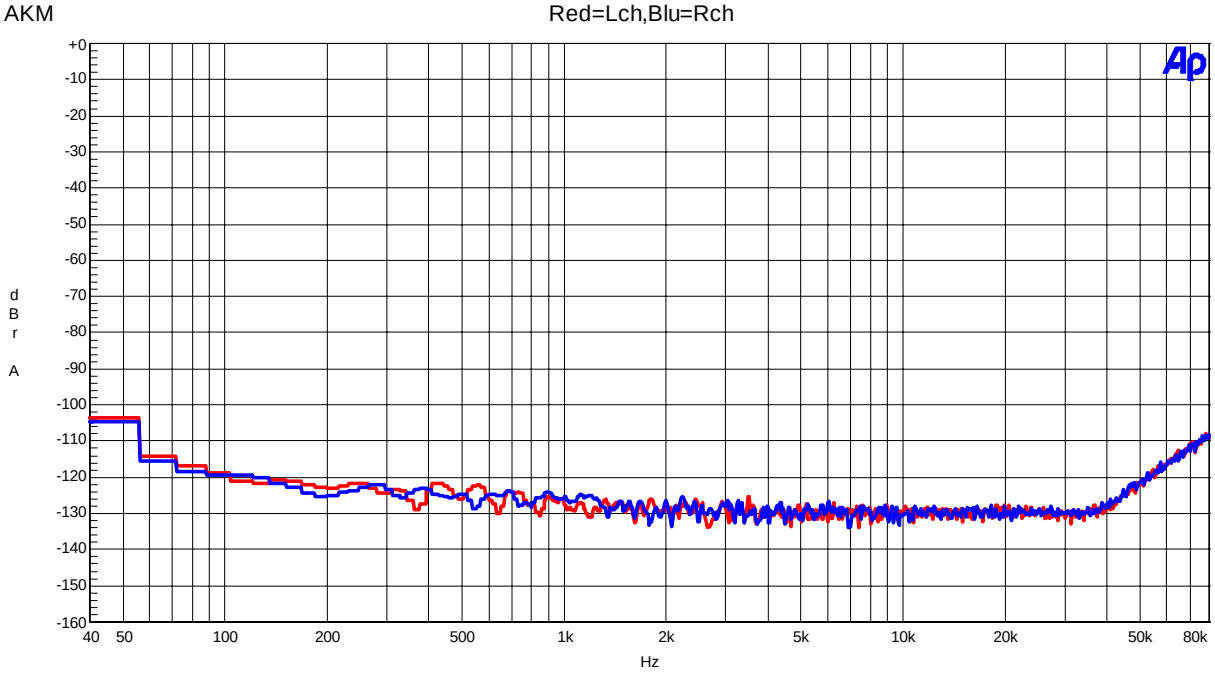


Figure 39. FFT(noise floor)

(DAC fs=192kHz)

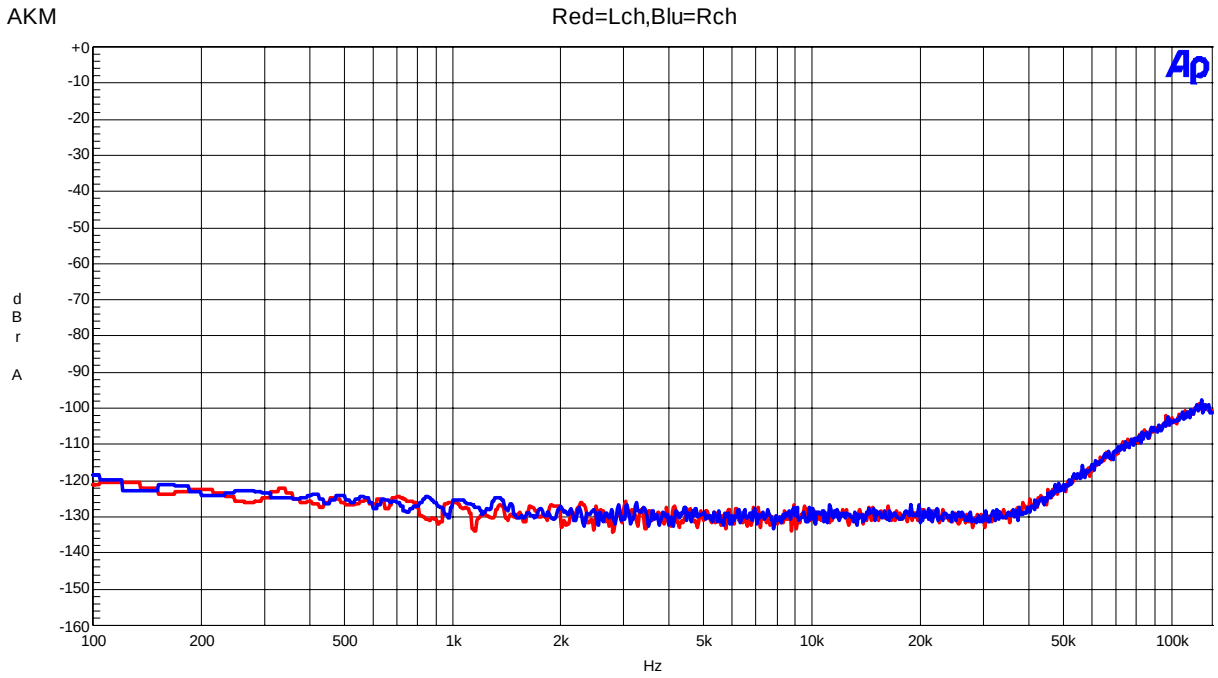


Figure 40. FFT(out-of-band noise)

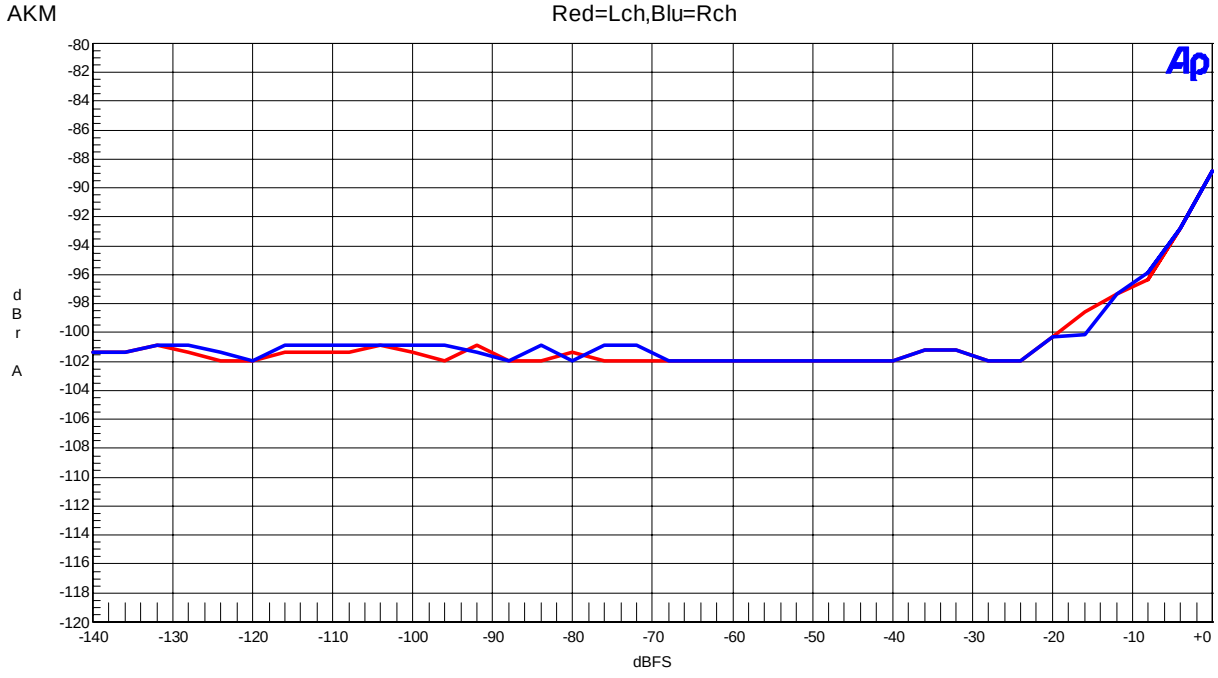


Figure 41. THD+N vs Input Level (Input Frequency=1kHz)

(DAC fs=192kHz)

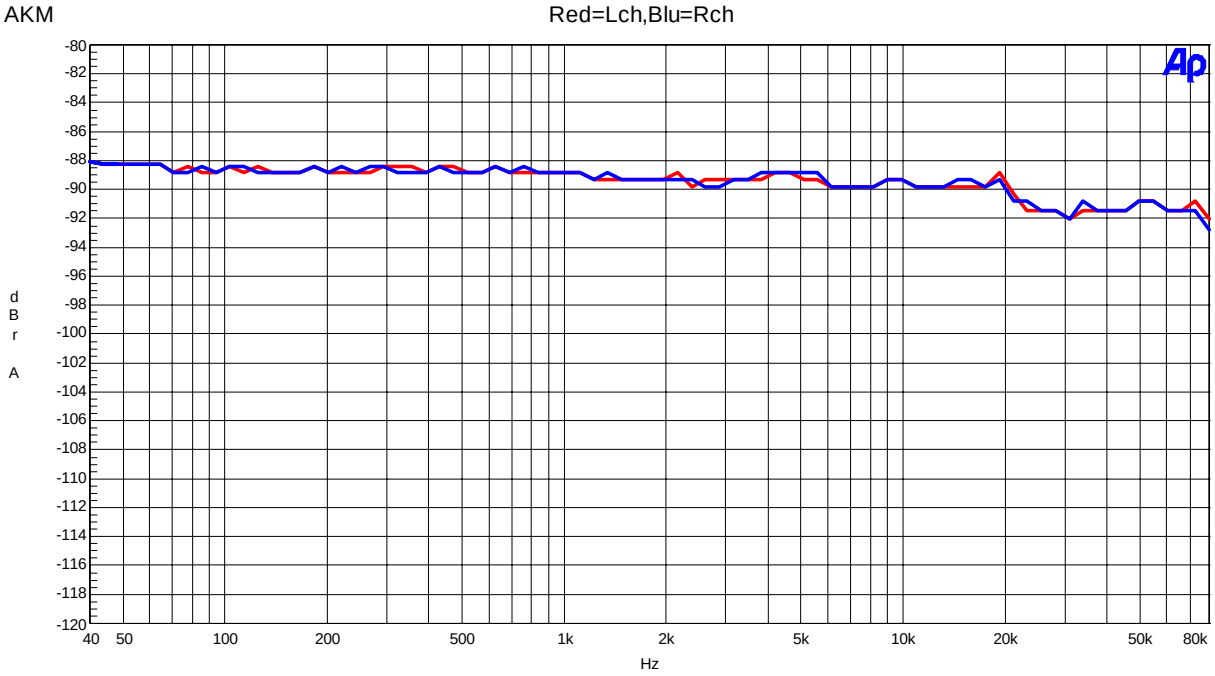


Figure 42. THD+N vs Input Frequency (Input Level=0dBFS)

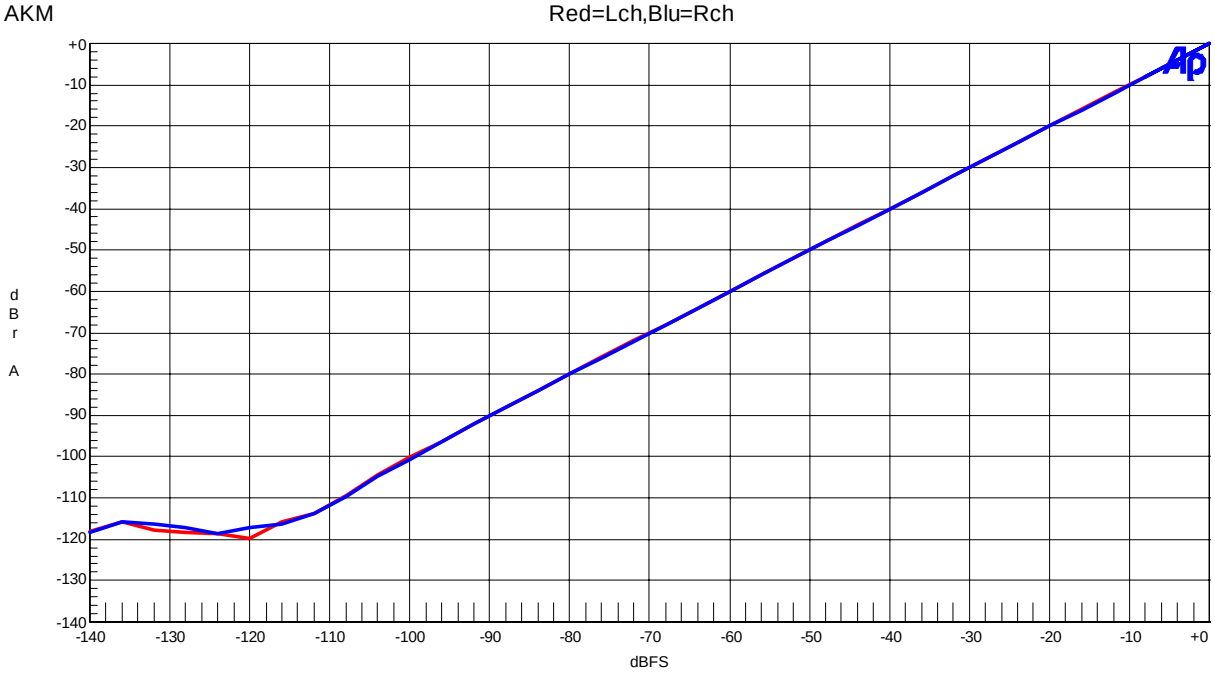


Figure 43. Linearity (Input Frequency=1kHz)

(DAC fs=192kHz)

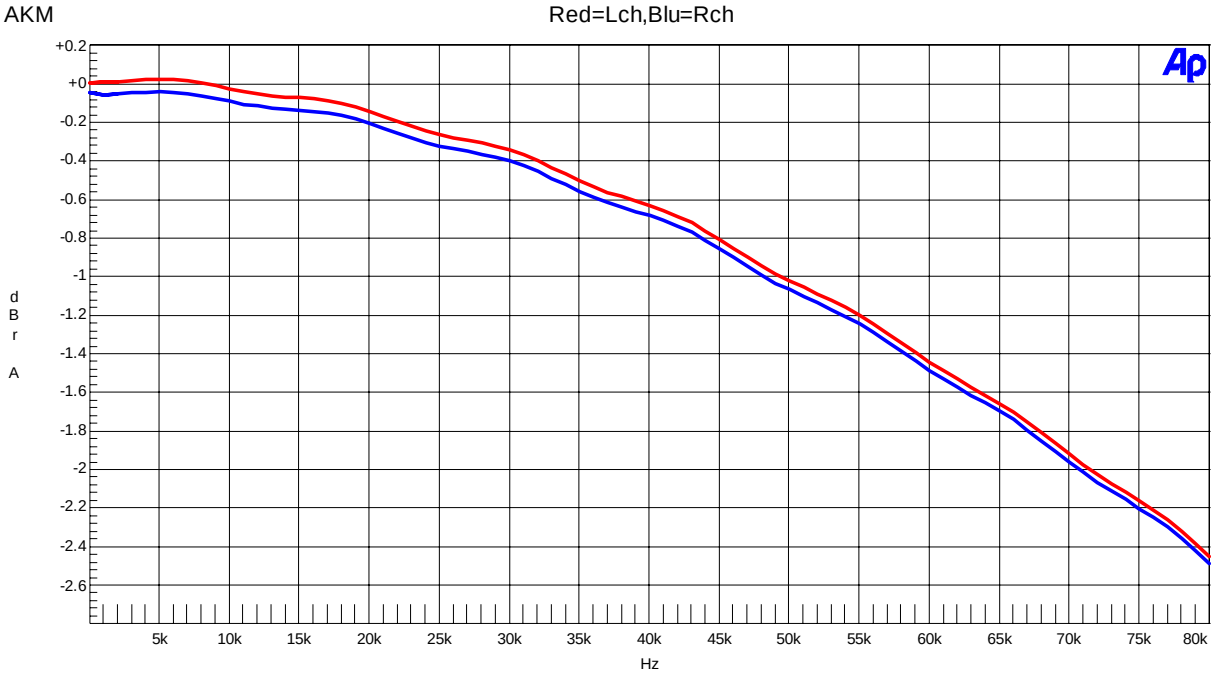


Figure 44. Frequency Response (Input Level=0dBFS)

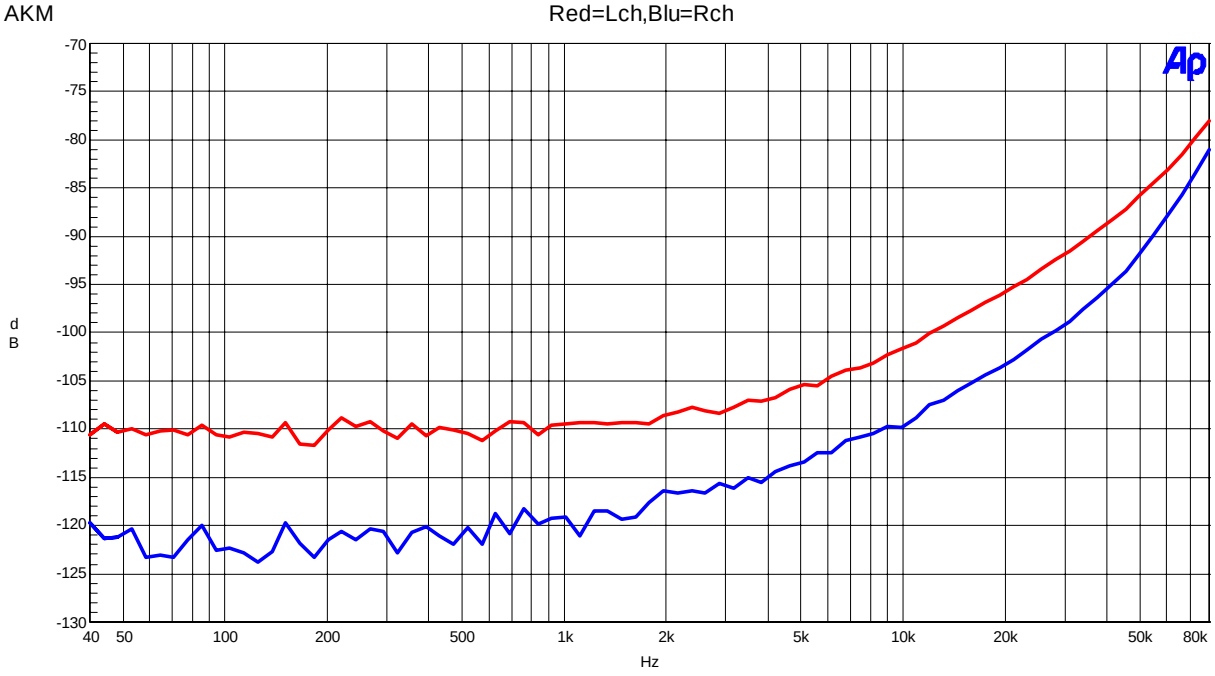
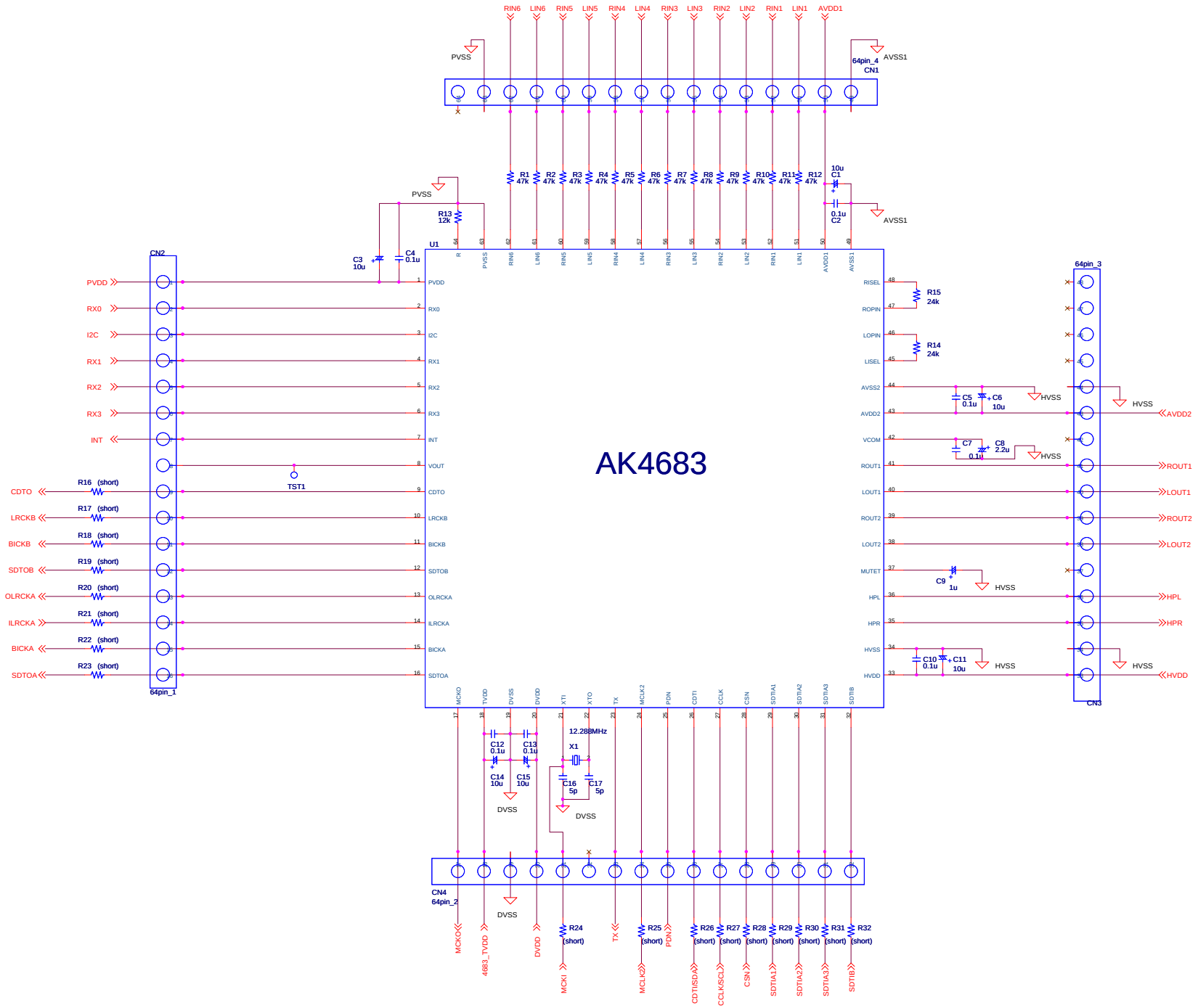


Figure 45. Cross-talk (Input Level=0dBFS)

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
05/03/10	KM077501	0	First Edition	
05/04/05	KM077502	1	Circuit Change	Board REV Change: REV.0 → REV.1 Resistance Value Change R45: 150 → 100 R46: 240 → 330
05/07/19	KM077503	1	Measurement Result Change	Device Revision Change: Rev.A→Rev.C Measurement Result Change (ADC part: fs=48KHz, DAC part: fs=48KHz) Plots Add (ADC part:fs=48KHz,96KHz, DAC part:fs=48KHz,96KHz,192KHz)
05/08/03	KM077504	1	Measurement Result Change	Measurement Result Change (DAC part: fs=48KHz, 96KHz, 192KHz)



Title	AKD4683-A	
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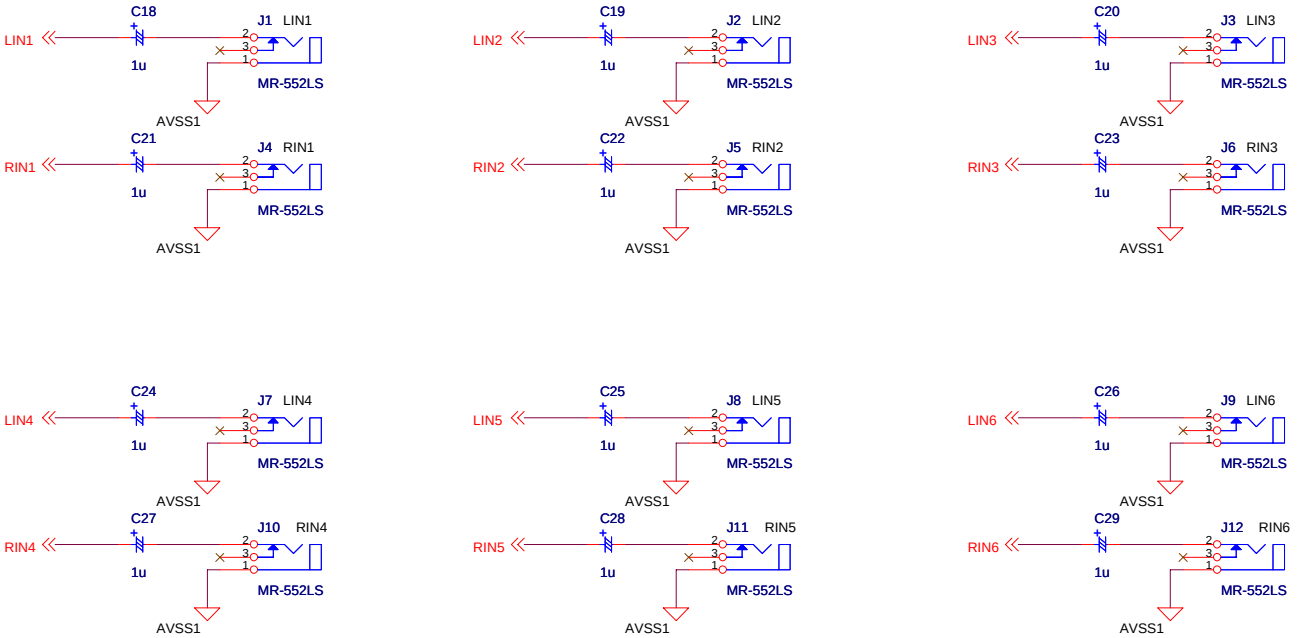
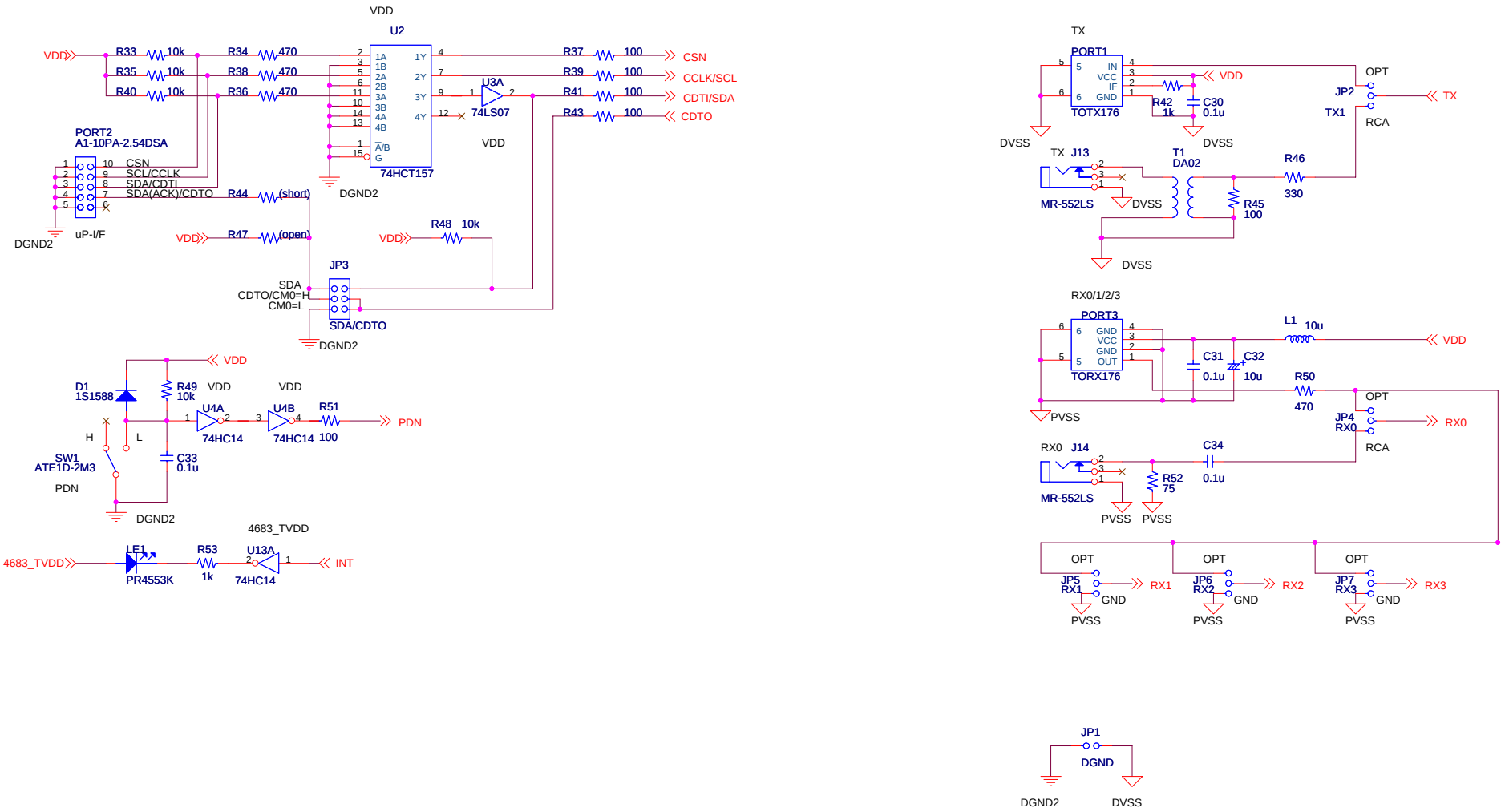


Title	AK4683-A		
Size A3	Document Number LIN/RIN		Rev 1
Date: Tuesday, April 05, 2005	Sheet 2 of 7		



Title	AKD4683-A	
Size A3	Document Number INPUT/OUTPUT	Rev 1
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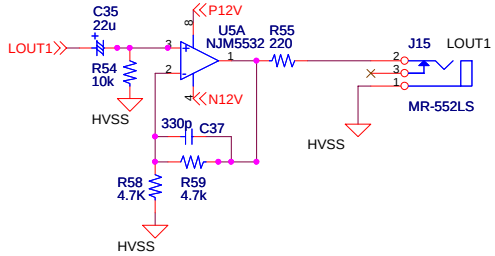

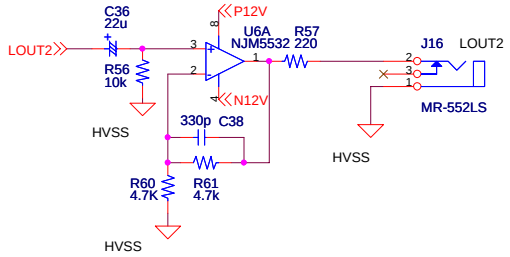

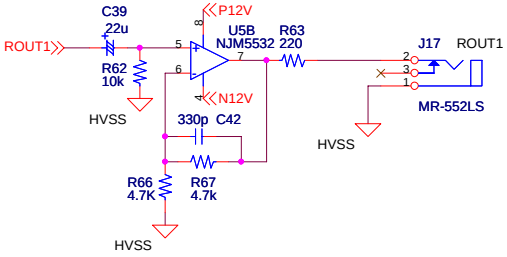

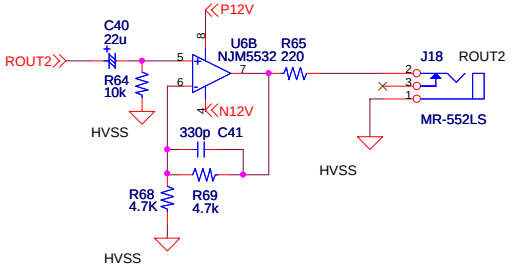

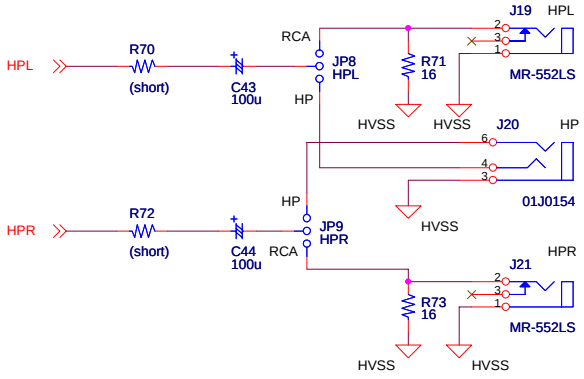

Title	AKD4683-A		
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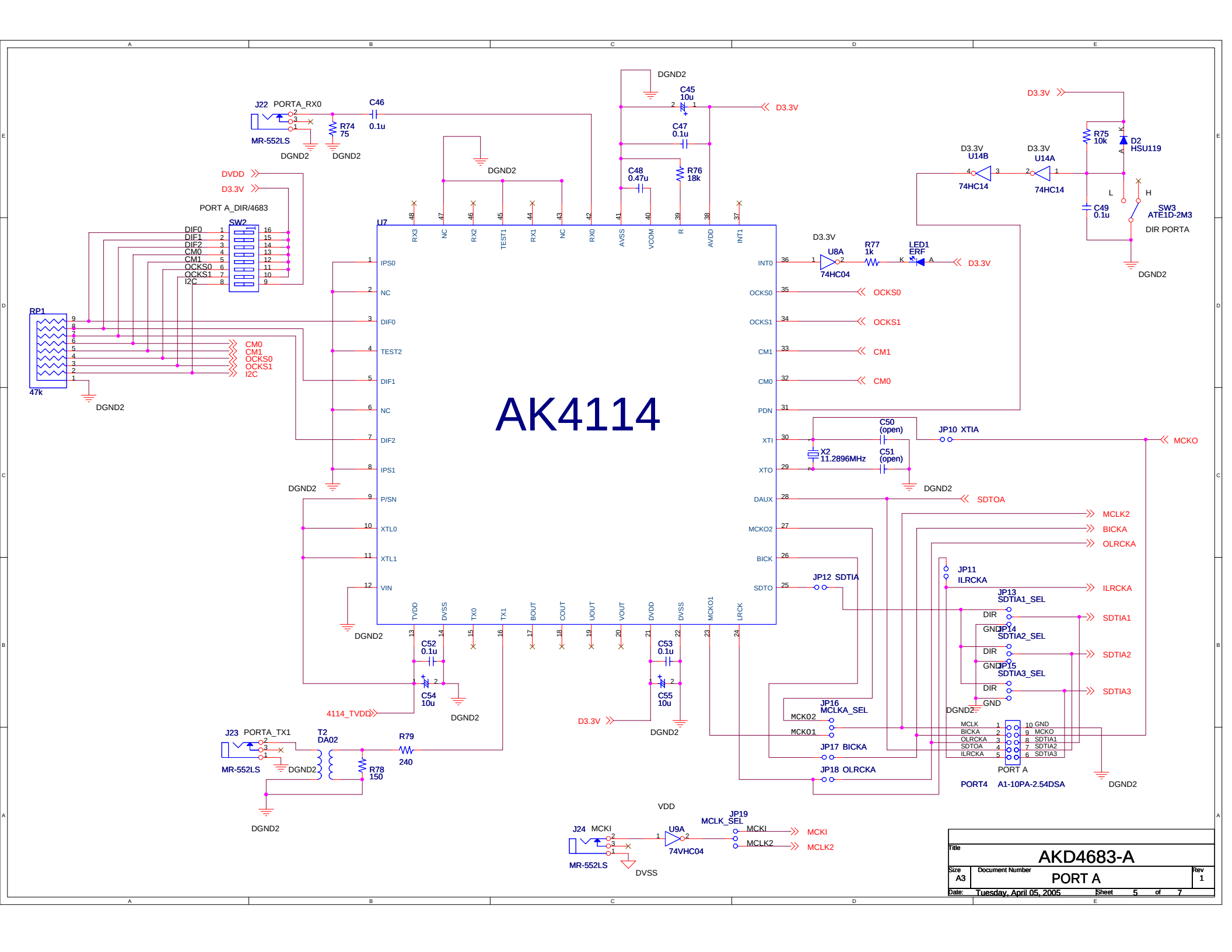
Date: Tuesday, April 05, 2005	Sheet 4 of 7		



Title	AKD4683-A
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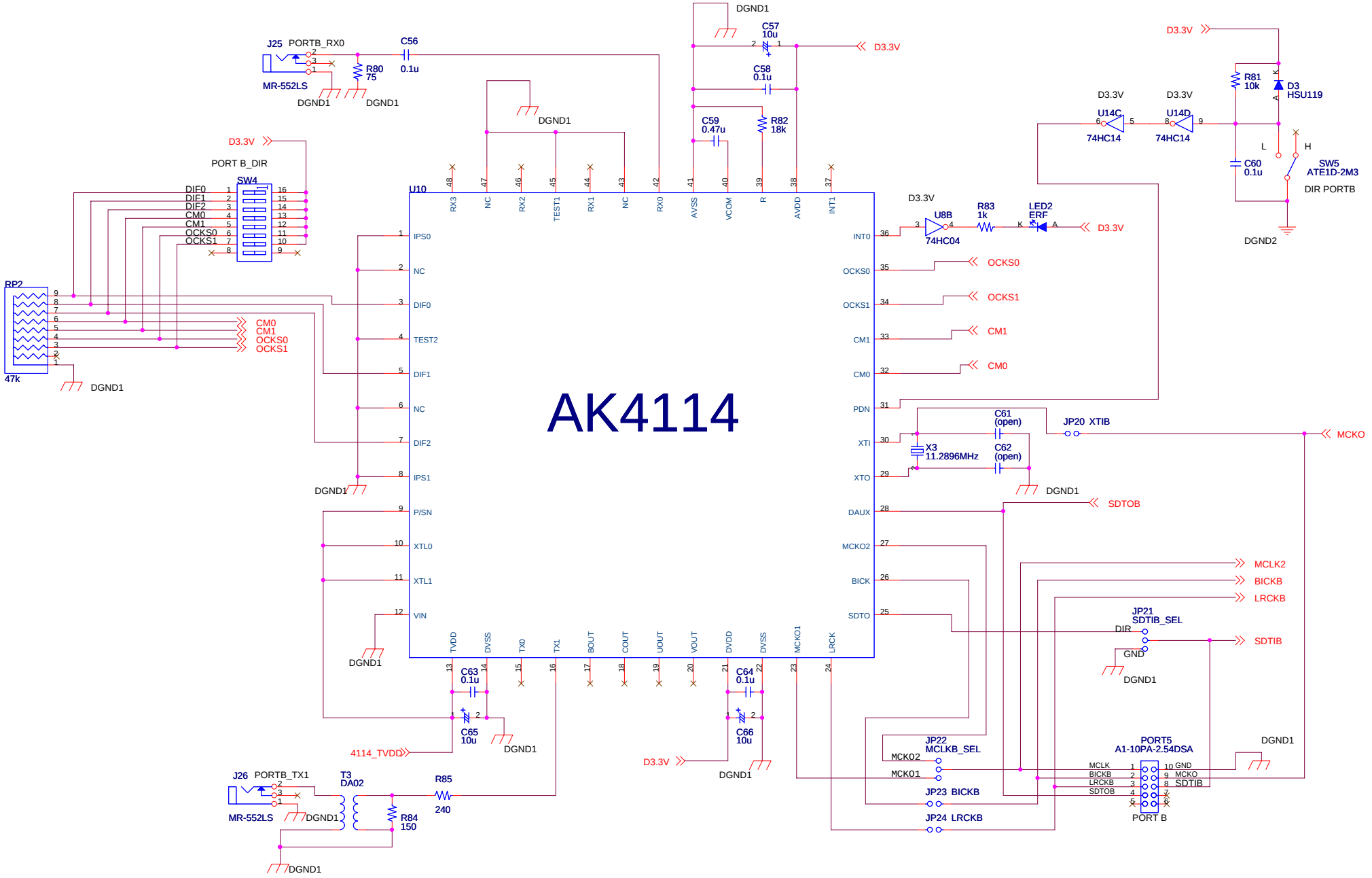

Title	AKD4683-A		
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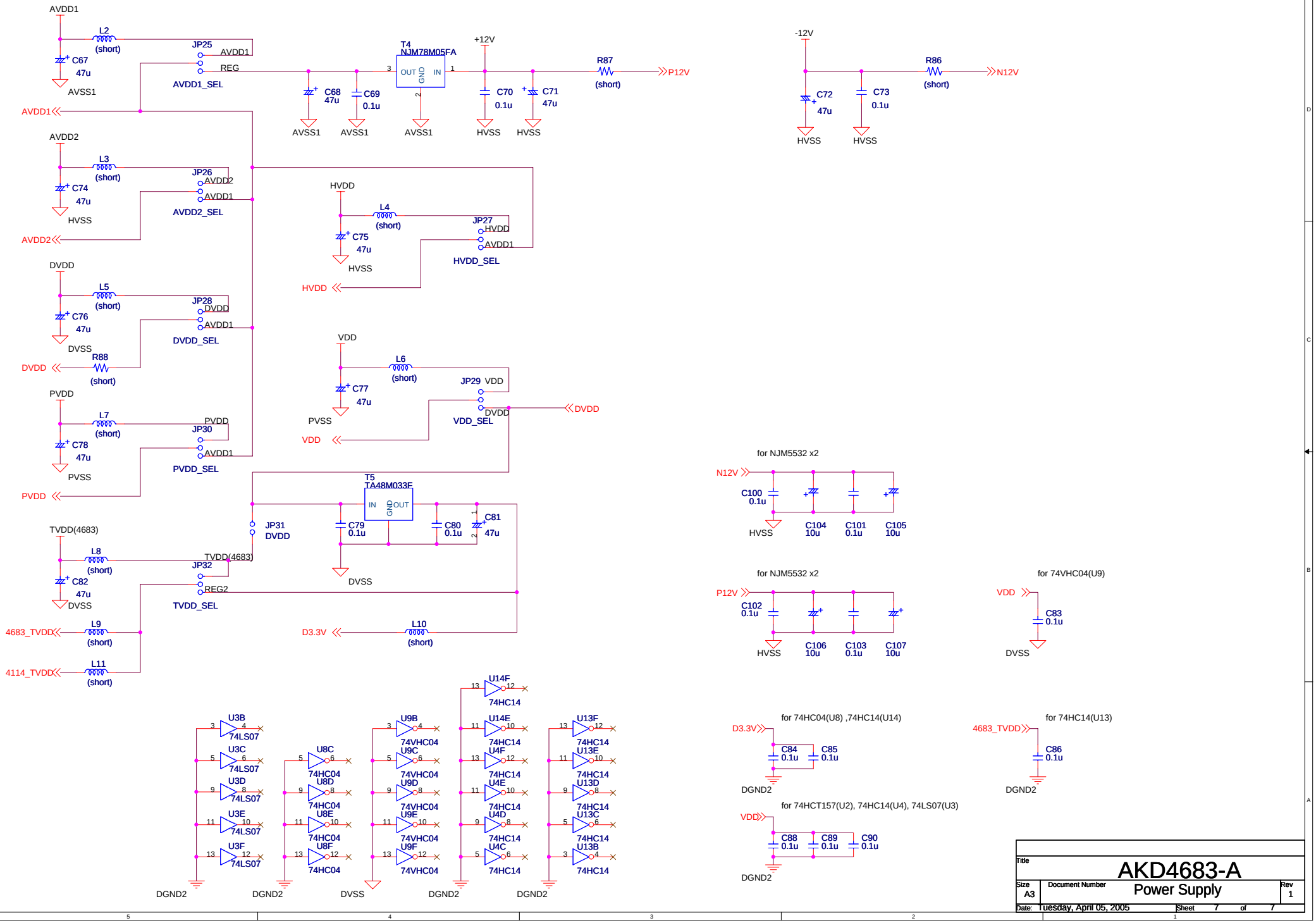
AVDD1
L2
(short)
C67
47u
AVSS1
JP25
AVDD1
REG
AVDD1_SEL
T4
NJM78M05FA
OUT
GND
IN
+12V
R87
(short)
P12V
C68
47u
C69
0.1u
C70
0.1u
C71
47u
HVSS
-12V
R86
(short)
N12V
C72
47u
C73
0.1u
AVDD2
L3
(short)
C74
47u
JP26
AVDD2
AVDD1
AVDD2_SEL
HVDD
L4
(short)
C75
47u
JP27
HVDD
AVDD1
HVDD_SEL
DVDD
L5
(short)
C76
47u
DVSS
JP28
DVDD
AVDD1
DVDD_SEL
R88
(short)
VDD
L6
(short)
C77
47u
PVSS
JP29 VDD
DVDD
VDD_SEL
PVDD
L7
(short)
C78
47u
JP30
PVDD
AVDD1
PVDD_SEL
T5
TA48M033F
IN
GND
OUT
C79
0.1u
C80
0.1u
C81
47u
JP31
DVDD
TVDD(4683)
L8
(short)
C82
47u
JP32
TVDD(4683)
REG2
TVDD_SEL
4683_TVDD
L9
(short)
4114_TVDD
L11
(short)
D3.3V
L10
(short)
for NJM5532 x2
C100
0.1u
C104
10u
C101
0.1u
C105
10u
C102
0.1u
C106
10u
C103
0.1u
C107
10u
for 74VHC04(U9)
C83
0.1u
U3B
U3C
U3D
U3E
U3F
74LS07
U8C
U8D
U8E
U8F
74HC04
U9B
U9C
U9D
U9E
U9F
74VHC04
U14F
U14E
U4F
U4E
U4D
U4C
74HC14
U13F
U13E
U13D
U13C
U13B
for 74HC04(U8) ,74HC14(U14)
C84
0.1u
C85
0.1u
for 74HC14(U13)
C86
0.1u
for 74HCT157(U2), 74HC14(U4), 74LS07(U3)
C88
0.1u
C89
0.1u
C90
0.1u
DGND2
DVSS
AKD4683-A
Power Supply
Size
A3
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1
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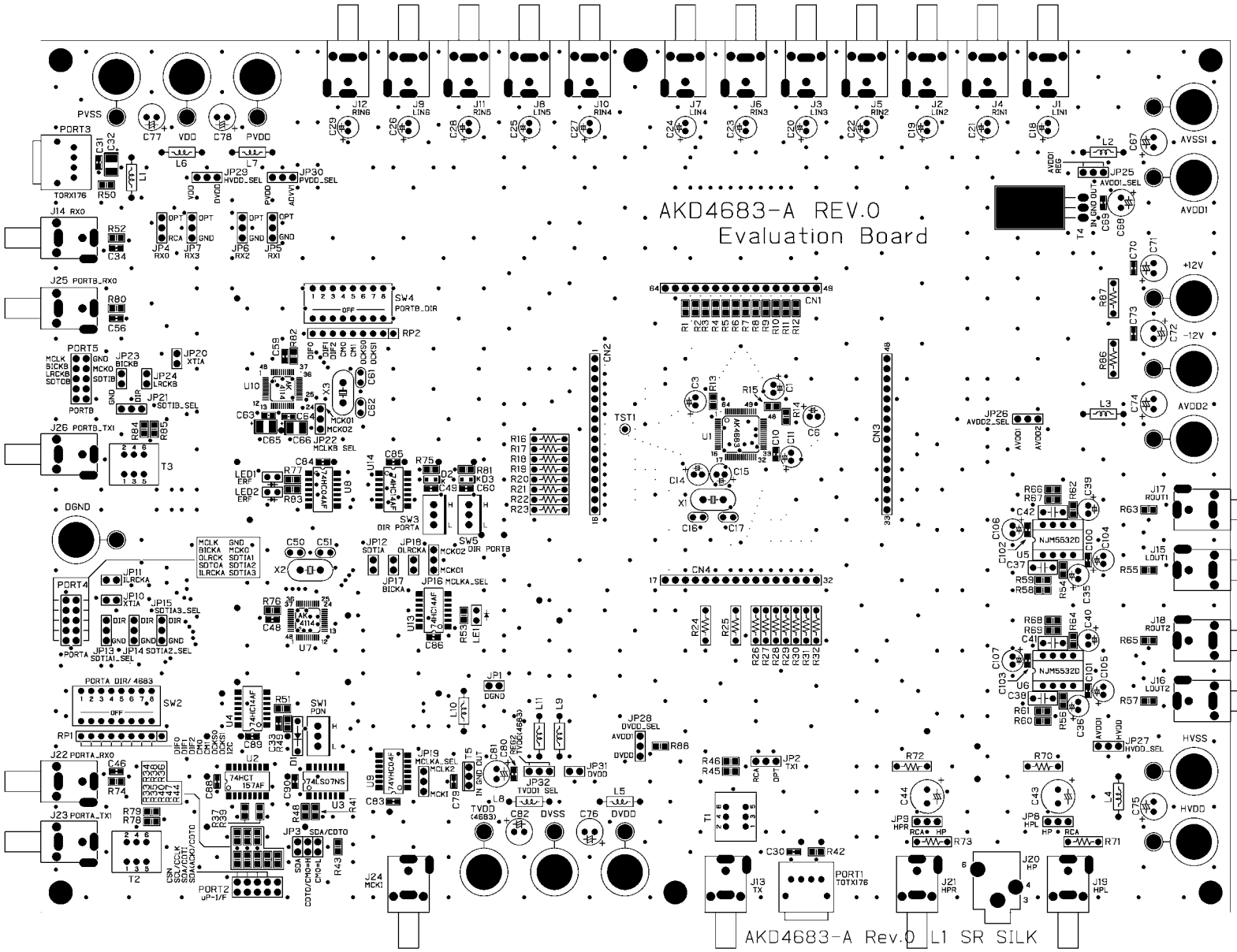
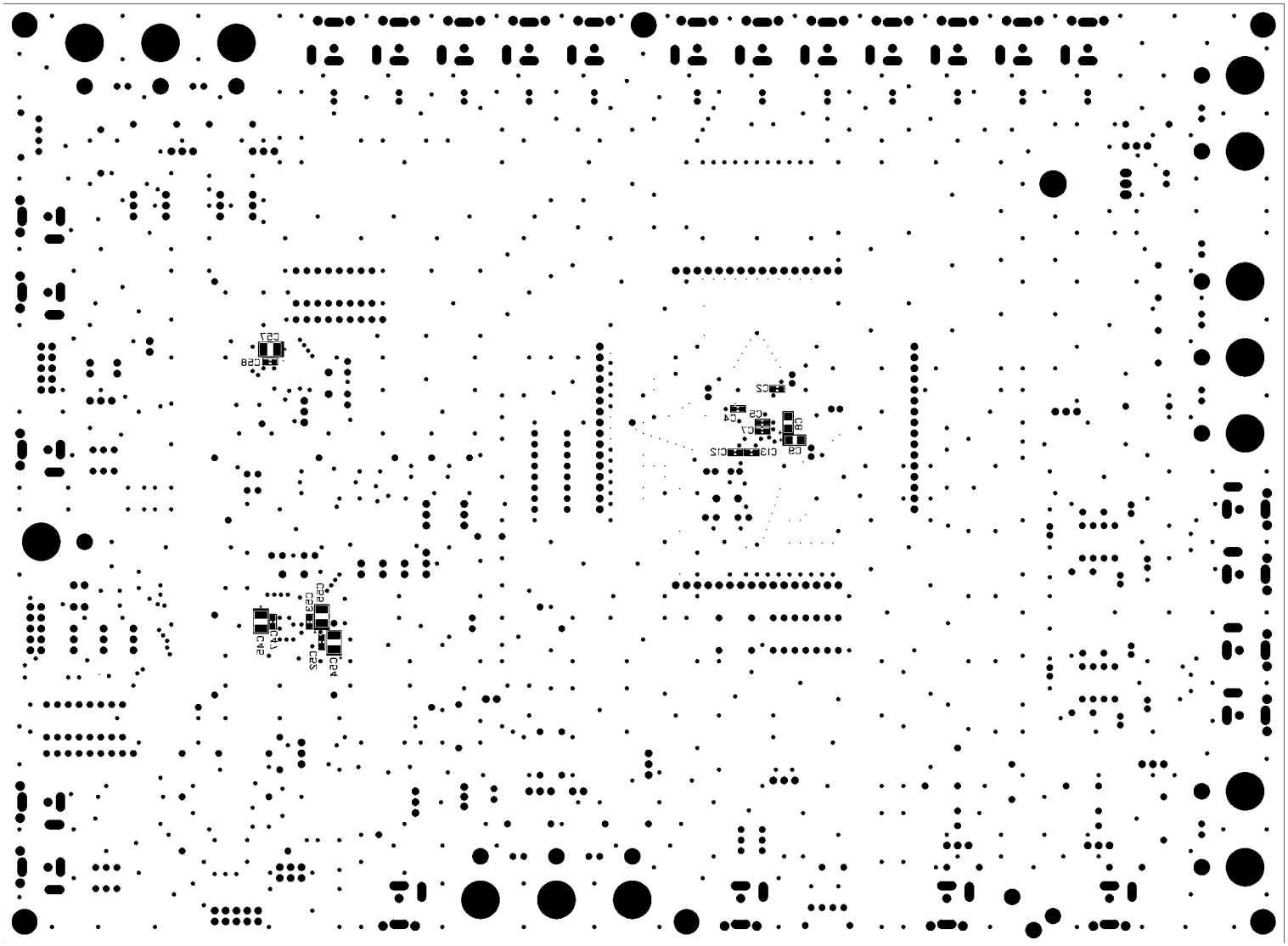
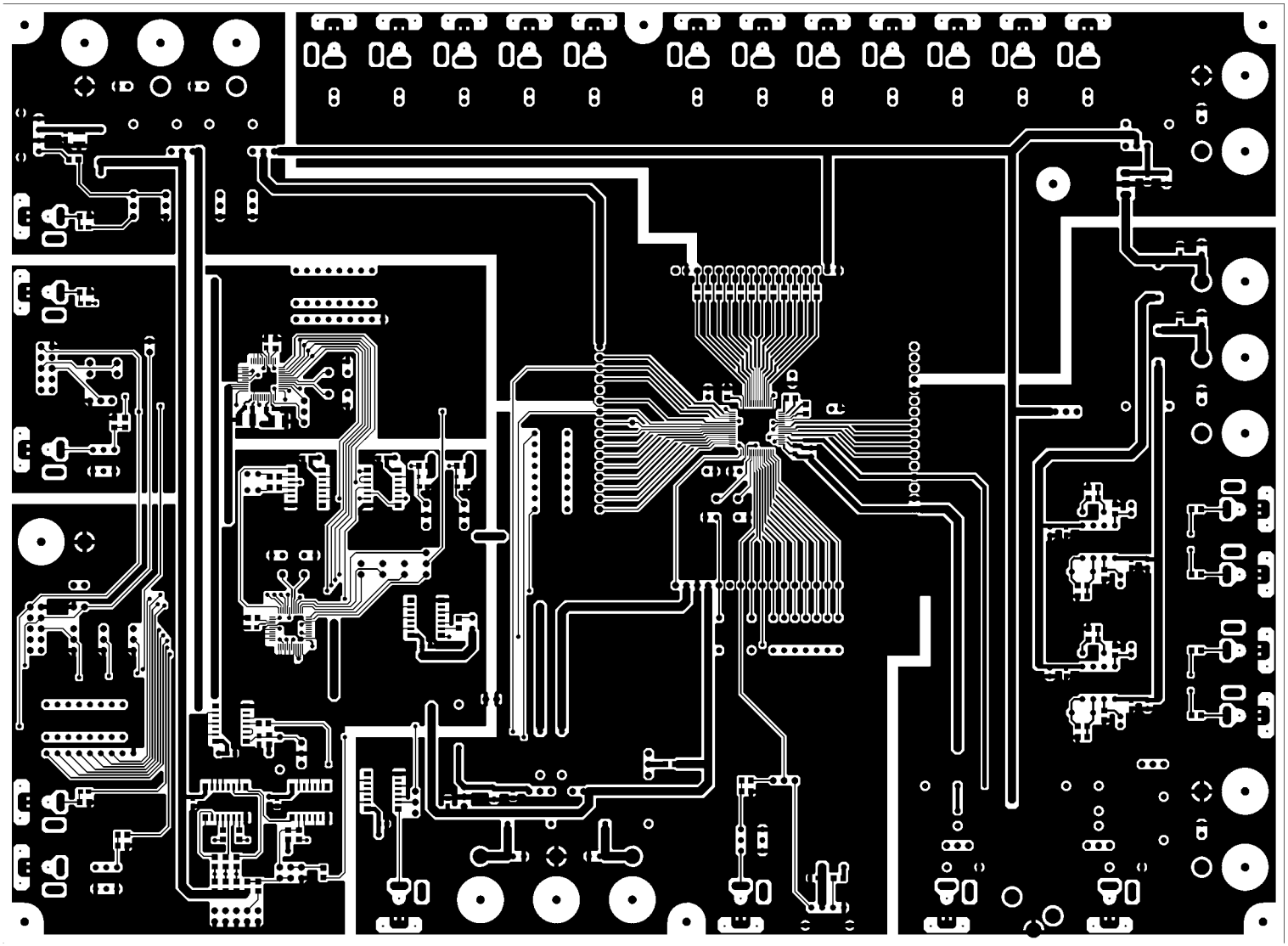

AKD4683-A REV.0
Evaluation Board
AKD4683-A Rev.0 L1 SR SILK


AKD4683-A Rev.0 L2 SR SILK



AKD4683-A Rev.0 L1

AKD4683-A Rev.0 L2