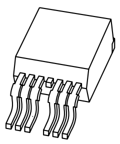


BUK7C06-40AITE

N-channel TrenchMOS standard level FET

Rev. 04 — 23 June 2005 **Product data sheet**

1. Product profile

1.1 General description

N-channel enhancement mode power Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology, featuring very low on-state resistance and including TrenchPLUS current sensing, and diodes for ElectroStatic Discharge (ESD) and overtemperature protection.

1.2 Features

- Q101 compliant
- ESD protection
- Integrated temperature sensor
- Integrated current sensor

1.3 Applications

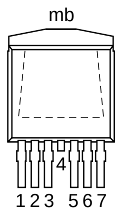
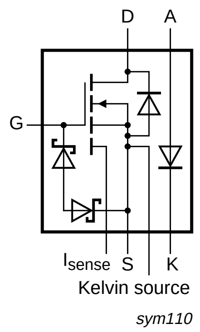
- Variable valve timing for engines
- Automotive and power switching
- Electrical power assisted steering
- Fan control

1.4 Quick reference data

- $V_{DS} \leq 40$ V
- $I_D \leq 155$ A
- $R_{DSon} = 4.7$ mΩ (typ)
- $V_F = 658$ mV (typ)
- $S_F = -1.54$ mV/K (typ)
- $I_D/I_{sense} = 615$ (typ)

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)	 SOT427 (D2PAK)	
2	I_{sense}		
3	anode (A)		
4	drain (D)		
5	cathode (K)		
6	kelvin source		
7	source (S)		
mb	mounting base; connected to drain (D)		

PHILIPS

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
BUK7C06-40AITE	D2PAK	Plastic single-ended surface mounted package; 7 leads (one lead cropped)	SOT427

4. Limiting values

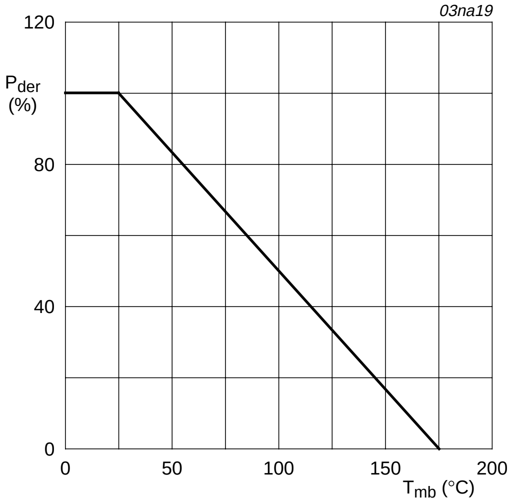
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage			-	40	V
V_{DGR}	drain-gate voltage (DC)	R_{GS} = 20 kΩ		-	40	V
V_{GS}	gate-source voltage			-	±20	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see Figure 2 and 3	[1]	-	155	A
			[2]	-	75	A
		T_{mb} = 100 °C; V_{GS} = 10 V; see Figure 2	[2]	-	75	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq$ 10 µs; see Figure 3		-	620	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 1		-	272	W
$I_{GS(CL)}$	gate-source clamping current	continuous		-	10	mA
		t_p = 5 ms; δ = 0.01		-	50	mA
$V_{isol(FET-TSD)}$	FET to temperature sense diode isolation voltage			-	±100	V
T_{stg}	storage temperature			–55	+175	°C
T_j	junction temperature			–55	+175	°C
Source-drain diode						
I_{DR}	reverse drain current	T_{mb} = 25 °C	[1]	-	155	A
			[2]	-	75	A
I_{DRM}	peak reverse drain current	T_{mb} = 25 °C; pulsed; $t_p \leq$ 10 µs		-	620	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 75 A; $V_{DS} \leq$ 40 V; V_{GS} = 10 V; R_{GS} = 50 Ω; starting at T_j = 25 °C		-	1.46	J
Electrostatic discharge						
V_{esd}	electrostatic discharge voltage, pins 1, 2, 4, 6, 7	Human Body Model; C = 100 pF; R = 1.5 kΩ		-	6	kV

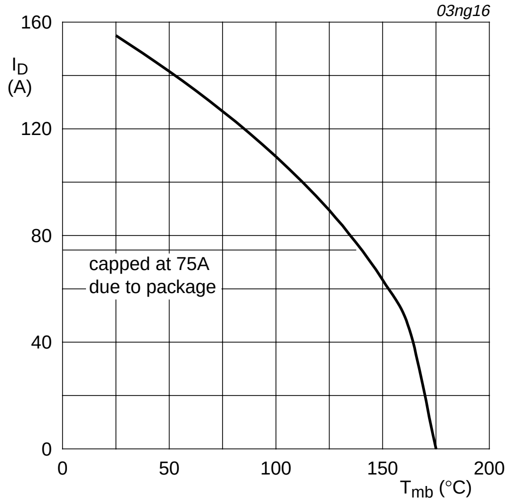
[1] Current is limited by power dissipation chip rating.

[2] Continuous current is limited by package.



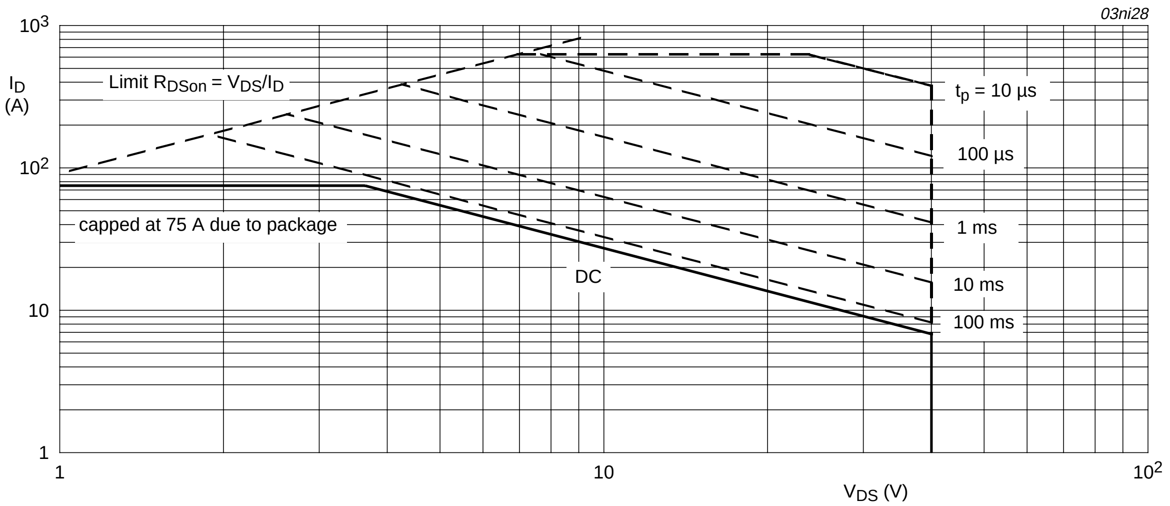
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\ \%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 10$ V

Fig 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	-	-	50	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.55	K/W

[1] Mounted on printed-circuit board; minimum footprint

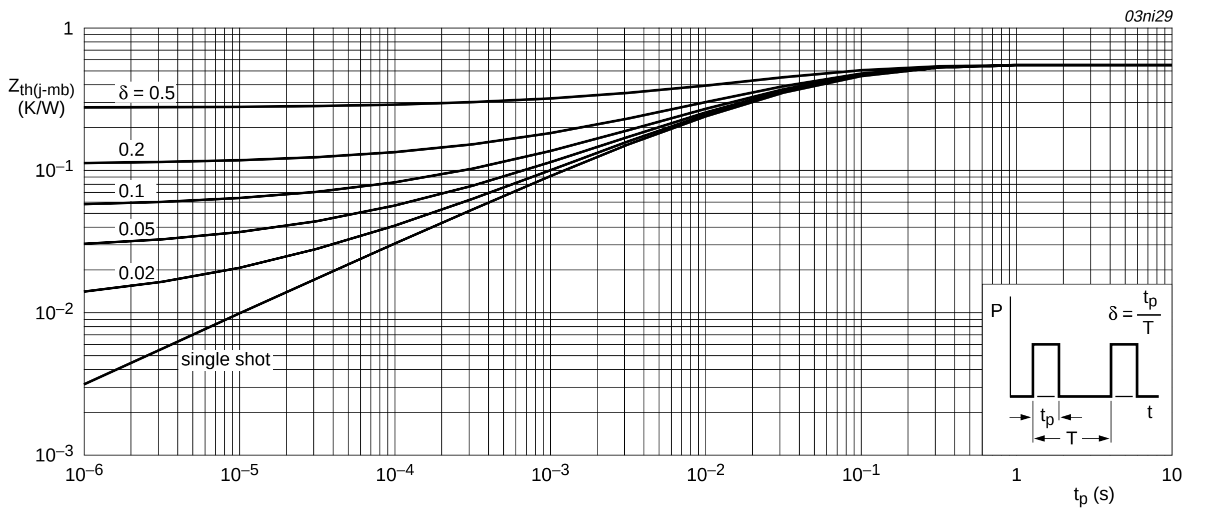


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 5: Characteristics

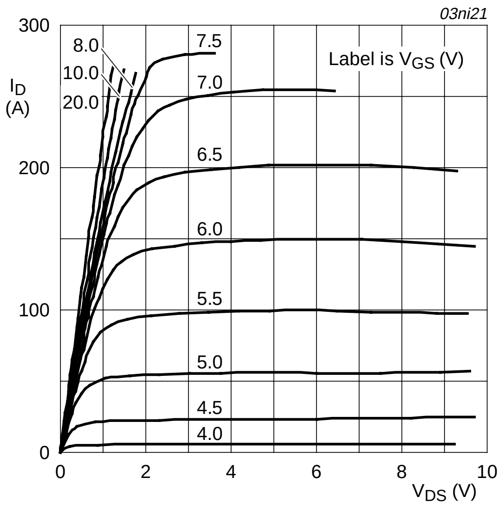
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V				
		T_j = 25 °C	40	-	-	V
		T_j = –55 °C	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; see Figure 9				
		T_j = 25 °C	2	3	4	V
		T_j = 175 °C	1	-	-	V
		T_j = –55 °C	-	-	4.4	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.1	10	µA
		T_j = 175 °C	-	-	250	µA
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = ±1 mA; –55 °C < T_j < +175 °C	20	22	-	V
I_{GSS}	gate leakage current	V_{GS} = ±10 V; V_{DS} = 0 V				
		T_j = 25 °C	-	22	1000	nA
		T_j = 175 °C	-	-	10	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 50 A; see Figure 7 and 8				
		T_j = 25 °C	-	4.7	6	mΩ
		T_j = 175 °C	-	-	11.4	mΩ
V_F	forward voltage of temperature sense diode	I_F = 250 µA	648	658	668	mV
S_F	temperature coefficient of temperature sense diode	I_F = 250 µA; –55 °C < T_j < +175 °C	–1.4	–1.54	–1.68	mV/K
V_{hys}	forward voltage hysteresis of temperature sense diode	125 µA < I_F < 250 µA	25	32	50	mV
I_D/I_{sense}	ratio of drain current to sense current	V_{GS} = 10 V; –55 °C < T_j < +175 °C	585	615	645	
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	V_{GS} = 10 V; V_{DS} = 32 V; I_D = 25 A; see Figure 14	-	120	-	nC
Q_{GS}	gate-source charge	V_{GS} = 10 V; V_{DS} = 32 V; I_D = 25 A; see Figure 14	-	19	-	nC
Q_{GD}	gate-drain charge	V_{GS} = 10 V; V_{DS} = 32 V; I_D = 25 A; see Figure 14	-	50	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; see Figure 12	-	4300	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; see Figure 12	-	1400	-	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; see Figure 12	-	820	-	pF

Table 5: Characteristics *...continued*

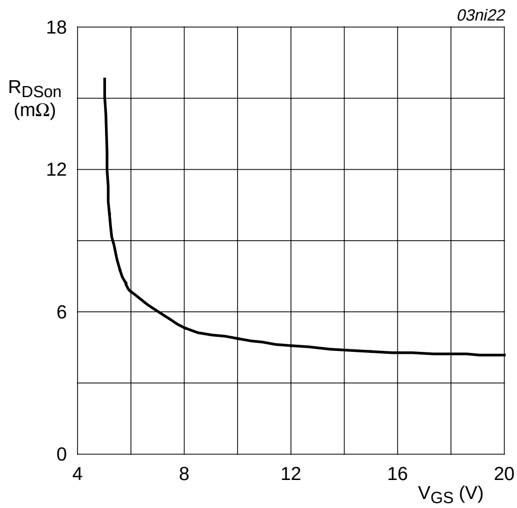
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	V_{DD} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; R_G = 10 Ω	-	35	-	ns
t_r	rise time	V_{DD} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; R_G = 10 Ω	-	115	-	ns
$t_{d(off)}$	turn-off delay time	V_{DD} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; R_G = 10 Ω	-	155	-	ns
t_f	fall time	V_{DD} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; R_G = 10 Ω	-	110	-	ns
L_D	internal drain inductance	measured from upper edge of drain mounting base to center of die	-	2.5	-	nH
L_S	internal source inductance	measured from source lead to source bond pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 40 A; V_{GS} = 0 V; see Figure 18	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs; V_{GS} = –10 V; V_{DS} = 30 V	-	96	-	ns
Q_r	recovered charge	I_S = 20 A; dI_S/dt = –100 A/µs; V_{GS} = –10 V; V_{DS} = 30 V	-	224	-	nC



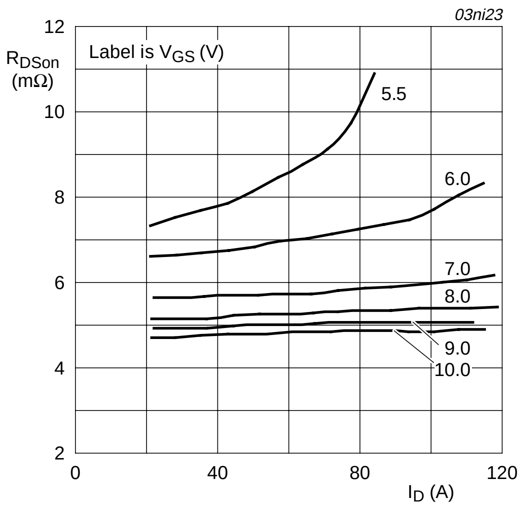
T_j = 25 °C; t_p = 300 µs

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



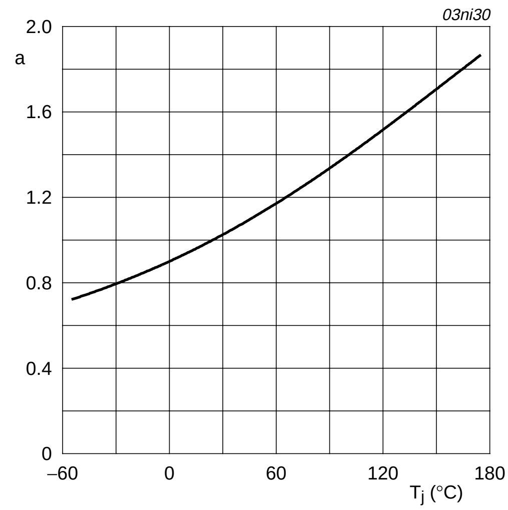
T_j = 25 °C; I_D = 50 A

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



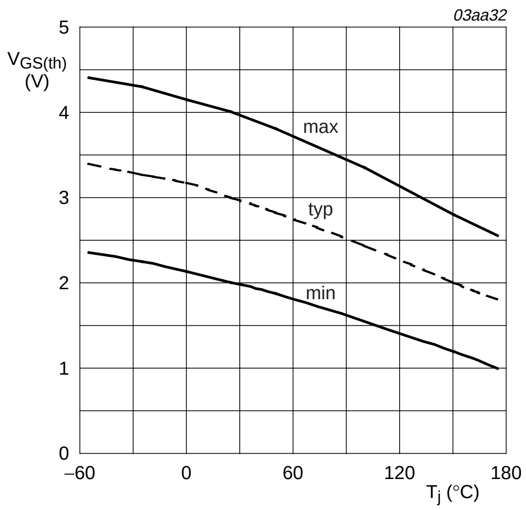
$T_j = 25\ °C$; $t_p = 300\ \mu s$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



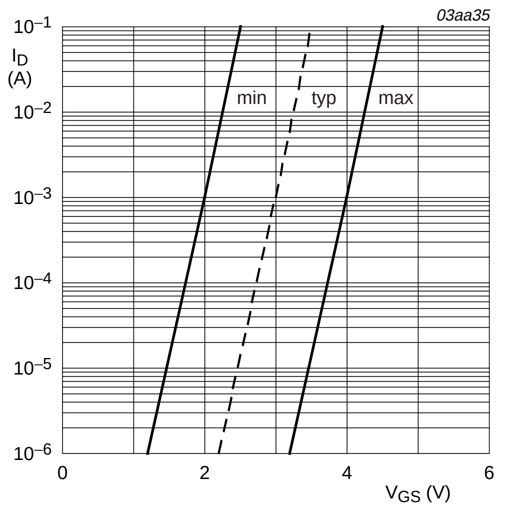
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



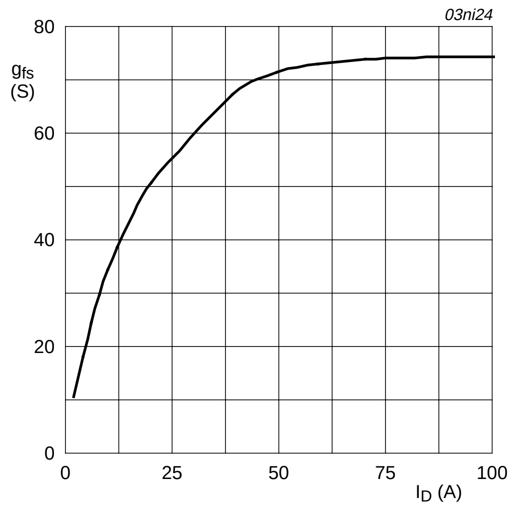
$I_D = 1\ mA$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



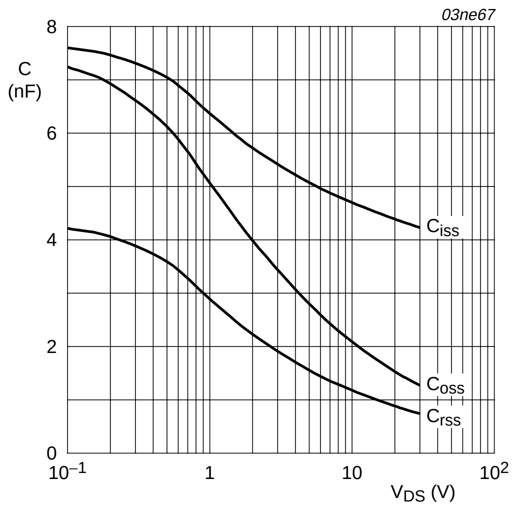
$T_j = 25\ °C$; $V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



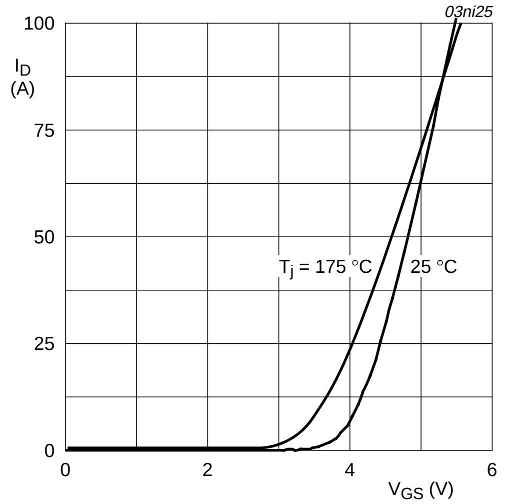
T_j = 25 °C; V_{DS} = 25 V

Fig 11. Forward transconductance as a function of drain current; typical values



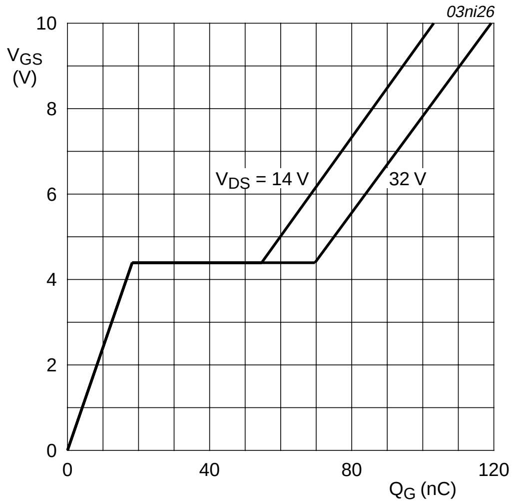
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



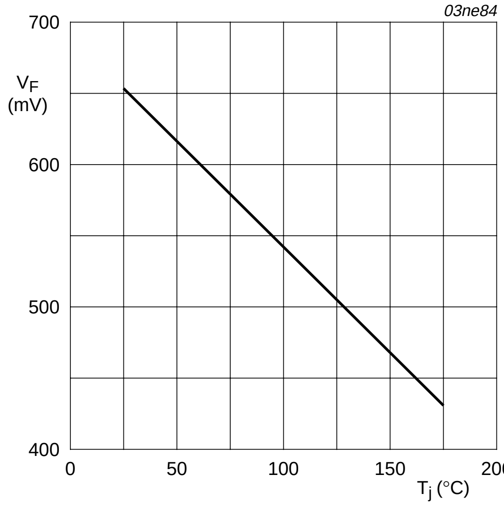
V_{DS} = 25 V

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values



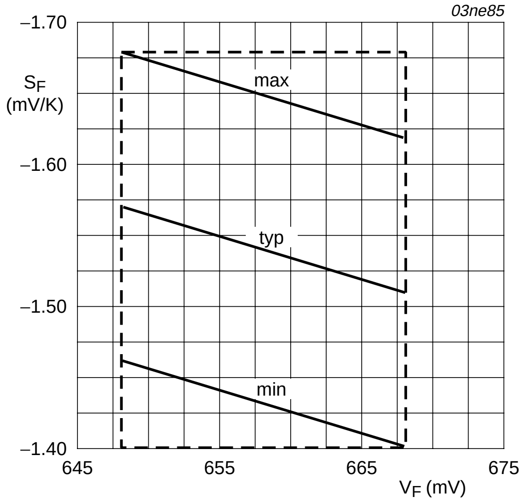
T_j = 25 °C; I_D = 25 A

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values



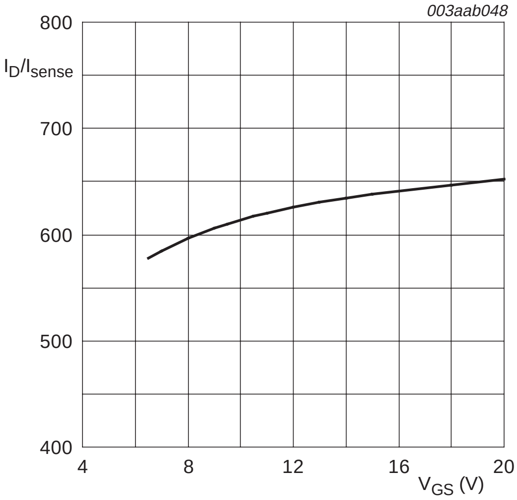
I_F = 250 µA

Fig 15. Forward voltage of temperature sense diode as a function of junction temperature; typical values



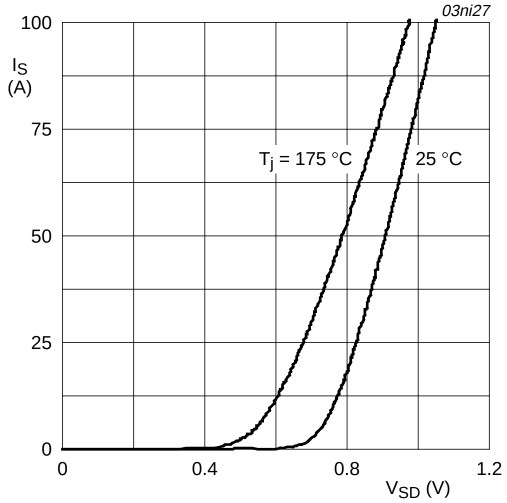
V_F at T_j = 25 °C; I_F = 250 µA

Fig 16. Temperature coefficient of temperature sense diode as a function of forward voltage; typical values



I_D = 25 A

Fig 17. Drain-sense current ratio as a function of gate voltage; typical values

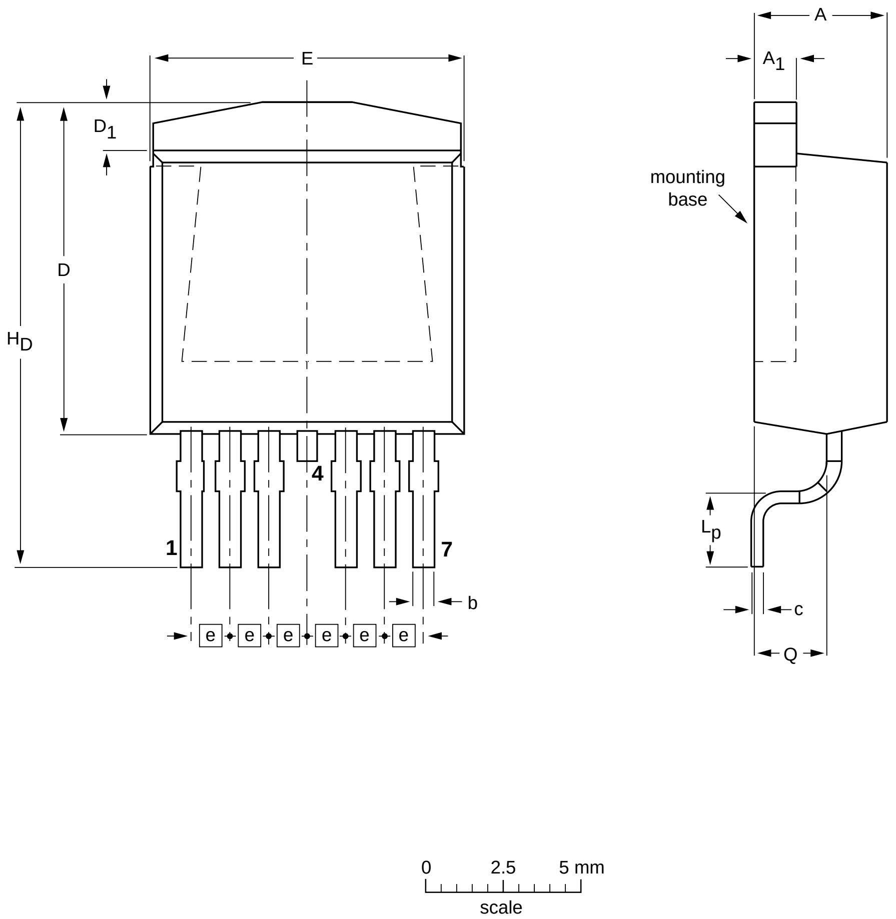


V_{GS} = 0 V

Fig 18. Source (diode forward) current as function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface mounted package (D2PAK); 7 leads (one lead cropped) **SOT427**



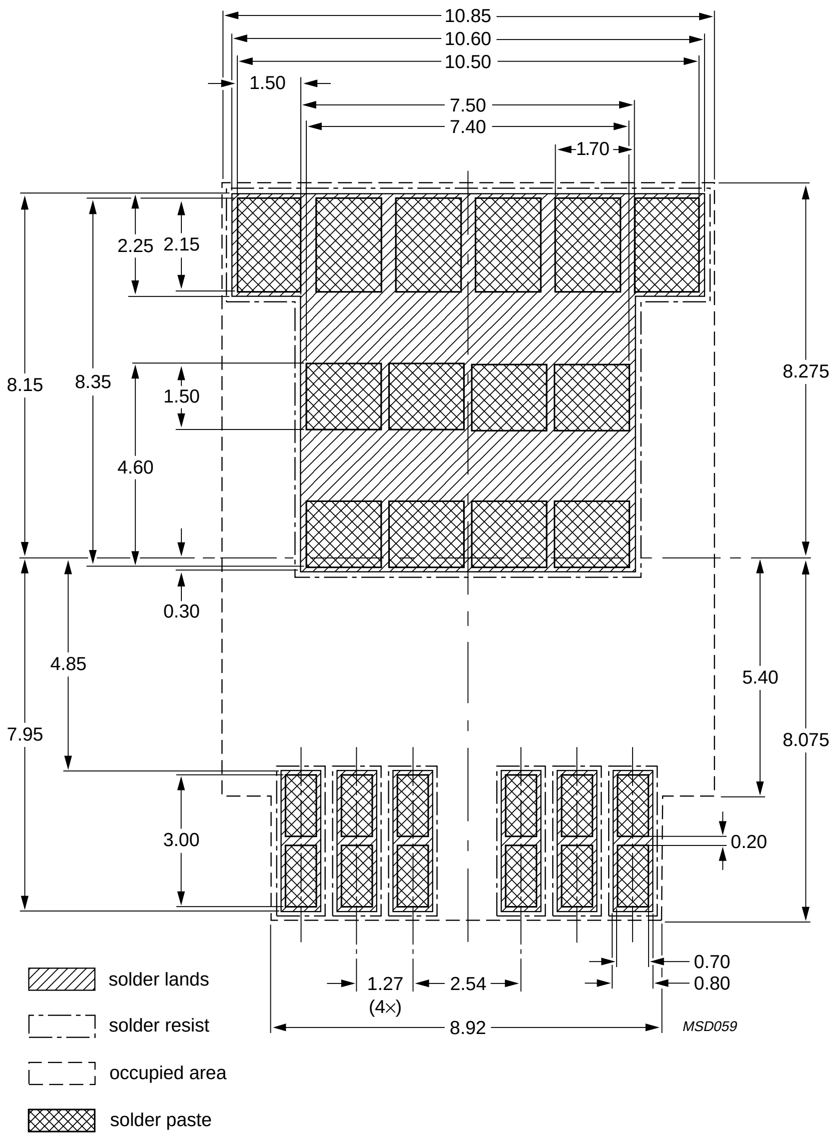
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	1.27	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT427						~~04-10-13~~ 05-03-09

Fig 19. Package outline SOT427 (D2PAK)

8. Soldering



Dimensions in mm

Fig 20. Reflow soldering footprint for SOT427

9. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
BUK7C06-40AITE_4	20050623	Product data sheet	-	-	BUK7C06-40AITE_3
Modifications:	• Figure 16: graph corrected				
BUK7C06-40AITE_3	20050616	Product data sheet	-	9397 750 15176	BUK7C06_40AITE-02
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Section 1 "Product profile" and Table 5: I_D/I_{sense} values changed. • Figure 17: graph changed.				
BUK7C06_40AITE-02	20040129	Product data	-	9397 750 12487	BUK7C06_40AITE-01
Modifications:	• Section 3 "Ordering information" added • Section 1 and Table 5: R_{DSon} typical value changed • Section 1 and Table 5: I_D/I_{sense} typical value changed • Table 5: $Q_{g(tot)}$, Q_{gs} and Q_{gd} typical values changed • Table 5: C_{iss}, C_{oss} and C_{rss} typical values changed • Figure 5, 6, 7, 11, 13, 17, 18: graphs changed				
BUK7C06_40AITE-01	20020717	Product data	-	9397 750 09873	-

10. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

11. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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15. Contents

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