Intersil HSP43220 Decimating Digital Filter Development Software

Intersil DECIMATE Development Software assists the design engineer to prototype designs for the Intersil HSP43220 Decimating Digital filter (DDF). Developed specifically for the DDF, this software consists of three integrated modules: DDF Design, DDF Simulator and DDF PROM. The Design module designs a filter from a set of user specifications for the DDF. The Simulator module models the DDF's internal operation. The PROM module uses the device configuration created by the Design module to build a PROM data file that can be used to store and download the DDF configuration.

DDF System Design

The DDF consists of two stages: a High Decimation Filter (HDF) and a Finite Impulse Response (FIR) filter. Together these provide a unique narrow band, low pass filter. Because of this unique architecture, special software is required to configure the device for a given set of filter parameters. This software uses system level filter parameters (listed below) to perform the trade off analysis and calculate the values for the DDF's Configuration Registers and FIR coefficients.

Design specifications are supplied by the user in terms of:

1. Input sample frequency.
2. Required output sample frequency.
3. Passband signal bandwidth.
4. Transition bandwidth.
5. Amount of attenuation allowed in the passband.
6. Amount of stopband attenuation required for signals outside of the band of interest.

This information is entered into a menu screen (See Figure 1), providing immediate feedback on the design validity. The design module calculates the order of the HDF, HDF decimation required, the FIR input data rate, minimum clock frequency for the FIR, FIR order and decimation required in the FIR.

The design module will then generate the FIR filter. Four different methods are provided for the FIR design:

1. A Standard FIR automatically designed by the module using the Parks-McClellan method to compute the coefficients of an equiripple (Chebyshev) filter.
2. Any FIR imported into the Design module from another FIR design program.
3. A precompensated FIR which is automatically designed by the module to compensate for the roll-off in the passband of the HDF frequency response.
4. The FIR may also be bypassed in which case the optimal HDF is designed from the user specifications.

Frequency response curves are then displayed showing the resulting responses in the HDF, FIR and for the entire chip using the given filter design. Figure 2 is a typical display. The user may save this frequency response data for further analysis. The design module also creates a report file documenting the filter design and providing the coefficients and setup register values for programming the device.

DDF Simulator

The simulator provides an accurate simulation of the device before any hardware is built. It can be used to simulate any filter designed with DECIMATE. The simulator takes into account the fixed point bus widths and pipeline delays for every element in the DDF.

The simulator provides the user with an input signal which can be used to stimulate the filter. This signal is created from the options shown in Table 1. The user can select a pure step, impulse, cosine, chirp, uniform or Gaussian noise as the input signal, or a more complex signal can be generated by combining that data with an option selected from the Signal #2 column, with the combining operator chosen from the middle column. The user can also import a signal from an outside source.

TABLE 1.

SIGNAL #1	OPERATION	SIGNAL #2
Step		Step
Impulse	No Operation	Impulse
COSINE	Add	COSINE
Chirp	Concatenate	Chirp
Uniform Noise	Multiply	Uniform Noise
Gaussian Noise		Gaussian Noise
Imported From Outside		

Probes are provided to select specific areas to graphically display data values, as well as save into data files for further processing. The DDF Simulator has two levels; the DDF Simulator Specification Screen and the DDF Simulator Main Screen.

The Specification Screen (see Figure 3) is used to input the simulation parameters. The user selects display modes in either continuous or decimated format and data formats in either decimal or hexadecimal. The Specification Screen also provides for selection of the input signal.

The simulator main screen (see Figure 4) defines the simulator test probes and displays the data values per clock cycle. The interactive simulator screen consists of the HSP43220 Block Diagram, test probes and register

contents. The user selects the step size of the input sample clock and also selects the probes to be monitored. The simulator will then clock through the specified number of clock cycles and display the resulting time domain response. Figure 5 shows a typical probe display.

Monarch 2.0 DSP Design Software

DECIMATE is fully integrated with Monarch 2.0 professional DSP design software. Monarch is a full featured DSP package with FIR IIR filter design and analysis, two dimensional and three dimensional viewing, a programmable signal/systems laboratory with 100 + DSP/Math functions, extensive fixed-point support and FFTs/IFETs Monarch is available separately from The Athena Group, Inc.

When used with Monarch 2.0, DECIMATE becomes a full feature design environment for a DSP system. Data can easily be transferred from DECIMATE modules to the Monarch modules for further analysis.

System Requirements

IBM PC™, XT™, AT™, PS/2 computer or 100% compatible with 640K RAM running MS/PC-DOS 2.0 or higher One MegaByte of fixed-disk space with 5.25” or 3.5” floppy drive. CGA, MCGA, EGA, VGA, 8514, or Hercules Graphics Adapter. A Math coprocessor is strongly recommended.

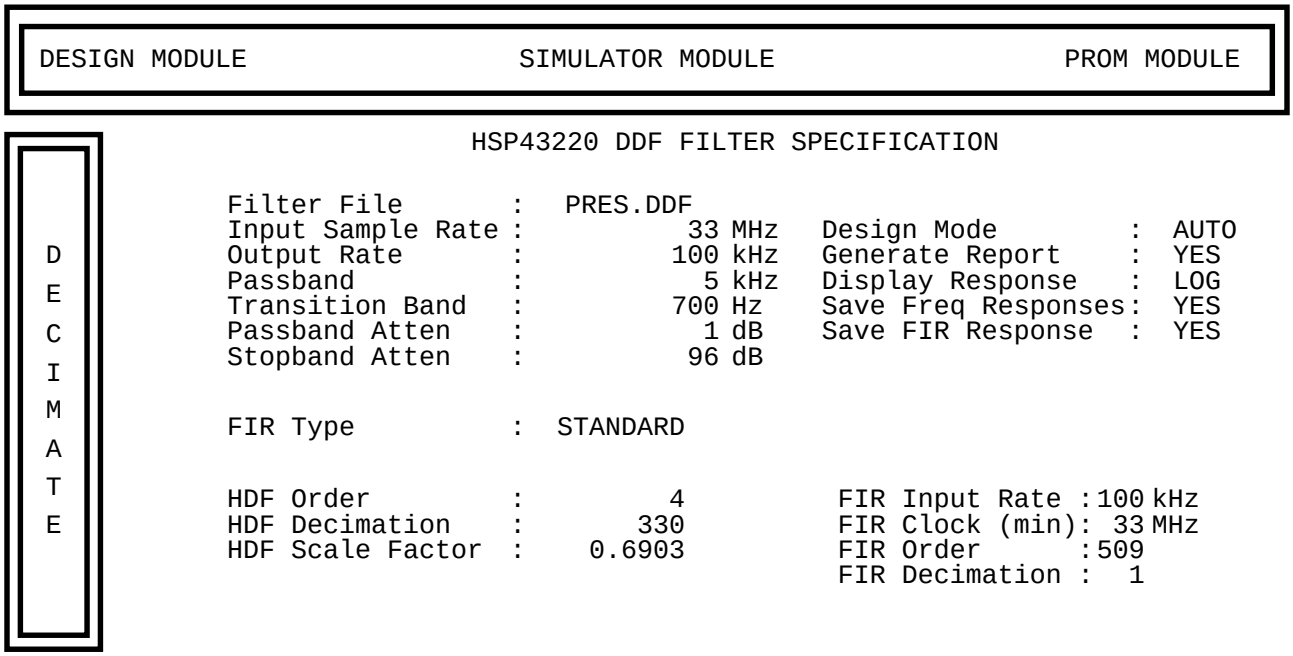

FIGURE 1. FILTER SPECIFICATION MENU

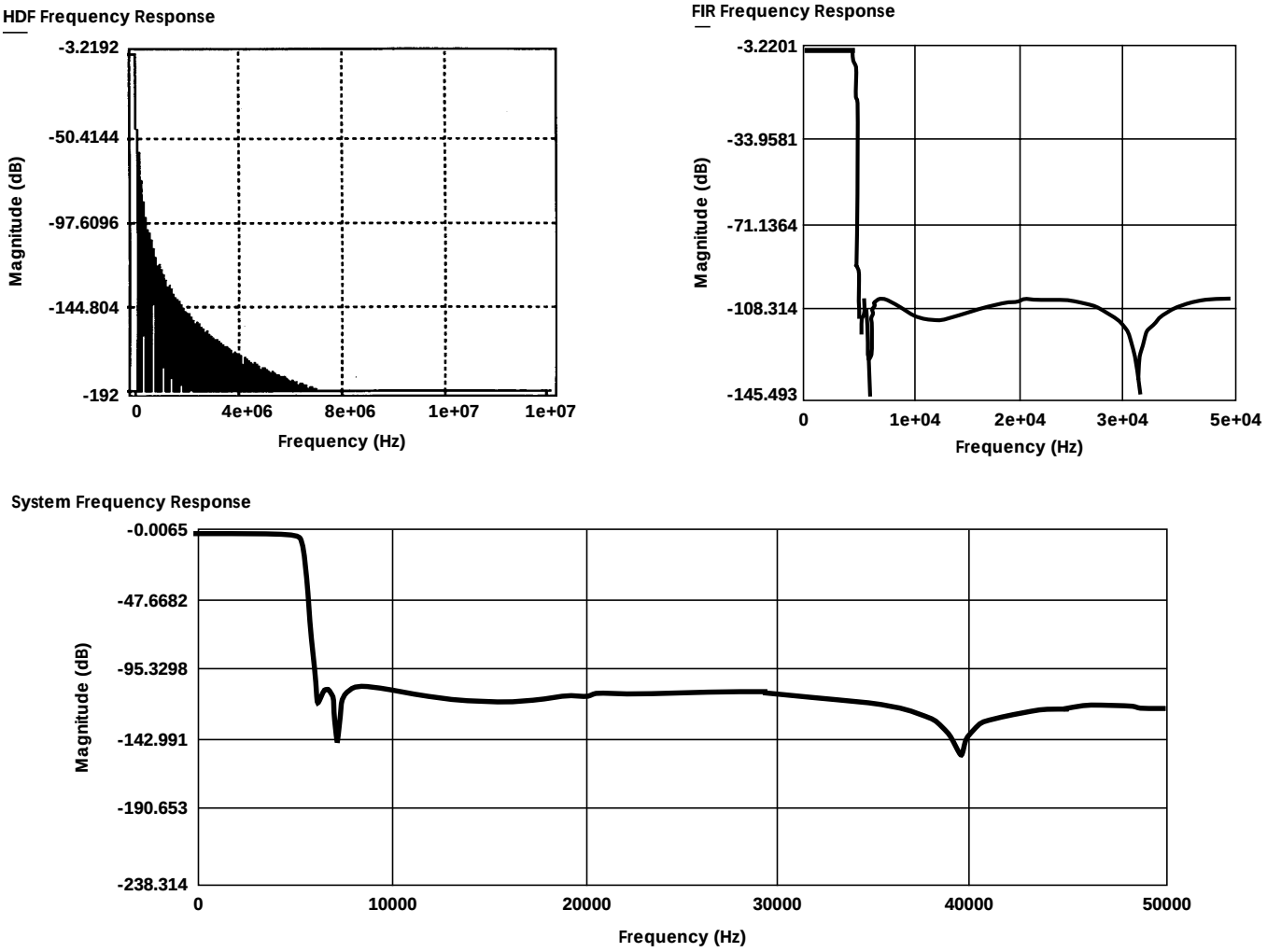

FIGURE 2. FREQUENCY DISPLAY

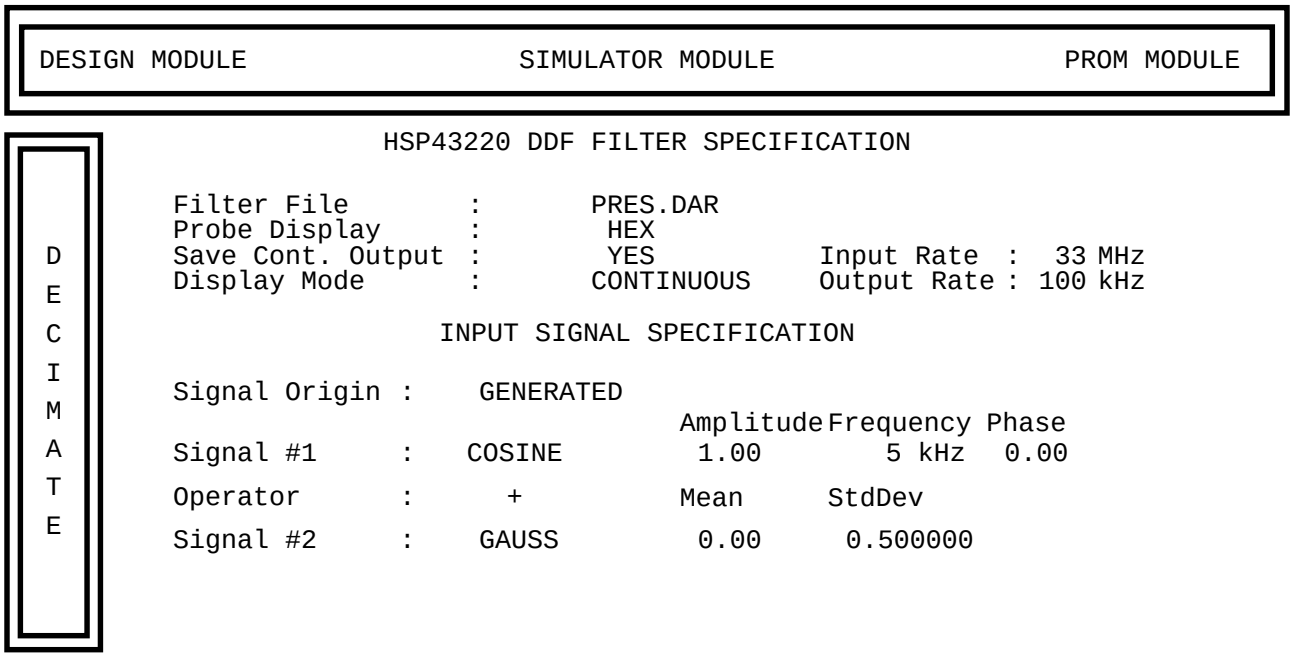

FIGURE 3. SPECIFICATION MENU

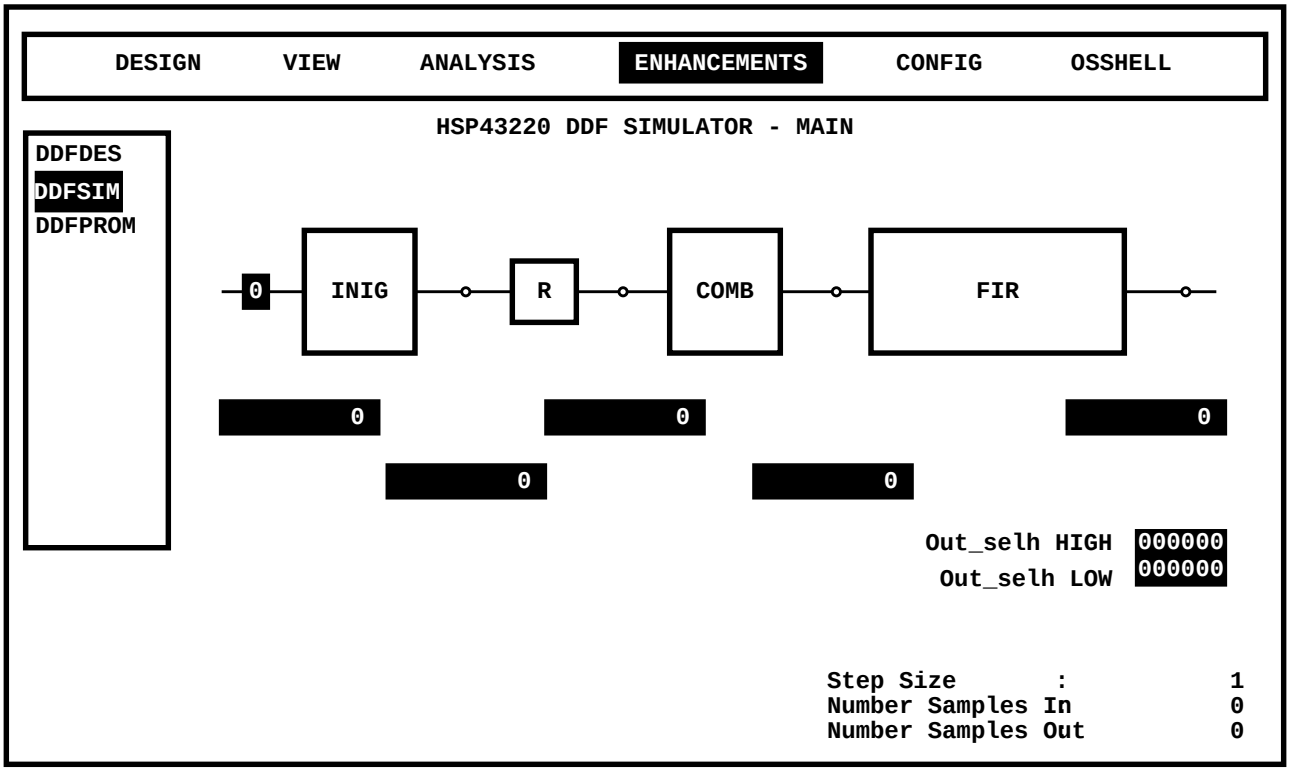

FIGURE 4. SIMULATOR - MAIN MENU

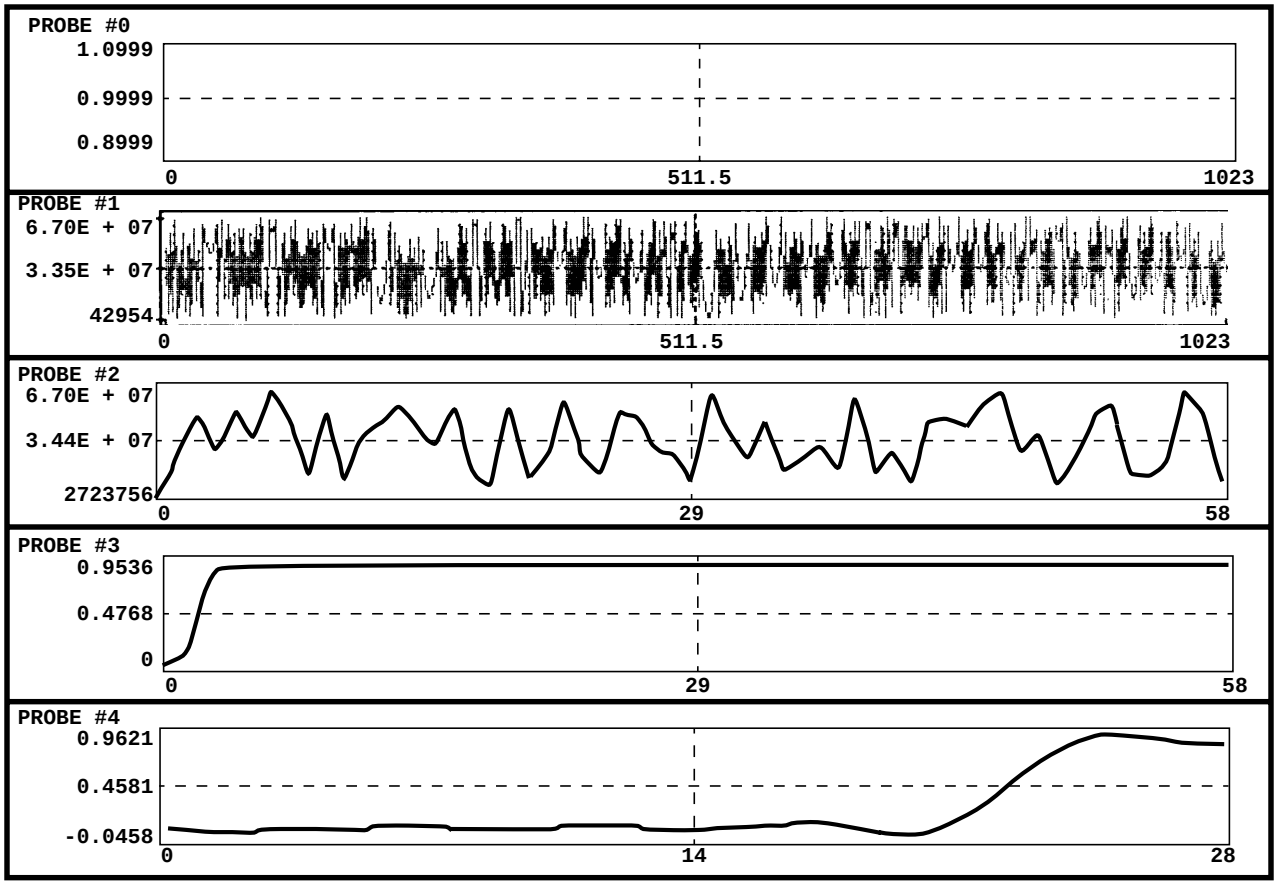

FIGURE 5. SIMULATOR PROBE DISPLAY

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