Design Idea DI-52

DPA-Switch™

60 W DC-DC Converter

Application	Device	Power Output	Input Voltage	Output Voltage	Topology
Telecom	DPA426R	60 W	36-75 VDC	12 V	Forward Sync. Rect.

Design Highlights

- Low component count
- High efficiency: 91.5% at 36 VDC using synchronous rectification
- Capacitor coupled synchronous rectification allows higher output voltages without overstressing MOSFET gates
- No current sense resistor or current transformer required
- Output overload, open loop and thermal protection
- 300 kHz switching frequency to allow sufficient transformer reset time
- 3.55 x 2.1 x 0.6 inch (approx. 13.4 W/cubic inch)

Operation

DPA-Switch greatly simplifies the design compared to a discrete implementation. The capacitor coupled synchronous rectifier drive used in this design is useful for higher voltage outputs, still allowing passive MOSFET drive without gate overvoltage, which would result from direct resistor drive.

Resistor R1 programs the under/over voltages and linearly reduces the maximum duty cycle with input voltage to prevent core saturation during load transients. Components D1, D2, C9, and L2 implement a resonant clamp circuit to catch and re-circulate the transformer leakage energy during normal operation, with Zener VR1 providing absolute clamping for transient conditions.

Capacitor C21 charges the gate of Q2, the forward synchronous rectifier MOSFET. Resistor R21 limits gate oscillation and R22 provides gate pull down. Zener diode VR20 limits the Q2 gate voltage during conduction and also reverse charges (resets) C21 during the Q2 off time.

A similar drive technique is used for the catch synchronous rectifier MOSFET Q1 (with C22, R23, R24, and VR21). MOSFET Q1 is driven by the transformer (T1) reset voltage and operates only when Q2 is off. Diode D20 provides a

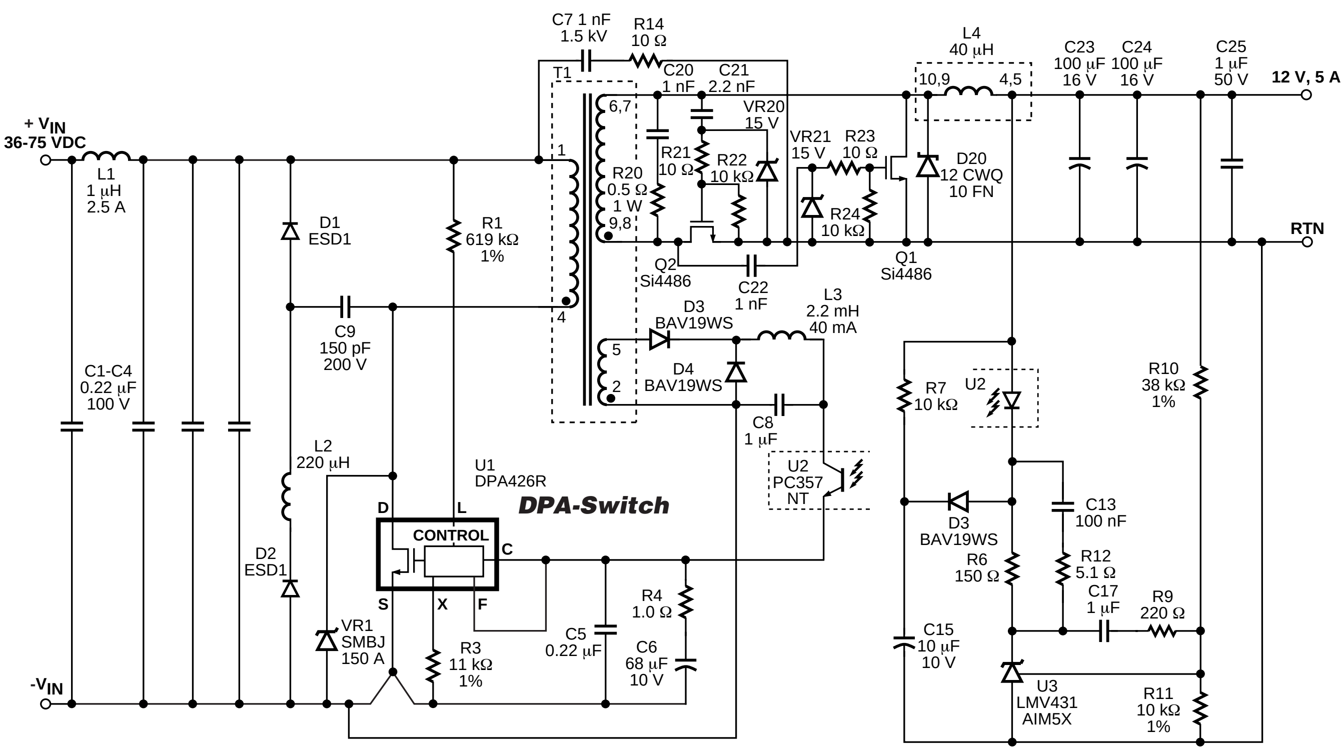

Figure 1. DPA426R - 60 W, 12 V, 5 A, DC-DC Converter.

conduction path for the output inductor (L4) current when the transformer reset is complete.

Key Design Points

- Transformer core reset is critical in this design. MOSFET gate loading will affect the transformer-reset waveform. Capacitors C20, C22 and C_{Q1GS} will all load transformer reset. Choose values to ensure sufficient reset at low line and safe maximum drain voltage at high line. Also use 300 kHz operation for longest reset time.
- Capacitors C20 and C22 will capacitively drive MOSFET gate capacitances C_{Q2GS} and C_{Q1GS}, respectively. C20 and C22 should be chosen to ensure that gate drive voltage attains turn-on threshold of MOSFET (Vg_{TH}) at worst case conditions (low line for forward MOSFET).
- Reduce transformer leakage inductance by filling each winding layer across the entire width of the bobbin.

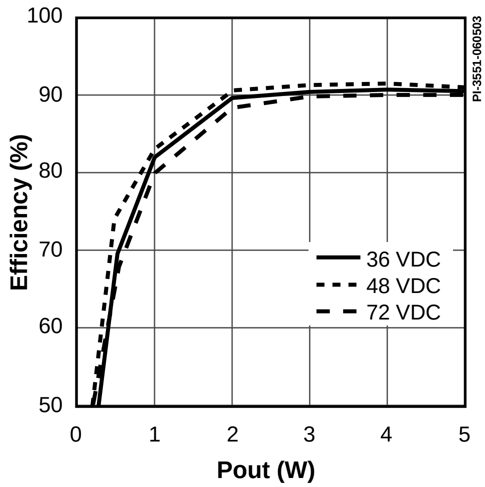

Figure 2. Efficiency vs. Output Power.

TRANSFORMER PARAMETERS	
Core Material	Ferroxcube P/N: EFD25, ungapped
Bobbin	10-pin EFD25 surface mount bobbin
Winding Details	Primary 5T + 5T, 4 x 26 AWG Bias 5T, 1 x 30 AWG 12 V 6T, 4 x 26 AWG
Winding Order and Pin Numbers	Bias (2-5), Primary-1 (4-NC), 12 V (9,10-6,7), Primary-2 (NC-1)
Primary Inductance	Pin (1-4): 190 μH ±25% @ 300 kHz
Primary Resonant Frequency	3.8 MHz (minimum)
Leakage Inductance	1 μH (maximum)

Table 1. Transformer Construction Information.

INDUCTOR PARAMETERS	
Core Material	Ferroxcube P/N: EFD20-3F3 gap for inductance required
Bobbin	10-pin EFD20 surface mount bobbin
Winding Details	Main 18T, 3 x 24 AWG
Winding Order and Pin Numbers	Main (4,5-9,10)
Inductance	Pin (4,5-9,10): 40 μH ±10% @ 300 kHz

Table 2. L4 Output Inductor Design Parameters.

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