

# FDZ2552P

## Dual P-Channel 2.5V Specified PowerTrench™ BGA MOSFET

### General Description

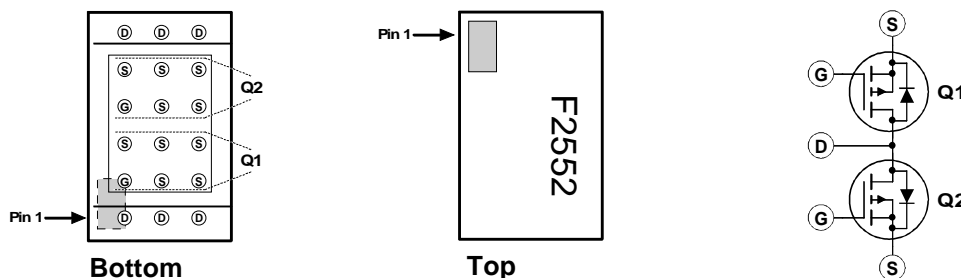
Combining Fairchild's advanced 2.5V specified PowerTrench process with state of the art BGA packaging, the FDZ2552P minimizes both PCB space and  $R_{DS(ON)}$ . This dual BGA MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultra-low profile packaging, low gate charge, and low  $R_{DS(ON)}$ .

### Applications

- Battery management
- Load switch
- Battery protection

### Features

- -6 A, -20 V.  $R_{DS(ON)} = 0.045 \Omega @ V_{GS} = -4.5 V$   
 $R_{DS(ON)} = 0.075 \Omega @ V_{GS} = -2.5 V$ .
- Occupies only 0.10 cm<sup>2</sup> of PCB area.  
1/3 the area of SO-8.
- Ultra-thin package: less than 0.70 mm height when mounted to PCB.
- Outstanding thermal transfer characteristics: significantly better than SO-8.
- Ultra-low  $Q_g \times R_{DS(ON)}$  figure-of-merit.
- High power and current handling capability.



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DSS}$	Drain-Source Voltage	-20	V
$V_{GSS}$	Gate-Source Voltage	±12	V
$I_D$	Drain Current – Continuous (Note 1a)	-6	A
	– Pulsed	-20	
$P_D$	Power Dissipation (Steady State) (Note 1a)	3.0	W
$T_J, T_{stg}$	Operating and Storage Junction Temperature Range	-55 to +175	°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	8	°C/W

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
F2552	FDZ2552P	TBD	TBD	TBD

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		28		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage Current, Forward	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
$I_{GSSR}$	Gate–Body Leakage Current, Reverse	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			100	nA

**On Characteristics** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.4	-0.9	-1.5	V
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -4.5\text{ V}, I_D = -6\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -4.5\text{ A}$		0.036 0.060	0.045 0.075	$\Omega$

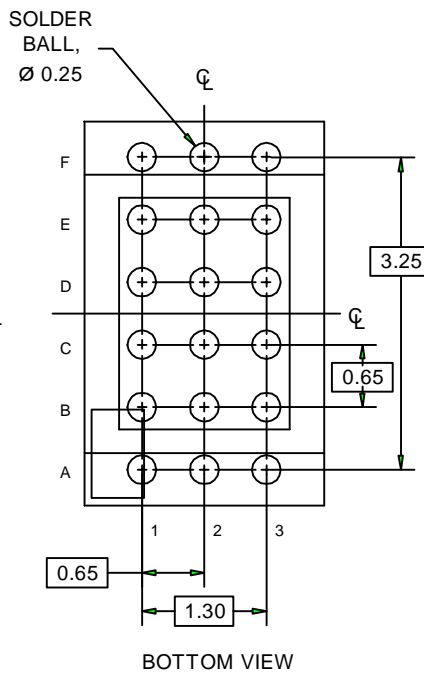
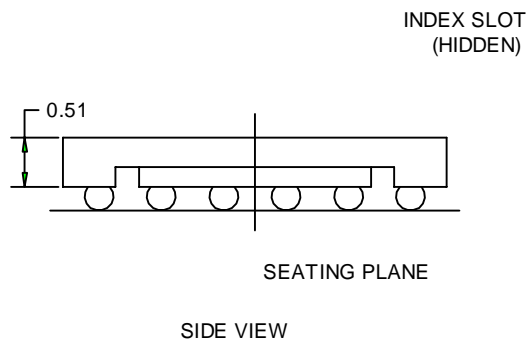
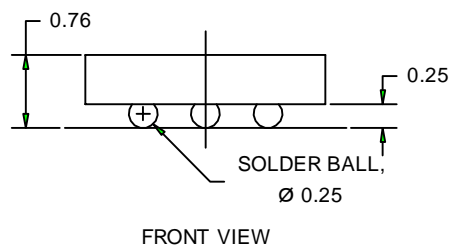
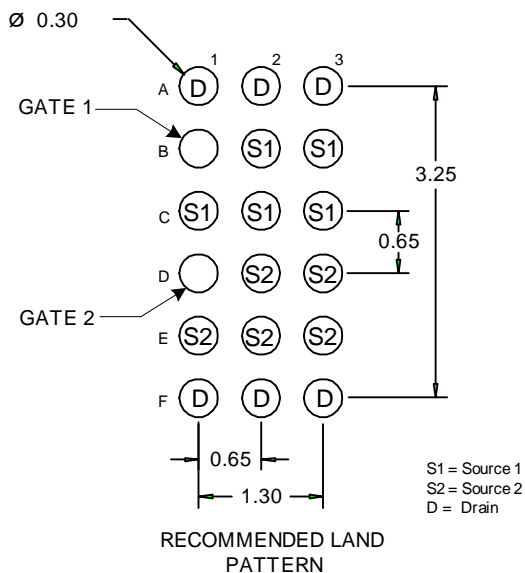
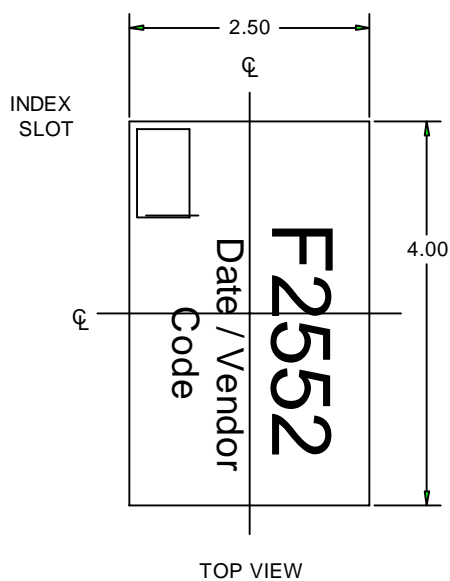
**Drain–Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain–Source Diode Forward Current				-2.5	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -2.5\text{ A}$ (Note 2)		-0.77	-1.2	V

**Notes:**

- $R_{\theta JA}$  is a function of the junction-to-case ( $R_{\theta JC}$ ), case-to-ambient ( $R_{\theta CA}$ ) and the PC Board ( $R_{\theta BA}$ ) thermal resistance where the case thermal reference is defined the top surface of the package.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  and  $R_{\theta BA}$  are determined by the user's design. Maximum current ratings assume single device operation.
  - $R_{\theta JA} = 50^\circ\text{C/W}$  (steady-state) when mounted on 1 in<sup>2</sup> of 2 oz. copper.
- Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

### Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.

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GTO™	SuperSOT™-6	
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