

International
IR Rectifier
RADIATION HARDENED
LOGIC LEVEL POWER MOSFET
THRU-HOLE (TO-39)

PD - 94695

IRHLF670Z4
60V, N-CHANNEL
R₆ TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	ID
IRHLF670Z4	100K Rads (Si)	0.5Ω	1.6A*
IRHLF630Z4	300K Rads (Si)	0.5Ω	1.6A*
IRHLF640Z4	600K Rads (Si)	0.5Ω	1.6A*
IRHLF680Z4	1000K Rads (Si)	0.5Ω	1.6A*



International Rectifier's R6™ Logic Level Power Mosfets provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

These devices are used in applications such as current boost low signal source in PWM, voltage comparator and operational amplifiers.

Features:

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight
- Complimentary P-Channel Available - IRHLF6970Z4

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
ID @ VGS = 4.5V, TC = 25°C	Continuous Drain Current	1.6*	A
ID @ VGS = 4.5V, TC = 100°C	Continuous Drain Current	1.0*	
IDM	Pulsed Drain Current ①	6.4	
PD @ TC = 25°C	Max. Power Dissipation	5.0	W
	Linear Derating Factor	0.04	W/°C
VGS	Gate-to-Source Voltage	±10	V
EAS	Single Pulse Avalanche Energy ②	9.0	mJ
IAR	Avalanche Current ①	1.6	A
EAR	Repetitive Avalanche Energy ①	0.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Lead Temperature	300 (0.063in/1.6mm from case for 10s)	
	Weight	0.98 (Typical)	g

* Derated to match the Complimentary P-Channel Logic Level Power Mosfet -IRHLF6970Z4

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.08	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.50	Ω	V _{GS} = 4.5V, I _D = 1.0A ④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	2.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	1.1	—	—	S (Ω)	V _{DS} = 10V, I _{DS} = 1.0A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	μA	V _{DS} = 48V, V _{GS} = 0V
		—	—	10		V _{DS} = 48V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -10V
Q _g	Total Gate Charge	—	—	3.6	nC	V _{GS} = 5.0V, I _D = 1.6A V _{DS} = 30V
Q _{gs}	Gate-to-Source Charge	—	—	1.5		
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	1.8		
t _{d(on)}	Turn-On Delay Time	—	—	8.0	ns	V _{DD} = 30V, I _D = 1.6A, V _{GS} = 5.0V, R _G = 24Ω
t _r	Rise Time	—	—	20		
t _{d(off)}	Turn-Off Delay Time	—	—	20		
t _f	Fall Time	—	—	15		
L _S + L _D	Total Inductance	—	7.0	—	nH	Measured from Drain lead (6mm /0.25in from package) to Source lead(6mm/0.25in from package)with Source wire internally bonded from Source pin to Drain pad
C _{iss}	Input Capacitance	—	152	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	39	—		
C _{rss}	Reverse Transfer Capacitance	—	1.6	—		
R _g	Gate Resistance	—	14	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	1.6*	A	T _j = 25°C, I _S = 1.6A, V _{GS} = 0V ④
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	6.4		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _j = 25°C, I _F = 1.6A, di/dt ≤ 100A/μs
t _{rr}	Reverse Recovery Time	—	—	100	ns	V _{DD} ≤ 25V ④
Q _{RR}	Reverse Recovery Charge	—	—	150	nC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

* Derated to match the Complimentary P-Channel Logic Level Power Mosfet -IRHLF6970Z4

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	25	°C/W	

Note: Corresponding Spice and Saber models are available on International Rectifier Web site.

For footnotes refer to the last page

Radiation Characteristics

IRHLF670Z4

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Parameter	Up to 600K Rads(Si) ¹	1000K Rads (Si) ²		Units	Test Conditions		
		Min	Max			Min	Max
BV _{DSS}	Drain-to-Source Breakdown Voltage	60	—	60	—	V	V _{GS} = 0V, I _D = 250μA
V _{GS(th)}	Gate Threshold Voltage	1.0	2.0	1.0	2.0		V _{GS} = V _{DS} , I _D = 250μA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	V _{GS} = 10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100	—	-100		V _{GS} = -10V
I _{DSS}	Zero Gate Voltage Drain Current	—	1.0	—	10	μA	V _{DS} = 48V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source On-State Resistance (TO-39)	—	0.5	—	0.5	Ω	V _{GS} = 4.5V, I _D = 1.0A
V _{SD}	Diode Forward Voltage ④	—	1.2	—	1.2	V	V _{GS} = 0V, I _S = 1.6A

1. Part numbers IRHLF670Z4, IRHLF630Z4 and IRHLF640Z4

2. Part number IRHLF680Z4

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)							
				@VGS= 0V	@VGS= -2V	@VGS= -4V	@VGS= -5V	@VGS= -6V	@VGS= -7V	@VGS= -8V	@VGS= -10V
Br	37.3	285	36.8	60	60	60	60	60	35	30	20
I	59.9	345	32.7	60	60	60	60	60	20	15	-
Au	82.3	357	357	60	60	60	60	-	-	-	-

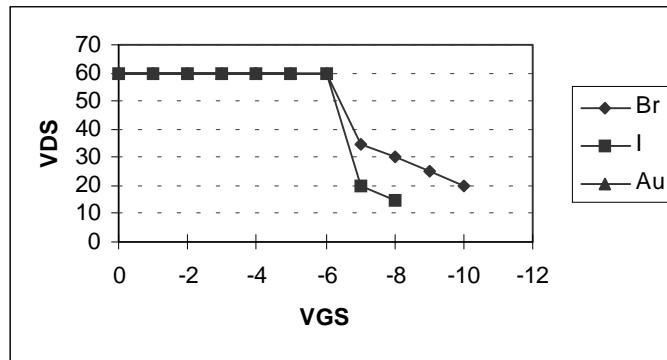


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

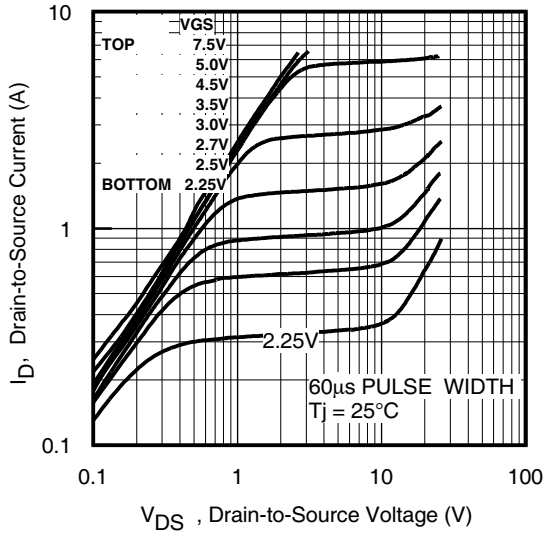


Fig 1. Typical Output Characteristics

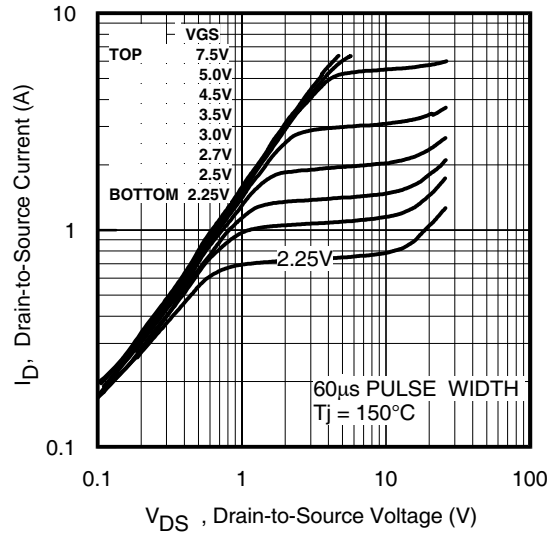


Fig 2. Typical Output Characteristics

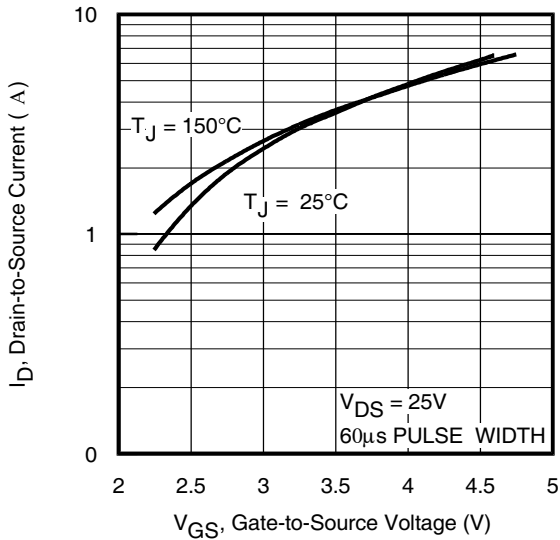


Fig 3. Typical Transfer Characteristics

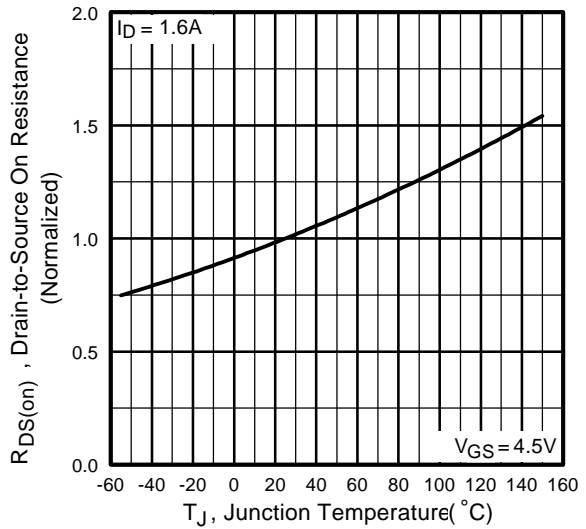


Fig 4. Normalized On-Resistance Vs. Temperature

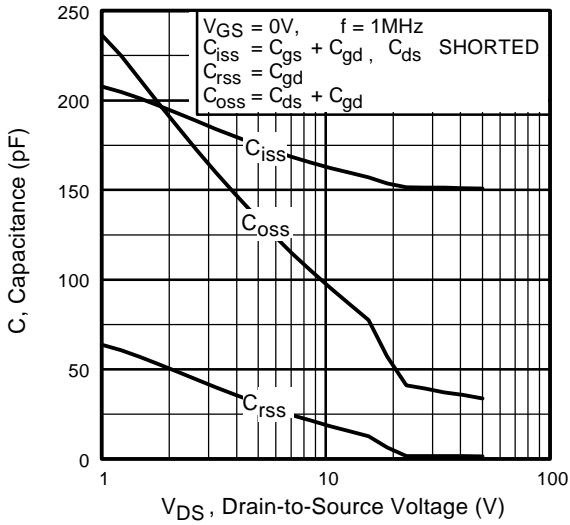


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

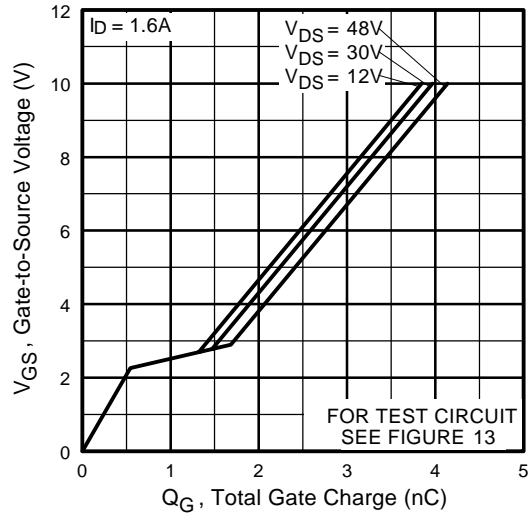


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

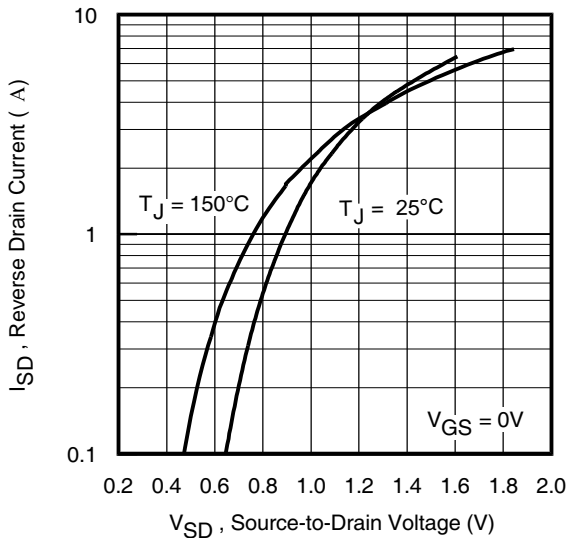


Fig 7. Typical Source-Drain Diode Forward Voltage

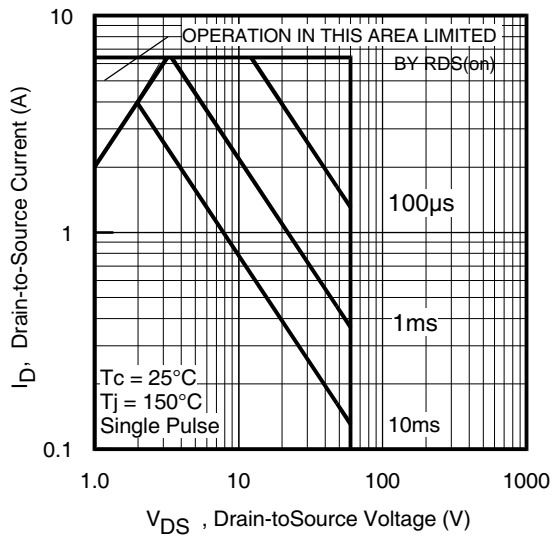


Fig 8. Maximum Safe Operating Area

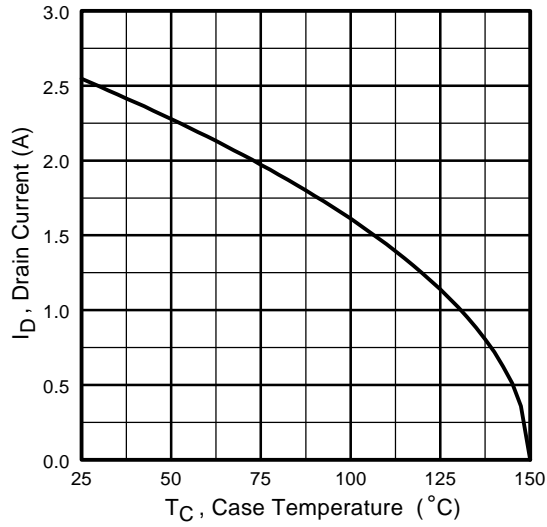


Fig 9. Maximum Drain Current Vs. Case Temperature

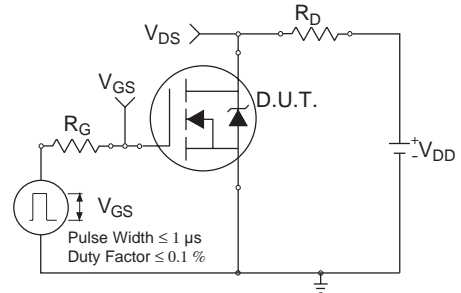


Fig 10a. Switching Time Test Circuit

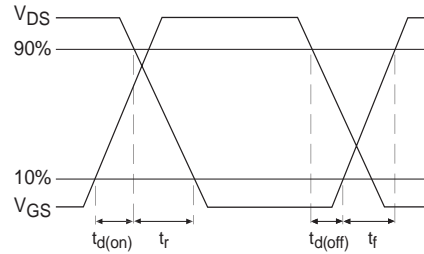


Fig 10b. Switching Time Waveforms

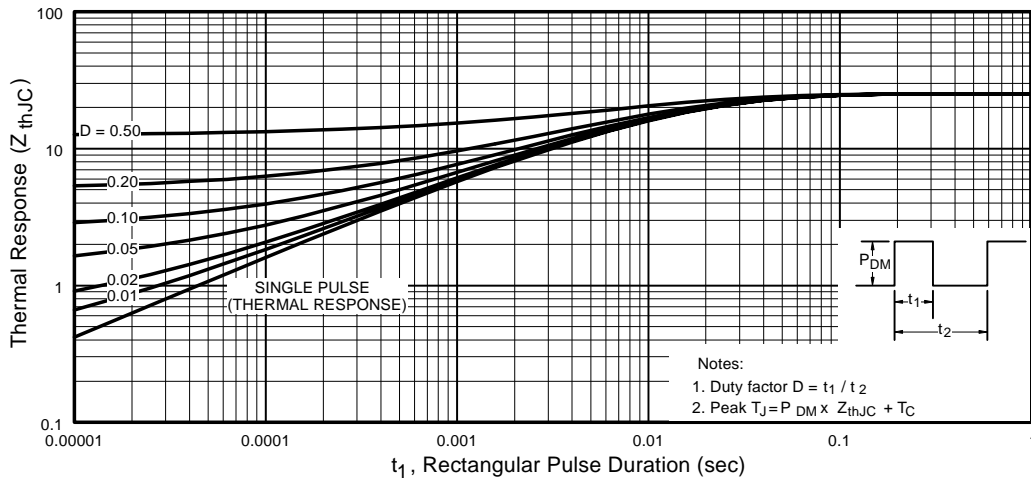


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

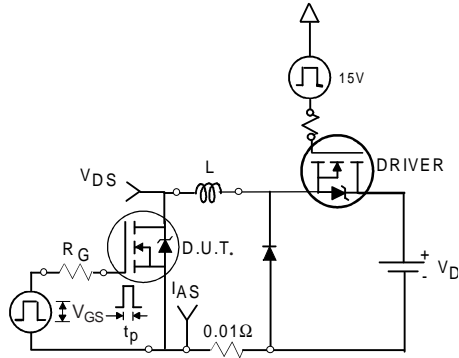


Fig 12a. Unclamped Inductive Test Circuit

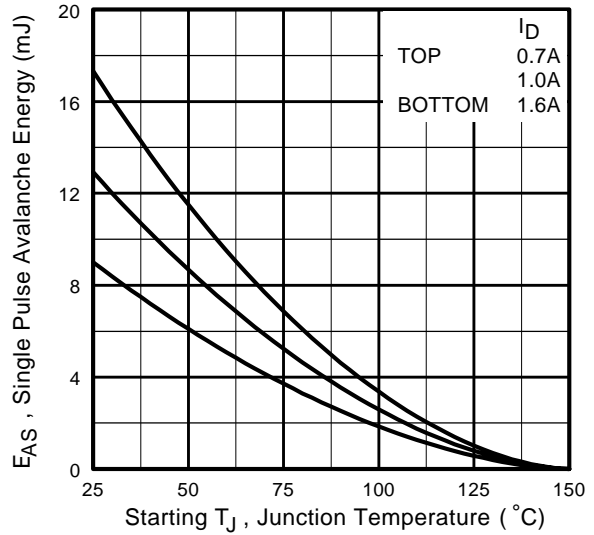


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

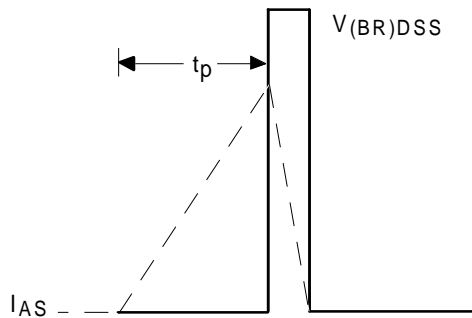


Fig 12b. Unclamped Inductive Waveforms

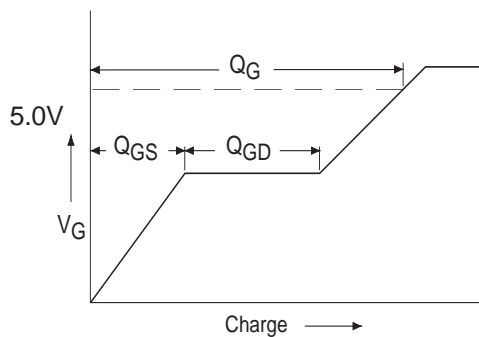


Fig 13a. Basic Gate Charge Waveform

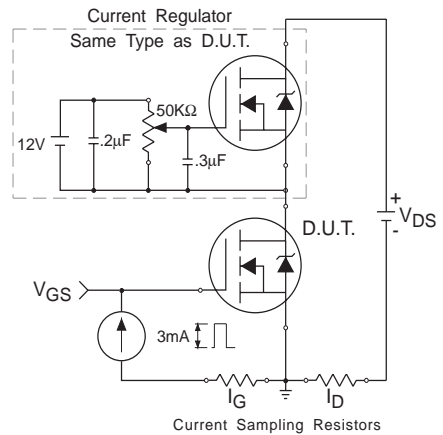


Fig 13b. Gate Charge Test Circuit

