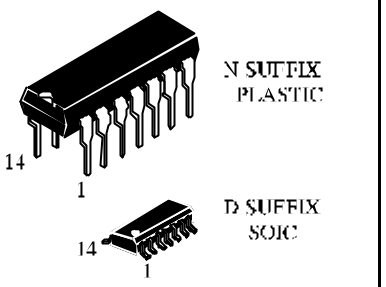
IN74HCT21A

Dual 4-Input AND Gate



ORDERING INFORMATION

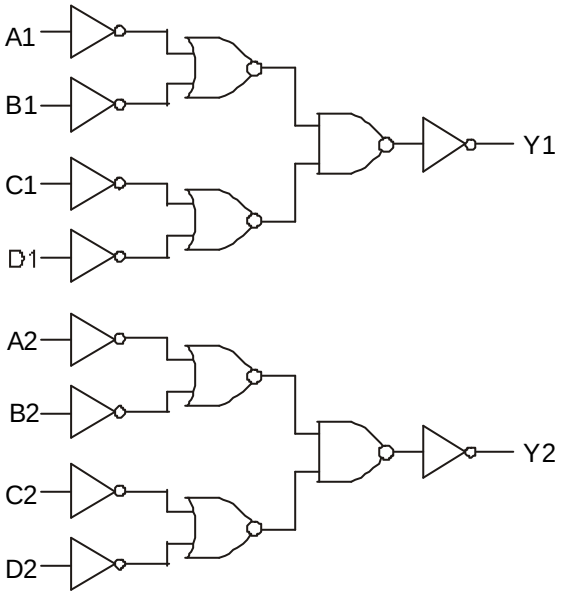
IN74HCT21AN	Plastic
IN74HCT21AD	SOIC
IZ74HCT21A	Chip

T_A = -55° to 125° C for all packages

The IN74HCT21A is high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL) . The device provide the Dual 4-input AND function.

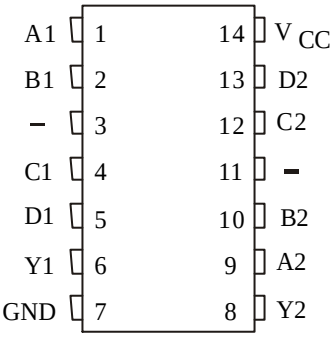
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices

LOGIC DIAGRAM



PIN 14 =V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Output
A	B	Ñ	D	Y
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

X = don’t care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
**Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		4.5	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =2.0 V V_{CC} =4.5 V V_{CC} =6.0 V	0 0 0	1000 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage		4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low -Level Input Voltage		4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|$ = - 50 ? A	4.5 5.5	4.42 5.42	4.4 5.4	4.4 5.4	V
		$V_{IN}= V_{IH}$ or V_{IL} $\|I_{OUT}\|$ = - 4.0 mA	4.5	3.98	3.84	3.70	
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN}= V_{IH}$ or V_{IL} $\|I_{OUT}\|$ = 50 ? A	4.5 5.5	0.09 0.09	0.1 0.1	0.1 0.1	V
		$V_{IN}= V_{IH}$ or V_{IL} $\|I_{OUT}\|$ = 4.0 mA	4.5	0.26	0.33	0.4	
I_{IL}	Maximum Low-Level Input Leakage Current	V_{IN}= 0 V	5.5	-0.1	-1.0	-1.0	µA
I_{IH}	Maximum High-Level Input Leakage Current	$V_{IN}= V_{CC}$	5.5	0.1	1.0	1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{IN}=V_{CC}$ or 0 V I_{OUT}=0 ? A	5.5	4.0	40	160	µA
I_{CCT}	Maximum Additional Quiescent Supply Current on input pin	V_{IN}=3.4 V any one input, V_{IN}= 0 V or V_{CC} others inputs	5.5	≤-55°C	25°C ? -125°C		mÀ
				2.9	2.4		

AC ELECTRICAL CHARACTERISTICS (C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t_{PHL}, t_{PLH}	Maximum Propagation Delay (Figure 1)	4.5	27	34	41	ns
t_{THL}, t_{TLH}	Maximum Output Transition Time (Figure 1)	4.5	15	19	22	ns
C_{IN}	Maximum Input Capacitance	5.0	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	T_A=25°C,V_{CC}=5.0 V 50	pF

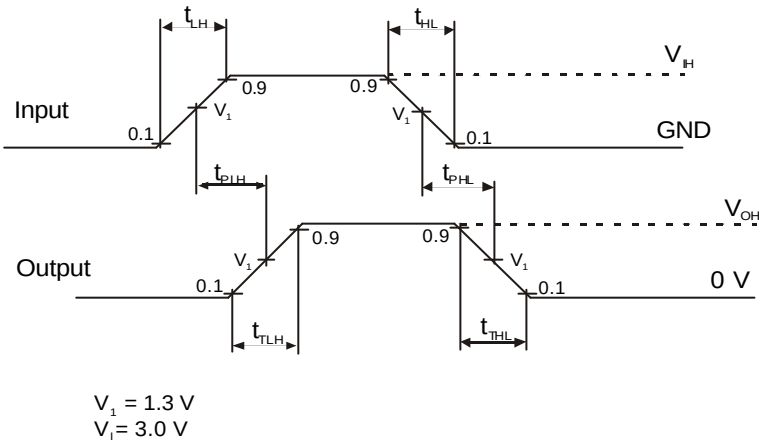


Figure 1. Switching Waveforms

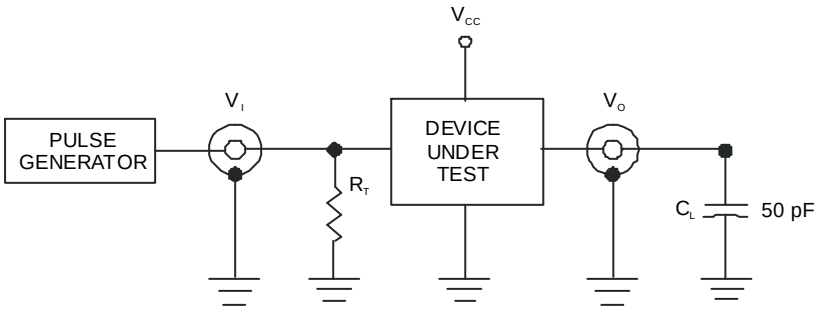
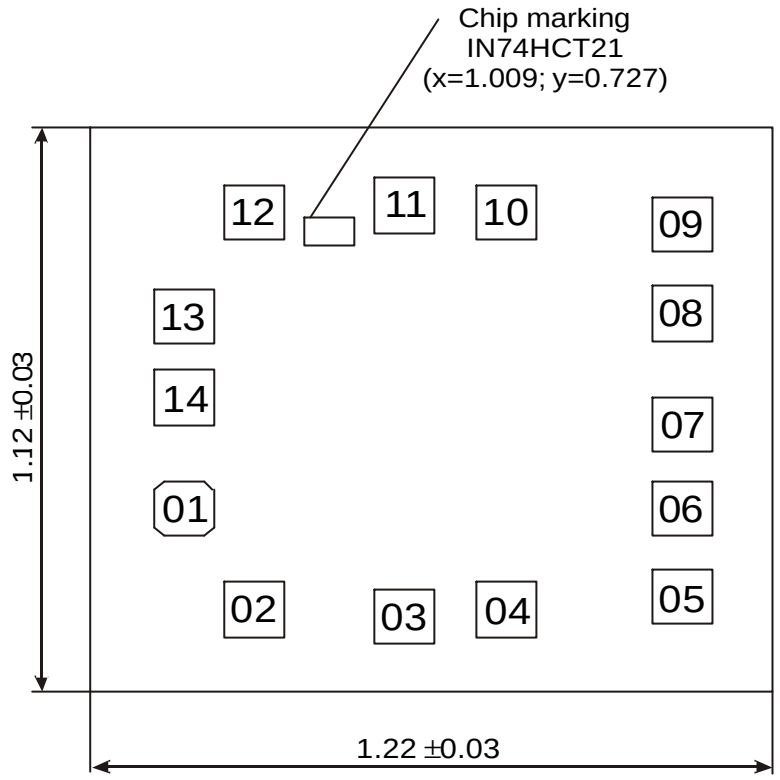


Figure 2. Test Circuit

CHIP PAD DIAGRAM IZ74HCT21A



Pad size 0.108 x 0.108 mm (Pad size is given as per passivation layer)
Thickness of chip 0.46 ± 0,02 mm

PAD LOCATION

Pad No	Symbol	X	Y
01	À1	1.1165	0.3160
02	B1	0.2405	0.1150
03	-	0.5105	0.1020
04	C1	0.6925	0.1150
05	D1	1.0065	0.1400
06	Y1	1.0065	0.3160
07	GND	1.0065	0.4840
08	Y2	1.0065	0.7040
09	A2	1.0065	0.8800
10	B2	0.6925	0.9050
11	-	0.5105	0.9180
12	C2	0.2405	0.9050
13	D2	0.1165	0.6960
14	Vcc	0.1165	0.5360