

# OKI Semiconductor

**FEDL63611A-01**

Issue Date: Jan. 28, 2004

## ML63611A

**4-Bit Microcontroller that Operates under Ultra-Low Supply Current, with RC Oscillation Type  
A/D Converter Built-In**

### GENERAL DESCRIPTION

The ML63611A is a CMOS 4-bit microcontroller using Oki's original CPU core nX-4/250.

The ML63611A is provided with the mask options of eight items of selection including (1.5 V or 3.0 V) power supply specifications and (With or Without) the regulator circuit for the LCD bias reference voltage. When a 3.0 V power supply specification is selected, the halver circuit can be used to decrease power consumption. The halver circuit cannot be used when a 1.5 V power supply specification is selected.

When "With the regulator circuit for the LCD bias reference voltage" is selected, the LCD bias reference voltage will be generated based on the output voltage of the regulator circuit. When "Without the regulator circuit for the LCD bias reference voltage" is selected, the LCD bias reference voltage will be generated based on the power supply voltage; for this reason, the LCD bias voltage decreases as the power supply voltage decreases, causing the display density of the LCD panel to thin down.

The ML63611A has incorporated in it an 8K-word program memory, a 1K-nibble data memory, four input ports, four output ports (only when the mask option of LCD driver pins is selected), 16 I/O ports, a melody circuit, a serial port, four 8-bit timers, and a 64-segment LCD driver (60 segment lines and 4 common lines, max.). (A part of the SEG pins can also be selected as output port pins or COM pins depending on the mask option.)

**Note:**

In this datasheet, for convenience of description, the symbols OPTION A, OPTION B, OPTION C, and OPTION D are used in accordance with the mask option selection of a power supply specification (1.5 V or 3.0 V) and the regulator circuit for the LCD bias reference voltage (With or Without), as shown below.

- OPTION A: 1.5 V power supply specification (halver circuit disabled), without the regulator circuit for the LCD bias reference voltage
- OPTION B: 1.5 V power supply specification (halver circuit disabled), with the regulator circuit for the LCD bias reference voltage
- OPTION C: 3.0 V power supply specification (halver circuit enabled), without the regulator circuit for the LCD bias reference voltage
- OPTION D: 3.0 V power supply specification (halver circuit enabled), with the regulator circuit for the LCD bias reference voltage

### FEATURES

The ML63611A has the following features.

a. Extensive instruction set

- 407 instructions  
Transfer, rotate, increment/decrement, arithmetic operations, compare, logic operations, mask operations, bit operations, ROM table reference, stack operations, flag operations, jump, conditional branch, call/return, control

b. Wide variety of addressing modes

- Indirect addressing mode for 4 types of data memory with current bank register, extra bank register, HL register and XY register
- Data memory bank internal direct addressing mode

## c. Processing speed

- 2 clocks per machine cycle, with most instructions executed in 1 machine cycle
- Minimum instruction execution time: 61  $\mu$ s (@ 32.768 kHz system clock)  
10  $\mu$ s (@ 200 kHz system clock)  
2.86  $\mu$ s (@ 700 kHz system clock)

## d. Clock generator circuit

- Low-speed clock:  
Crystal oscillation (32.768 kHz)
- High-speed clock:  
OPTION A, OPTION B: RC oscillation (200 kHz max.)  
OPTION C, OPTION D: Ceramic oscillation or RC oscillation selected with software (700 kHz max.)

## e. Program memory space

- 8K words
- The basic instruction length is 16 bits per word.

## f. Data memory space

- 1024 nibbles

## g. Stack level

- Call stack level: 16
- Register stack level: 16

## h. Ports

Input port (Port 0.0 to Port 0.3):

Selectable as input with pull-up resistor/high-impedance input

Provided with the reset function that resets the system when there is a simultaneous key depression of multiple bits (2, 3, or 4 bits).

Output port: Selectable as N-channel open drain output/CMOS output

Enabled only when the SEG pins (L32 to L35) are selected as the output port by the mask option.

Input-output port (Port A.0 to Port A.3, Port B.0 to Port B.3, Port C.0 to Port C.3, Port E.0 to Port E.3):

Selectable as input with pull-up resistor/input with pull-down resistor/high-impedance input

Selectable as P-channel open drain output/N-channel open drain output/CMOS output/high-impedance output

Number of ports:

	Input ports	Output ports	Input-output ports
Chip products	1 port $\times$ 4 bits	1 port $\times$ 4 bits (mask option)	4 ports $\times$ 4 bits

## i. Melody output

- Melody frequency: 529 Hz to 2979 Hz (@ 32.768 kHz)
- Tone length: 63 varieties
- Tempo: 15 varieties
- Melody data: Stored in program memory
- Buzzer driver signal output: 4 kHz (@ 32.768 kHz)

## j. LCD driver

Segment-type LCD drivers built-in

The following pin modes can be specified for L0 to L63 by the mask option generator setting. (Refer to the “MOGTOOL Mask Option Generator User’s Manual”.)

“●” in the table below indicates that that particular function can be selected.

	L0 to L3	L4 to L31	L32 to L35	L36 to L39	L40 to L63
SEG Pins	●	●	●	●	●
COM Pins	●*1	—	—	●*1	—
Output Port Pins	—	—	●*2	—	—

\*1 Can be selected as a COM pin in 1-bit unit (L0 to L3, L36 to L39). A maximum of four pins can be selected as COM pins.

\*2 Can be selected as an output port in 4-bit unit (L32 to L35).  
N-channel open drain output or CMOS output can be specified for each bit.

Number of segments : 64 (60 SEG. × 4 COM. Max.)

Duty : 1/1 to 1/4 duty (fixed to 1/2 duty when at 1/2 bias)

Bias : Selectable as 1/2 or 1/3 bias (Selectable by the mask option. Refer to the “MOGTOOL Mask Option Generator User’s Manual”.)

OPTION B, OPTION D: Regulator circuit used (0.95/1.90/2.85 V)

OPTION A, OPTION C: Regulator circuit not used (directly connected to the power supply voltage (1.5/3.0/4.5 V))

Frame frequency : 64 Hz (at 1/1, 1/2, 1/4 duty), 85.3 Hz (at 1/3 duty)

Contrast : OPTION B, OPTION D: Adjustable up to 16 levels (in steps of 0.03 V)

OPTION A, OPTION C: Adjustment not available

Display modes : Selectable as all-ON mode/all-OFF mode/power down mode/normal display mode

## k. RC oscillation type A/D converter

- 2 channels (time sharing is used)

## l. System reset function

- System reset by RESET pin (2 kHz sampling function provided)
- System reset that resets the system when the combined bits (2, 3, or 4 bits) of the input port (Port 0) are all set to a “H” level

(Whether system reset is disabled or enabled, the number of bits to be combined, and the polarity can be specified by mask option. Refer to the “MOGTOOL Mask Option Generator User’s Manual”.)

2 bits : P0.0, P0.1

3 bits : P0.0, P0.1, P0.2

4 bits : P0.0, P0.1, P0.2, P0.3

## m. Battery check

- Applies to the OPTION C and OPTION D. Does not apply to the OPTION A and OPTION B.
- Function that detects battery low voltage
- Selection of judgment voltage by software (LD1 and LD0 bit settings of BLDCON)
- Judgment voltage : 1.80 ±0.10 V, 2.00 ±0.10 V, 2.40 ±0.10 V, 2.60 ±0.10 V (Ta = 25°C)

## n. Timers, counters

- 8-bit timer: 4 channels  
Selectable as auto-reload mode, capture mode, clock frequency measurement mode
- Watchdog timer: 1 channel
- 100 Hz timer: 1 channel  
1/100 sec. measurement possible
- 15-bit TBC: 1 channel  
1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz, 128 Hz signals can be read

## o. Serial port

- Mode: UART mode, synchronous mode
- Communication speed in UART mode: 1200 bps, 2400 bps, 4800 bps, 9600 bps
- Clock frequency in synchronous mode: 32.768 kHz (internal clock mode); external clock frequency
- Data length: 5 to 8 bits

## p. Interrupt factors

- External interrupt (4 sources) : Selectable as rising edge/falling edge/both rising and falling edges
- Internal interrupt (14 sources) : Watchdog timer interrupt × 1  
Melody end interrupt × 1  
ADC interrupt × 1  
Timer interrupt × 4  
Serial port reception interrupt × 1  
Serial port transmission interrupt × 1  
1/100 timer (10 Hz) interrupt × 1  
Time base interrupt × 4 (2, 4, 16, and 32 Hz)

## q. Operating temperature

- -20 to +70°C

## r. Power supply voltage

OPTION A, OPTION B (1.5 V versions): 1.3 to 1.7 V

Note: The operation will only be at the battery voltage and no voltage halver circuit can be used.

OPTION C, OPTION D (3.0 V versions): 1.8 to 3.6 V

Note: It is possible to select by software to use the output of the halver circuit as the power supply of the voltage regulator circuit when the battery voltage is in the range 2.4 to 3.6 V, and to use the battery voltage itself as the power supply of the voltage regulator circuit when the battery voltage is in the range 1.8 to 2.4 V.

It is possible to detect whether the battery voltage is 2.4 V or 1.8 V using the BLD function.

- When the halver circuit is ON: 2.4 to 3.6 V
- When the halver circuit is OFF: 1.8 to 2.4 V

## s. Supply current

- In the HALT mode, with the LCD display OFF, low-speed operation,  $-20$  to  $+70^{\circ}\text{C}$ :
  - OPTION A (1.5 V power supply specification, without the regulator circuit for the LCD bias reference voltage): Typ.  $1.4\ \mu\text{A}$  / Max.  $2.8\ \mu\text{A}$
  - OPTION B (1.5 V power supply specification, with the regulator circuit for the LCD bias reference voltage): Typ.  $1.6\ \mu\text{A}$  / Max.  $3.0\ \mu\text{A}$
  - OPTION C (3.0 V power supply specification, without the regulator circuit for the LCD bias reference voltage): Typ.  $0.53\ \mu\text{A}$  / Max.  $1.2\ \mu\text{A}$
  - OPTION D (3.0 V power supply specification, with the regulator circuit for the LCD bias reference voltage): Typ.  $0.70\ \mu\text{A}$  / Max.  $1.4\ \mu\text{A}$

## t. Packages available

Package	Product name
Chip (116-pad)	ML63611A-xxxWA (Here, 'xxx' denotes the code number.)

## MASK OPTIONS

There are nine items in the mask option of the ML63611A.

Make the settings for the following items using the MOGTOOL mask option generator. Refer to the “MOGTOOL Mask Option Generator User’s Manual” for details of the method of making the settings.

- 1) Selection of power supply voltage  
Select a power supply specification for the power supply voltage to be used as either a 1.5 V power supply specification (1.3 to 1.7 V) or a 3.0 V power supply specification (1.8 to 3.6 V).



Note:

When a 1.5 V power supply specification (OPTION A and OPTION B) is selected, the halver circuit and the battery low detect circuit cannot be used.

- 2) Selection of the regulator circuit for the LCD bias reference voltage  
Select the LCD bias reference voltage as either the output of the regulator circuit or the power supply voltage.



Note:

When power is supplied from the battery:

When “Without the regulator circuit for the LCD bias reference voltage” is selected with the mask option, the LCD bias reference voltage will be generated based on the power supply voltage. When a 1.5 V power supply specification is selected,  $V_{DD1}$  will be the pin for the LCD bias reference voltage, and when a 3.0 V power supply specification is selected,  $V_{DD2}$  will be the pin for the LCD bias reference voltage. In addition, the LCD bias voltage will decrease as the power supply voltage decreases, causing the display density of the LCD panel to thin down.

When “With the regulator circuit for the LCD bias reference voltage” is selected, the display density will be kept constant even if the battery voltage decreases.

- 3) Selection of the initial state of Port 0  
Select the initial state of Port 0 as either “input with pull-down resistor” or “input with pull-up resistor”. This selection determines the initial value of POPUD (POCON1).



Note:

This selection applies to all four bits and it is not possible to make this selection separately for each bit.

- 4) Selection of simultaneous key depression reset function of Port 0  
Select the simultaneous key depression reset function and the number of bits (pins) that can be pressed simultaneously.  
The pins that are set according to the number of bits pressed simultaneously are fixed as follows:  
2 bits: P0.0, P0.1; 3 bits: P0.0, P0.1, P0.2; 4 bits: P0.0, P0.1, P0.2, P0.3.



Note:

The system reset mode will be entered at the second falling edge of the 1 Hz signal.

- 5) Selection of MDB pin output voltage level  
Select whether to make the output voltage level of the melody output pin (MDB: negative logic) either  $V_{DD}$  or  $V_{SS}$  when the melody is OFF.

- 6) SEG/COM/PORT/DATA selection of the LCD driver pins  
It is possible to make the pins L0 to L3 and L36 to L39 either SEG pins or COM pins. However, it is a maximum of four pins that can be selected as COM pins.  
It is possible to make the pins L32 to L35 either SEG pins or output port pins.  
The pins L4 to L31 and L40 to L63 are always SEG pins.  
The segment register corresponding to the pins L0 to L63 can also be used as a DATA area.



Notes:

- When the selection is made as output port pins, the selection applies to all four bits.
  - When the segment register is selected as the DATA area, the corresponding pins will still be outputting the segment waveforms, and hence should be left open.
- 7) Selection of the register address and data of the LCD driver pins  
The allocation of the register address and data is set for each LCD driver pin.



Note:

It is not possible to make multiple settings for the same address and the same bit.

- 8) Selection of whether or not to detect stoppage of low-speed clock oscillations  
Select whether or not to detect stoppage of the low-speed clock oscillations and to transfer to the system reset mode.
- 9) Selection of the LCD bias  
1/3 or 1/2 bias is selected for the LCD bias.



Note:

The setting of the mask option should match the setting of bit 3 of display control register 0. Otherwise, normal waveforms are not output.

**BLOCK DIAGRAM**

Figures 1 through 4 show the block diagram of OPTION A to D  
 Asterisks (\*) indicate the port secondary functions.

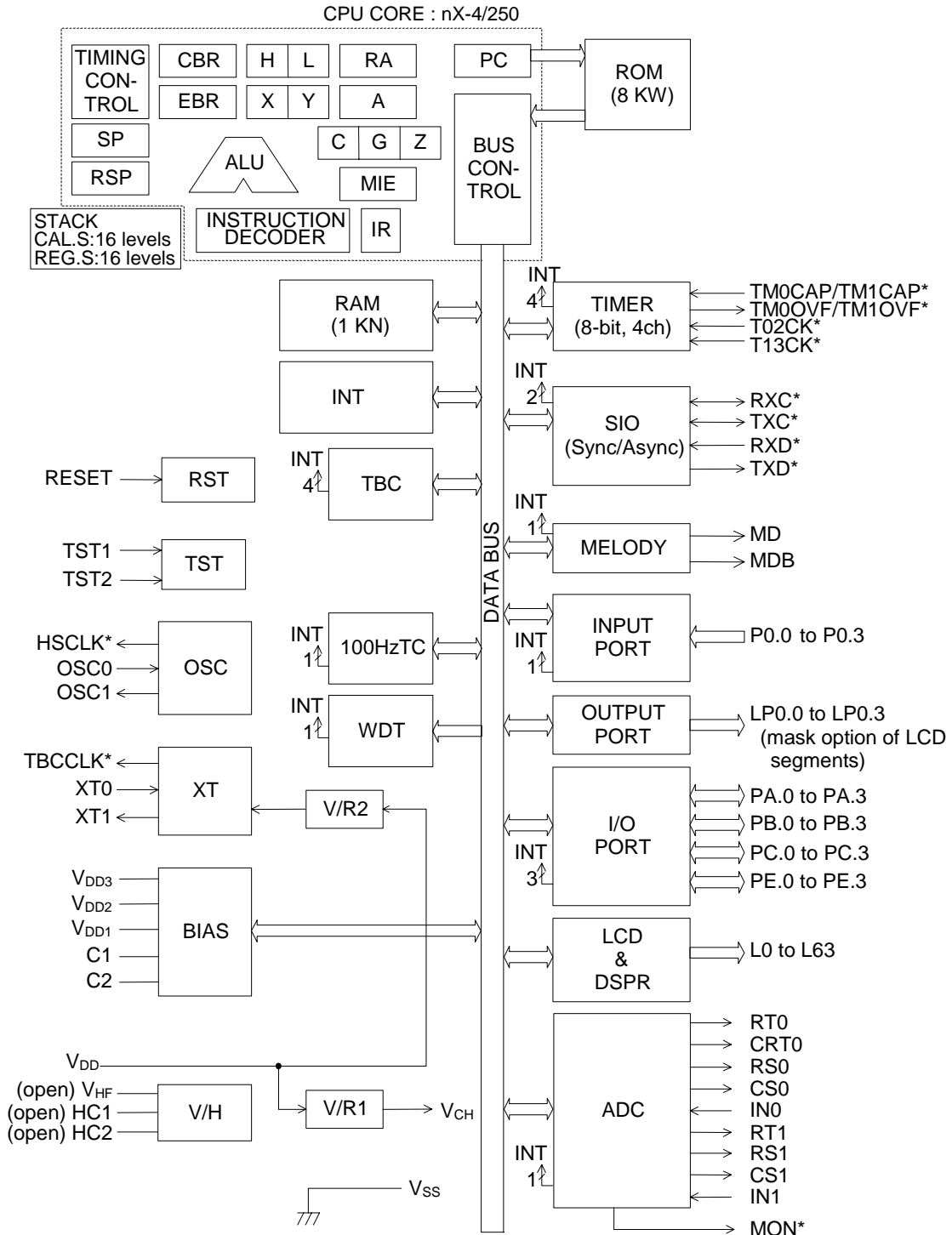


Figure 1 OPTION A Block Diagram



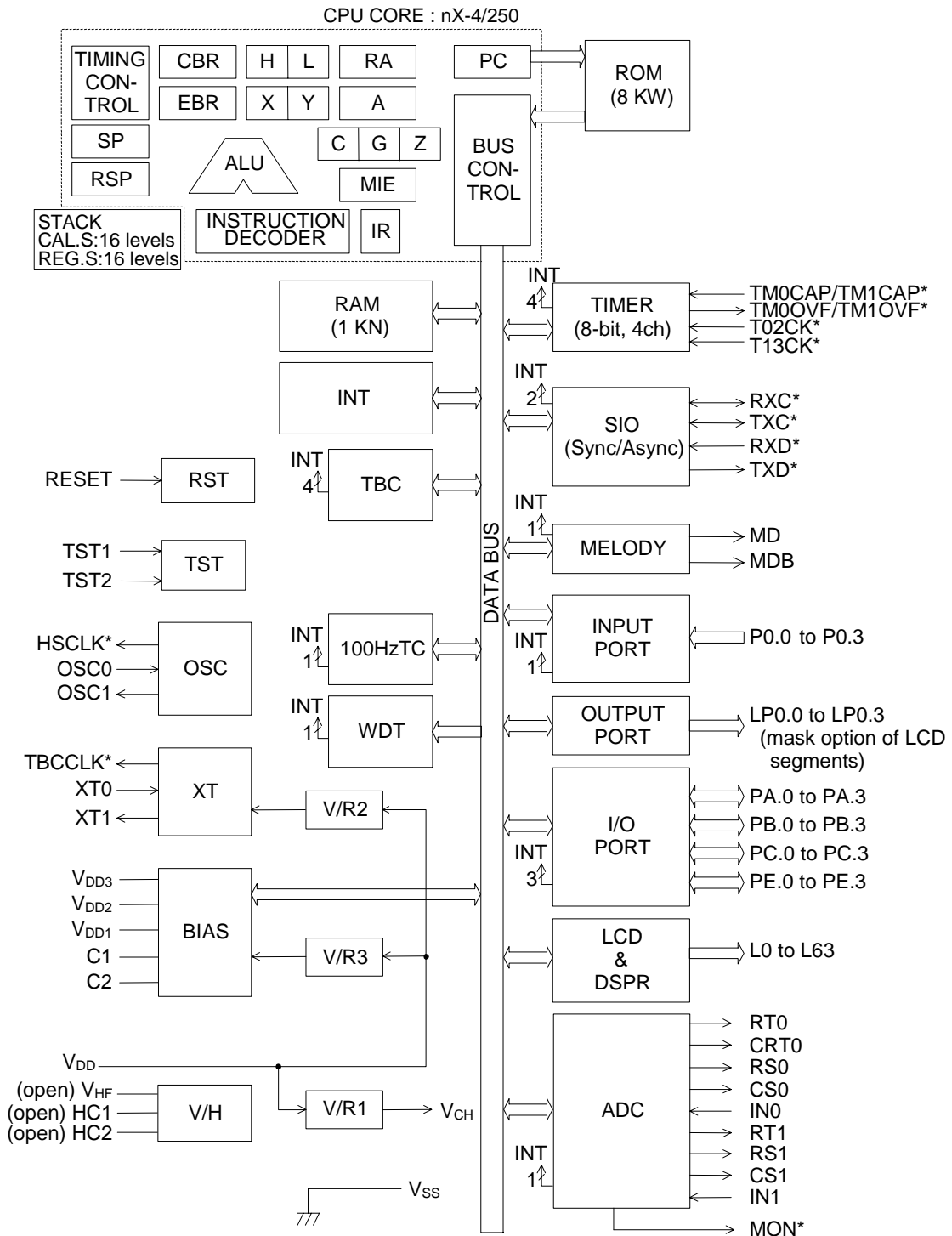


Figure 2 Option B Block Diagram

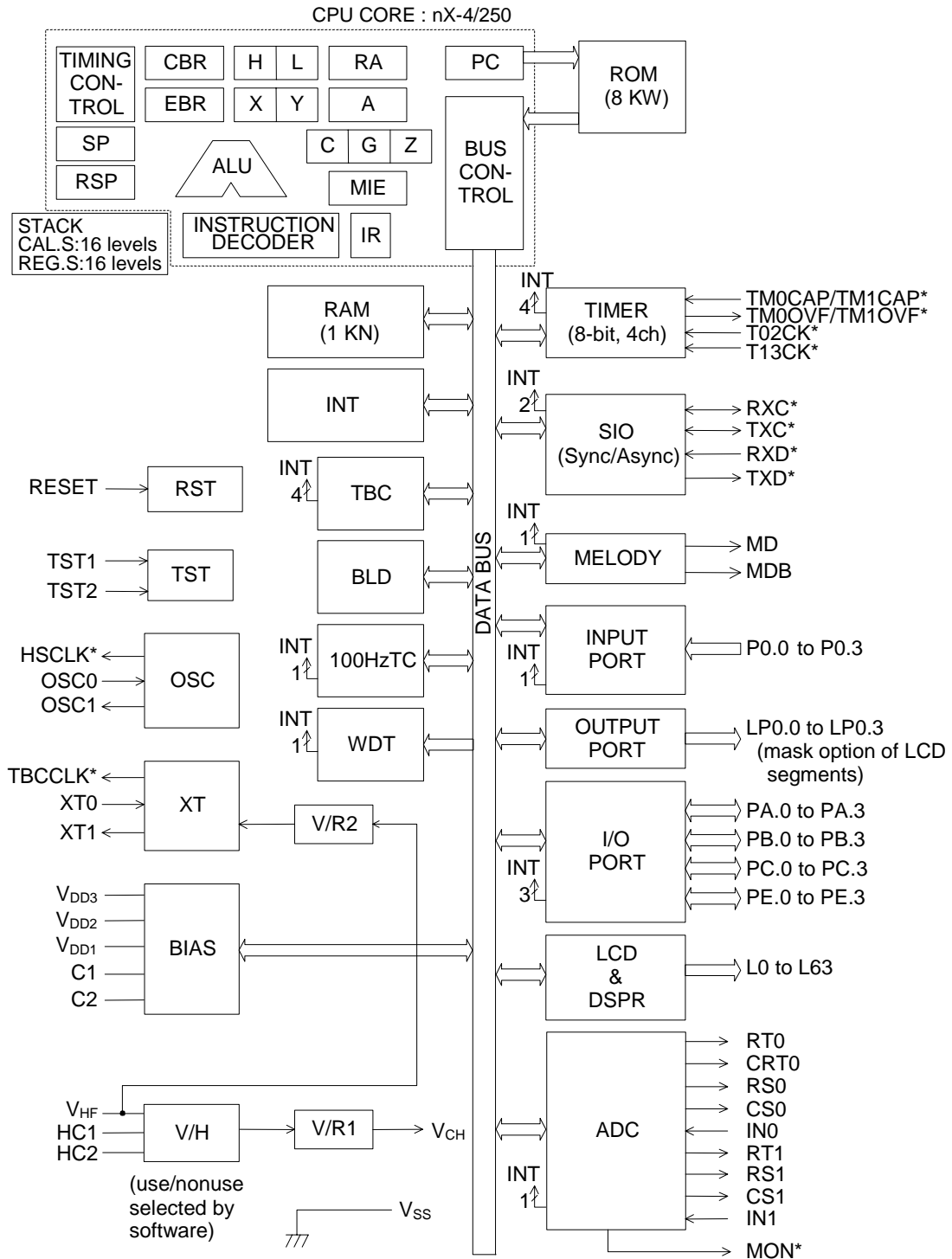


Figure 3 Option C Block Diagram

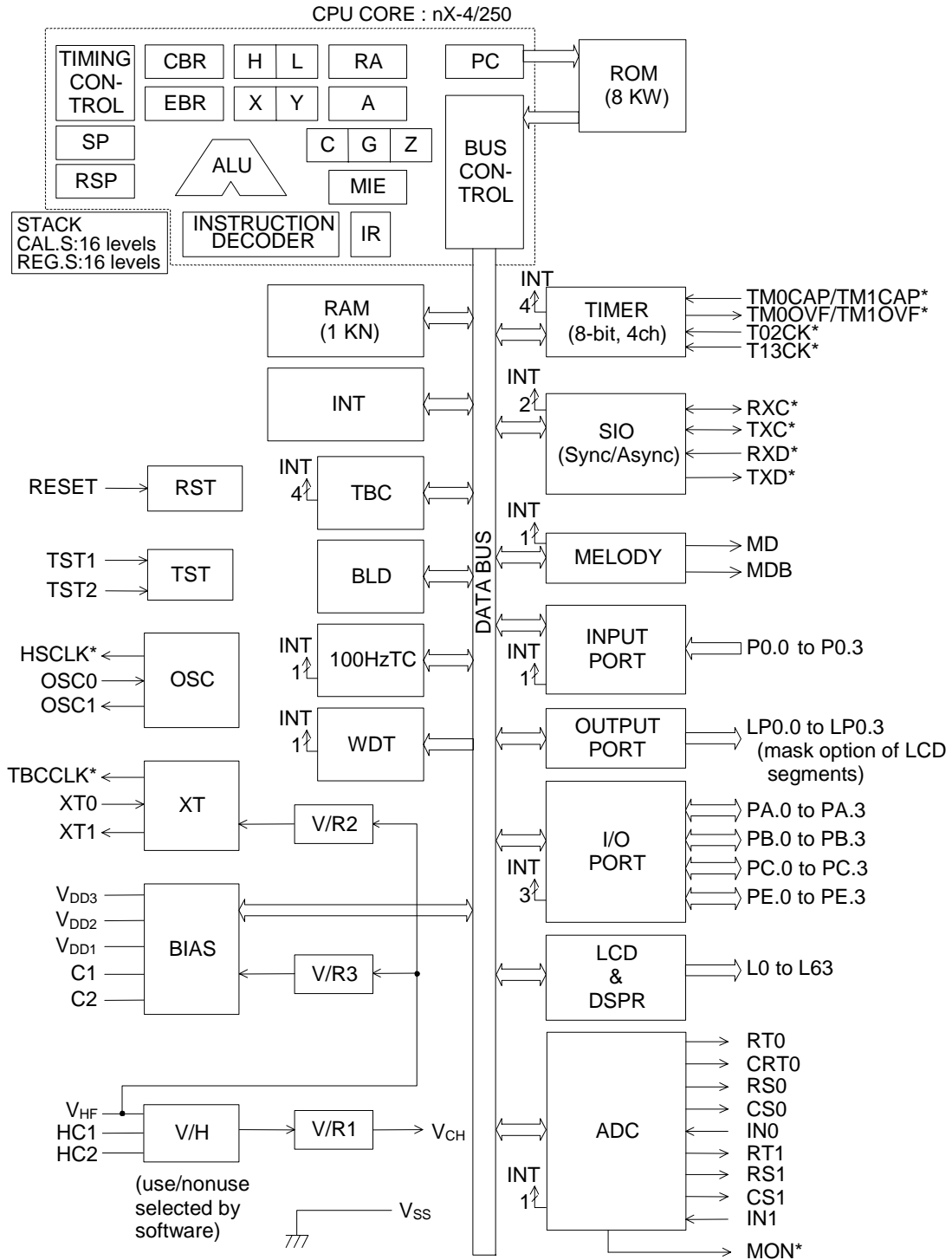
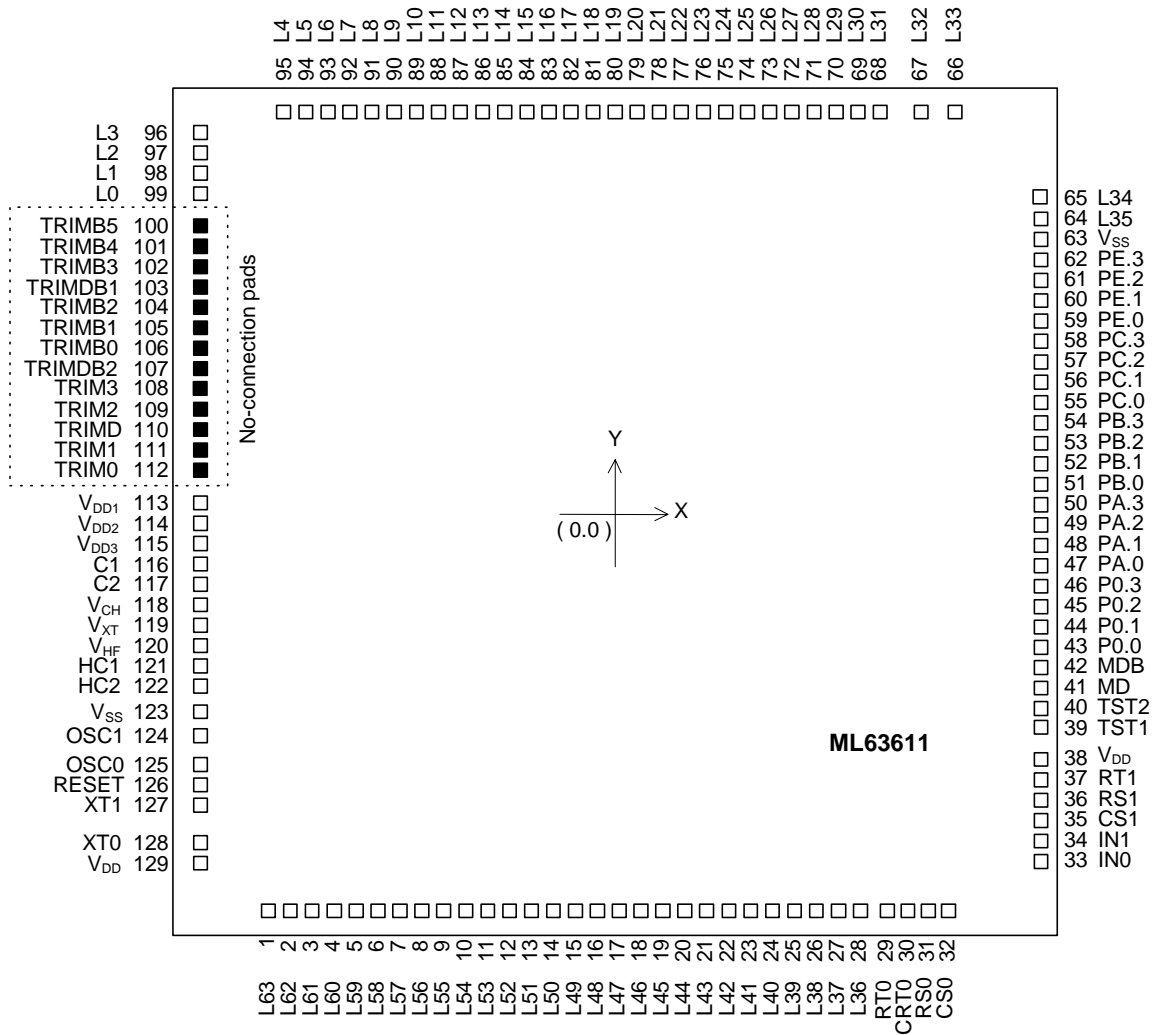


Figure 4 Option D Block Diagram

**PAD CONFIGURATION**

The ML63611A chip pin configuration and the pad coordinates are shown in Figure 5 and Table 1, respectively.



- Chip Size : 5.20 mm × 5.20 mm
- Chip Thickness : 350 μm (typ.) (280 μm: available as required)
- Coordinate Origin : Chip center
- Pad Hole Size : 80 μm × 80 μm
- Pad Size : 90 μm × 90 μm
- Minimum Pad Pitch : 115 μm
- Number of bonding pads: 116 (total number of pads: 129)
- Notes: The chip substrate voltage is V<sub>SS</sub>.  
Do not bond pins 100 to 112 (marked by “■”). Leave them open.

**Figure 5 ML63611A Chip Pin Configuration (Top View)**

Table 1 ML63611A Pad Coordinates

Chip center: X = 0, Y = 0

Pad No.	Pad Name	X ( $\mu\text{m}$ )	Y ( $\mu\text{m}$ )	Pad No.	Pad Name	X ( $\mu\text{m}$ )	Y ( $\mu\text{m}$ )
1	L63	-2109	-2454	34	IN1	2474	-2119
2	L62	-1987	-2454	35	CS1	2474	-1997
3	L61	-1865	-2454	36	RS1	2474	-1876
4	L60	-1742	-2454	37	RT1	2474	-1754
5	L59	-1620	-2454	38	VDD	2474	-1517
6	L58	-1498	-2454	39	TST1	2474	-1402
7	L57	-1376	-2454	40	TST2	2474	-1287
8	L56	-1254	-2454	41	MD	2474	-1157
9	L55	-1131	-2454	42	MDB	2474	-1042
10	L54	-1009	-2454	43	P0.0	2474	-912
11	L53	-887	-2454	44	P0.1	2474	-797
12	L52	-765	-2454	45	P0.2	2474	-682
13	L51	-643	-2454	46	P0.3	2474	-566
14	L50	-520	-2454	47	PA.0	2474	-448
15	L49	-398	-2454	48	PA.1	2474	-327
16	L48	-276	-2454	49	PA.2	2474	-205
17	L47	-154	-2454	50	PA.3	2474	-84
18	L46	-32	-2454	51	PB.0	2474	38
19	L45	91	-2454	52	PB.1	2474	160
20	L44	213	-2454	53	PB.2	2474	281
21	L43	335	-2454	54	PB.3	2474	403
22	L42	457	-2454	55	PC.0	2474	524
23	L41	579	-2454	56	PC.1	2474	646
24	L40	702	-2454	57	PC.2	2474	767
25	L39	824	-2454	58	PC.3	2474	889
26	L38	946	-2454	59	PE.0	2474	1010
27	L37	1068	-2454	60	PE.1	2474	1132
28	L36	1190	-2454	61	PE.2	2474	1254
29	RT0	1442	-2474	62	PE.3	2474	1375
30	CRT0	1563	-2474	63	Vss	2474	1493
31	RS0	1685	-2474	64	L35	2440	1713
32	CS0	1806	-2474	65	L34	2440	1950
33	IN0	2474	-2240	66	L33	1944	2440

Table 1 ML63611A Pad Coordinates (continued)

Chip center: X = 0, Y = 0

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
67	L32	1707	2440	99	L0	-2362	1898
68	L31	1563	2440	100	TRIMB5	No-connection	
69	L30	1441	2440	101	TRIMB4		
70	L29	1319	2440	102	TRIMB3		
71	L28	1197	2440	103	TRIMDB1		
72	L27	1074	2440	104	TRIMB2		
73	L26	952	2440	105	TRIMB1		
74	L25	830	2440	106	TRIMB0		
75	L24	708	2440	107	TRIMDB2		
76	L23	586	2440	108	TRIM3		
77	L22	463	2440	109	TRIM2		
78	L21	341	2440	110	TRIMD		
79	L20	219	2440	111	TRIM1		
80	L19	97	2440	112	TRIM0		
81	L18	-25	2440	113	VDD1	-2474	179
82	L17	-148	2440	114	VDD2	-2474	58
83	L16	-270	2440	115	VDD3	-2474	-63
84	L15	-392	2440	116	C1	-2474	-184
85	L14	-514	2440	117	C2	-2474	-305
86	L13	-636	2440	118	VCH	-2474	-426
87	L12	-759	2440	119	VXT	-2474	-547
88	L11	-881	2440	120	VHF	-2474	-668
89	L10	-1003	2440	121	HC1	-2474	-788
90	L9	-1125	2440	122	HC2	-2474	-909
91	L8	-1247	2440	123	VSS	-2474	-1042
92	L7	-1370	2440	124	OSC1	-2474	-1175
93	L6	-1492	2440	125	OSC0	-2474	-1296
94	L5	-1614	2440	126	RESET	-2474	-1461
95	L4	-1736	2440	127	XT1	-2474	-1596
96	L3	-2362	2265	128	XT0	-2474	-1921
97	L2	-2362	2143	129	VDD	-2474	-2063
98	L1	-2362	2021				

## PIN DESCRIPTIONS

The basic functions of each pin of the ML63611A are described in Table 2.

A symbol with a slash (/) denotes a pin that has a secondary function.

Refer to Table 3 for secondary functions.

For type, “—” denotes a power supply pin, “I” an input pin, “O” an output pin, and “I/O” an input-output pin.

**Table 2 Pin Description (Basic Functions)**

Classification	Pin name	Pad No.	I/O	Function	
Power Supply	V <sub>DD</sub>	38, 129	—	Positive power supply	
	V <sub>SS</sub>	63, 123		Negative power supply	
	V <sub>DD1</sub>	113		Power supply pins for LCD bias voltage (internally generated): A capacitor (1.0 μF) should be connected between V <sub>DD1</sub> and V <sub>SS</sub> , between V <sub>DD2</sub> and V <sub>SS</sub> , and between V <sub>DD3</sub> and V <sub>SS</sub> . For the OPTION A, connect V <sub>DD1</sub> with V <sub>DD</sub> ; for the OPTION C, connect V <sub>DD2</sub> with V <sub>DD</sub> .	
	V <sub>DD2</sub>	114			
	V <sub>DD3</sub>	115			
	C1	116			
	C2	117			
	V <sub>HF</sub>	120			Power supply pin for the internal regulator: A capacitor (0.1 μF) should be connected between this pin and V <sub>SS</sub> . Leave this pin open for the OPTION A and OPTION B.
	V <sub>XT</sub>	119			Power supply pin for the voltage regulator circuit for low-speed oscillation: A capacitor (1.0 μF) should be connected between this pin and V <sub>SS</sub> .
	V <sub>CH</sub>	118			Power supply pin for the voltage regulator circuit for internal logic: A capacitor C <sub>1</sub> (1.0 μF) should be connected between this pin and V <sub>SS</sub> .
HC1	121	Capacitor connection pins for the halver circuit: A capacitor (0.1 μF) should be connected between HC1 and HC2. Leave these pins open for the OPTION A and OPTION B.			
HC2	122				
Oscillation	XT0	128	I	Low-speed clock oscillation pins: Connect a crystal between XT0 and XT1, and connect capacitor (C <sub>G</sub> ) between XT0 and V <sub>SS</sub> .	
	XT1	127	O		
	OSC0	125	I	High-speed clock oscillation pins: Ceramic oscillation or RC oscillation is selected by the software. In the OPTION A and OPTION B, only RC oscillation is available. If ceramic oscillation is selected, connect a ceramic resonator between OSC0 and OSC1, and connect capacitor (C <sub>L0</sub> , C <sub>L1</sub> ) between OSC0 and V <sub>SS</sub> and between OSC1 and V <sub>SS</sub> . If RC oscillation is selected, connect external oscillation resistor (R <sub>OSH</sub> ) between OSC0 and OSC1.	
	OSC1	124	O		
Test	TST1	39	I	Input pins for testing: A pull-down resistor is internally connected to these pins.	
	TST2	40			

**Table 2 Pin Description (Basic Functions) (continued)**

Classification	Pin name	Pad No.	I/O	Function
Reset	RESET	126	I	Reset input pin: 2 kHz sampling circuit is equipped. Holding this pin to “H” level for 1 ms or more puts this device into a reset state. Then, setting this pin to “L” level starts executing an instruction from address 0000H. A pull-down resistor is internally connected to this pin.
Melody	MD	41	O	Melody output pin (Positive logic)
	MDB	42		Melody output pin (Negative logic): $V_{DD}$ or $V_{SS}$ is selectable for the pin output voltage when melody output is turned off (mask option).
Port	P0.0	43	I	4-bit input port: Pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit. A system reset function is provided that resets the system when there is a simultaneous key depression of multiple bits (mask option).
	P0.1	44		
	P0.2	45		
	P0.3	46		
	PA.0	47	I/O	4-bit input-output ports: In input mode, pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit. In output mode, P-channel open drain output, N-channel open drain output, CMOS output, or high-impedance output is selectable for each bit.
	PA.1	48		
	PA.2	49		
	PA.3	50		
	PB.0	51	I/O	
	PB.1	52		
	PB.2	53		
	PB.3	54		
	PC.0	55	I/O	
	PC.1	56		
	PC.2	57		
	PC.3	58		
PE.0	59	I/O		
PE.1	60			
PE.2	61			
PE.3	62			



**Table 2 Pin Description (Basic Functions) (continued)**

Classification	Pin name	Pad No.	I/O	Function
LCD	L0	99	O	These pins can be selected as LCD segment signal output pins (L0 to L3) or common signal output pins by the mask option. The common signal can be selected from among COM1 to COM4.
	L1	98		
	L2	97		
	L3	96		
	L4	95	O	Output pins dedicated to the LCD segment signal (L4 to L31).
	L5	94		
	L6	93		
	L7	92		
	L8	91		
	L9	90		
	L10	89		
	L11	88		
	L12	87		
	L13	86		
	L14	85		
	L15	84		
	L16	83		
	L17	82		
	L18	81		
	L19	80		
	L20	79		
	L21	78		
	L22	77		
	L23	76		
	L24	75		
	L25	74		
	L26	73		
	L27	72		
	L28	71		
	L29	70		
	L30	69		
	L31	68		
	L32/ LP0.3	67	O	These pins can be selected as LCD segment signal output pins (L32 to L35) or output port pins (LP0.0 to LP0.3) by the mask option.
	L33/ LP0.2	66		
L34/ LP0.1	65			
L35/ LP0.0	64			
L36	28	O	These pins can be selected as output pins dedicated to the LCD segment signal (L36 to L39) or common signal output pins by the mask option. The common signal can be selected from among COM1 to COM4.	
L37	27			
L38	26			
L39	25			

**Table 2 Pin Description (Basic Functions) (continued)**

Classification	Pin name	Pad No.	I/O	Function
LCD	L40	24	O	Output pins dedicated to the LCD segment signal (L40 to L63).
	L41	23		
	L42	22		
	L43	21		
	L44	20		
	L45	19		
	L46	18		
	L47	17		
	L48	16		
	L49	15		
	L50	14		
	L51	13		
	L52	12		
	L53	11		
	L54	10		
	L55	9		
	L56	8		
	L57	7		
	L58	6		
L59	5			
L60	4			
L61	3			
L62	2			
L63	1			
A/D Converter	RT0	29	O	Resistance temperature sensor connection pin (for channel 0)
	CRT0	30		Resistance/capacitance temperature sensor connection pin (for channel 0)
	RS0	31		Reference resistor connection pin (for channel 0)
	CS0	32		Reference capacitor connection pin (for channel 0)
	IN0	33	I	Input pin for RC oscillator circuit (for channel 0)
	IN1	34		Input pin for RC oscillator circuit (for channel 1)
	CS1	35	O	Reference capacitor connection pin (for channel 1)
	RS1	36		Reference resistor connection pin (for channel 1)
RT1	37	Resistance temperature sensor connection pin (for channel 1)		

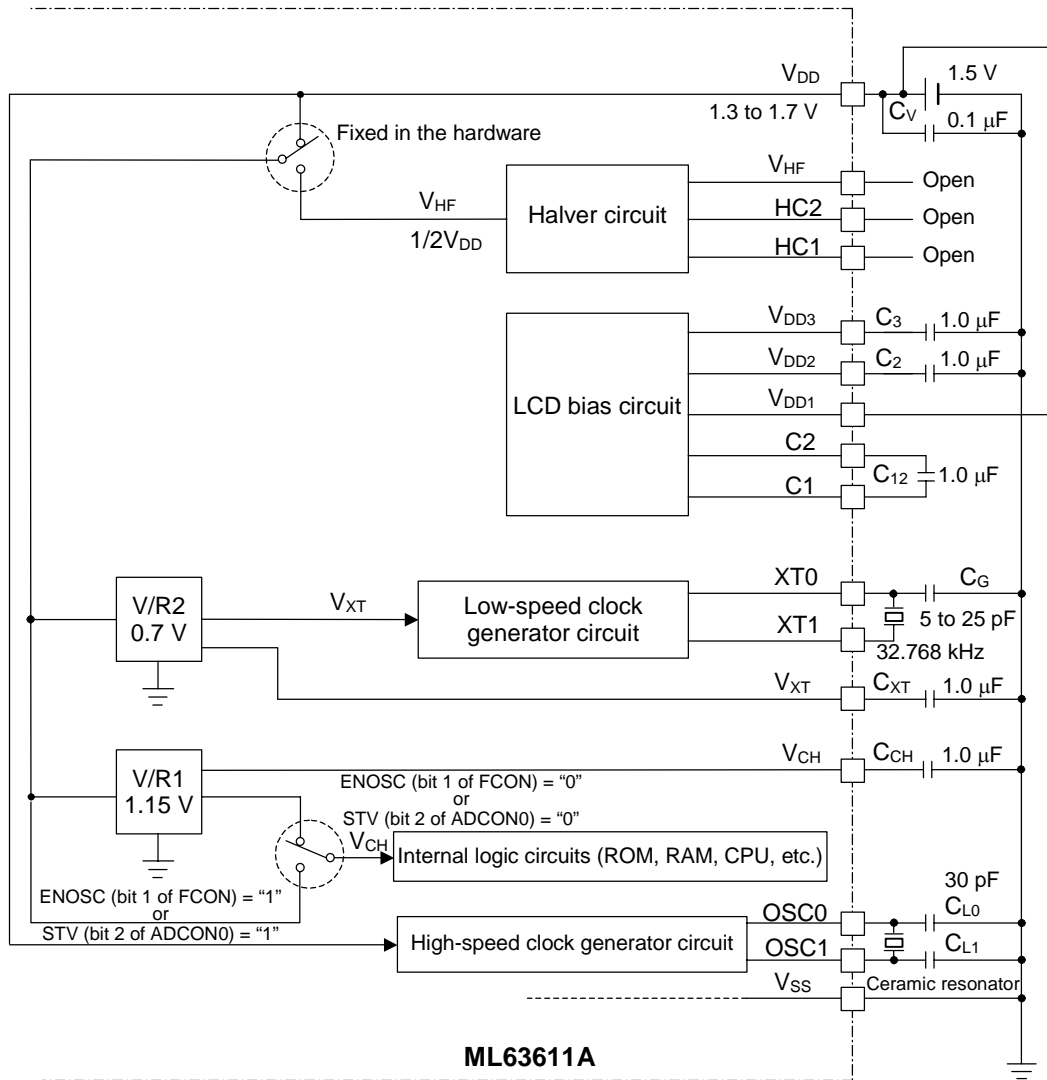
Table 3 shows the secondary functions of each pin of the ML63611A

**Table 3 Pin Description (Secondary Functions)**

Classification	Pin name	Pad No.	I/O	Function	
External Interrupt	PB.0/INT0	51	I	External 0 interrupt input pins: The change of input signal level causes an interrupt to occur. The Port B Interrupt Enable register (PBIE) enables or disables an interrupt for each bit.	
	PB.1/INT0	52			
	PB.2/INT0	53			
	PB.3/INT0	54			
	PC.0/INT1	55	I	External 1 interrupt input pins: The change of input signal level causes an interrupt to occur. The Port C Interrupt Enable register (PCIE) enables or disables an interrupt for each bit.	
	PC.1/INT1	56			
	PC.2/INT1	57			
	PC.3/INT1	58			
		PE.3/INT2	62	I	External 2 interrupt input pin: The change of input signal level causes an interrupt to occur.
		P0.0/INT5	43	I	External 5 interrupt input pins: The change of input signal level causes an interrupt to occur. The Port 0 Interrupt Enable register (POIE) enables or disables an interrupt for each bit.
		P0.1/INT5	44		
		P0.2/INT5	45		
	P0.3/INT5	46			
Capture	PB.0/TM0CAP	51	I	Timer 0 capture trigger input pin	
	PB.1/TM1CAP	52		Timer 1 capture trigger input pin	
Timer	PB.0/TM0OVF	51	O	Timer 0 (TM0) overflow flag output pin	
	PB.1/TM1OVF	52		Timer 1 (TM1) overflow flag output pin	
	PB.2/T02CK	53	I	External clock input pin for Timer 0 (TM0) and Timer 2 (TM2)	
	PB.3/T13CK	54		External clock input pin for Timer 1 (TM1) and Timer 3 (TM3)	
Serial Port	PC.0/RXD	55	I	Serial port receive data input pin	
	PC.1/TXC	56	I/O	Sync serial port clock input-output pin: Transmit sync clock input-output pin when a serial port is used synchronously. Transmit clock output when this device is used as a master processor. Transmit clock input when this device is used as a slave processor.	
				Sync serial port clock input-output pin: Receive sync clock input-output pin when a serial port is used synchronously. Receive clock output when this device is used as a master processor. Receive clock input when this device is used as a slave processor.	
	PC.2/RXC	57			
PC.3/TXD	58	O		Serial port transmit data output pin	
Monitor	PE.0/MON	59	O	Pin for monitoring the RC oscillation clock for the A/D converter	
	PE.1/TBCCLK	60	O	Low-speed oscillation clock (TBCCLK) monitoring pin	
	PE.2/HSCLK	61	O	High-speed oscillation clock (HSCLK) monitoring pin	

**POWER SUPPLY CIRCUIT CONFIGURATION**

Figures 6 through 9 show the power supply circuit configuration of OPTION A to D.



**Figure 6 OPTION A Power Supply Circuit Configuration**

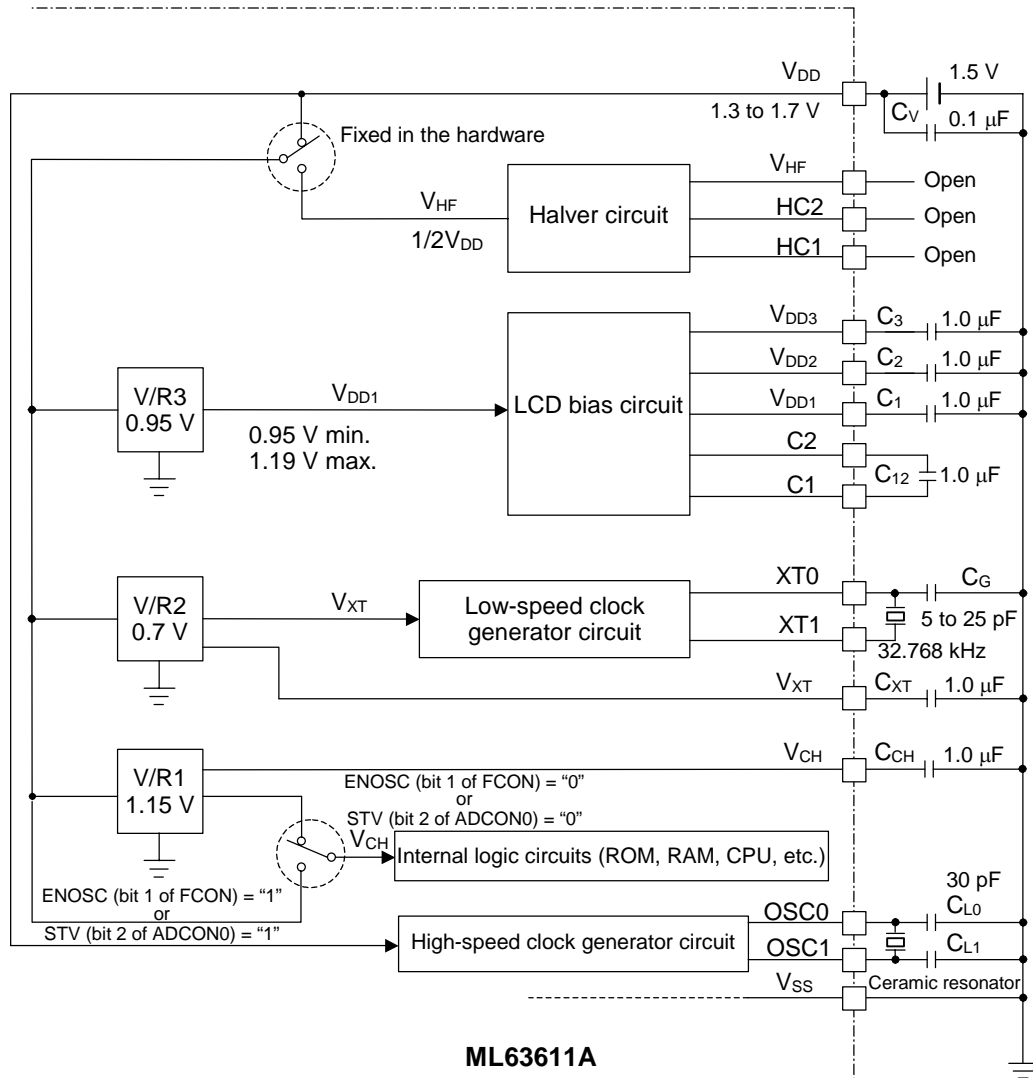


Figure 7 OPTION B Power Supply Circuit Configuration

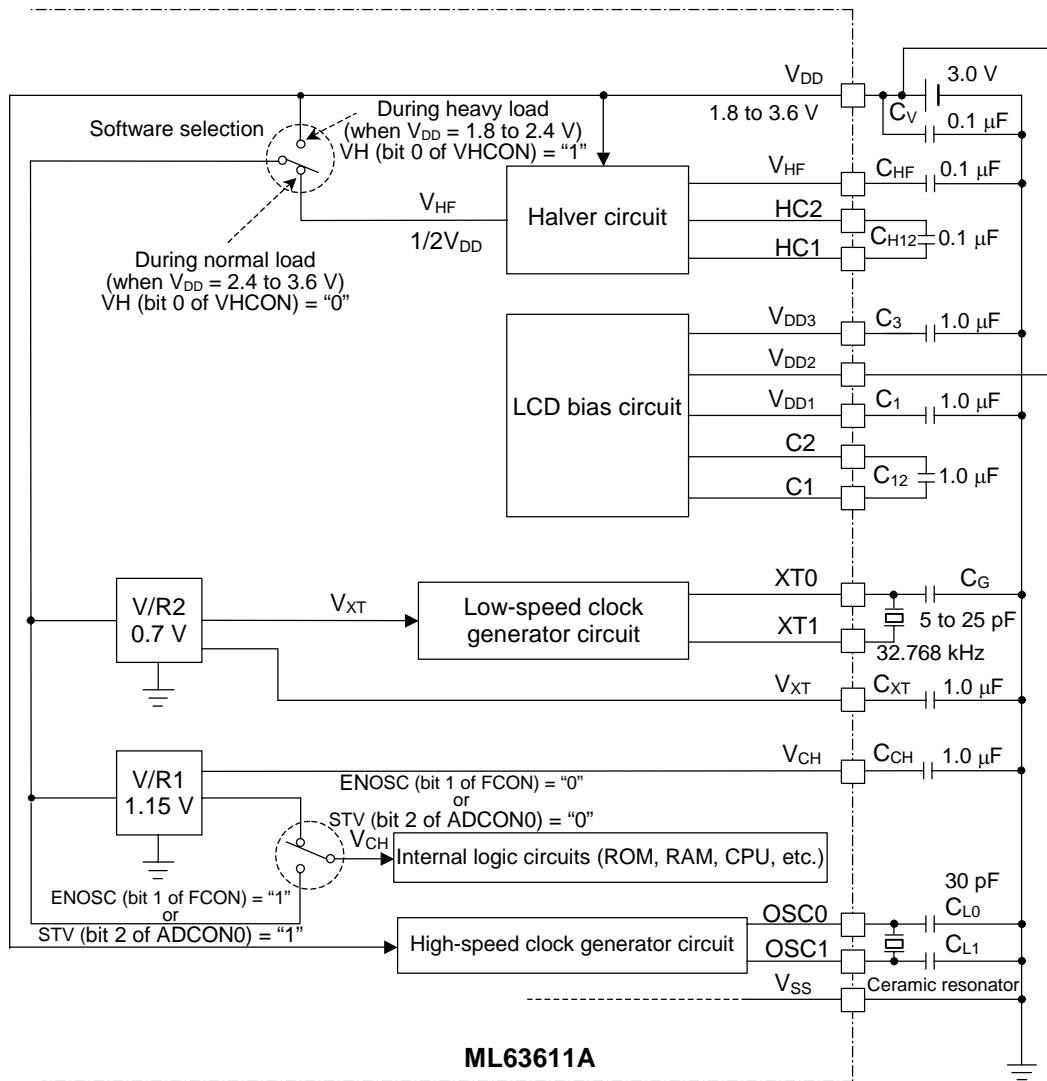


Figure 8 OPTION C Power Supply Circuit Configuration

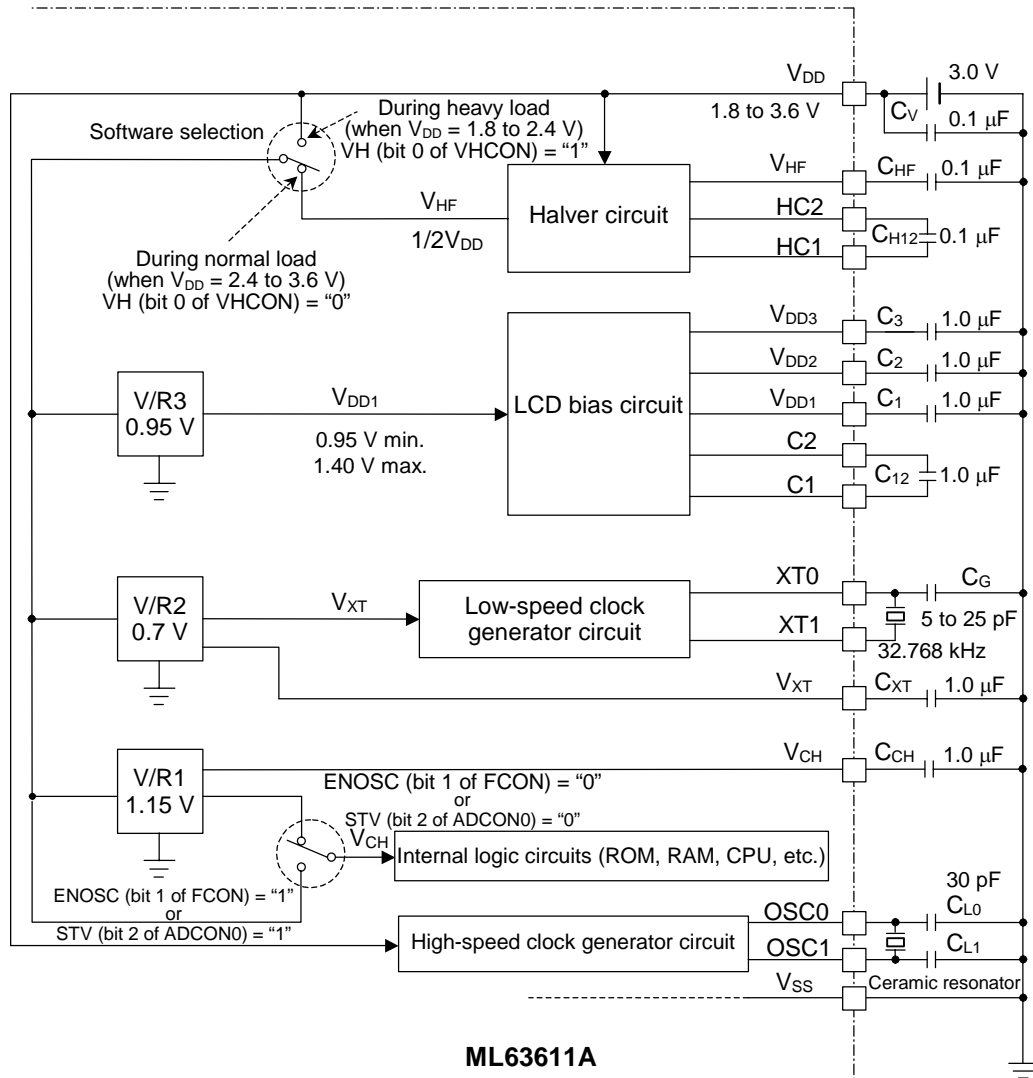


Figure 9 OPTION D Power Supply Circuit Configuration

**ELECTRICAL CHARACTERISTICS (3.0 V)****Absolute Maximum Ratings**

(V <sub>SS</sub> = 0 V)				
Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V <sub>DD1</sub>	Ta = 25°C	-0.3 to +1.8	V
Power Supply Voltage 2	V <sub>DD2</sub>	Ta = 25°C	-0.3 to +3.6	V
Power Supply Voltage 3	V <sub>DD3</sub>	Ta = 25°C	-0.3 to +5.4	V
Power Supply Voltage 4	V <sub>DD</sub>	Ta = 25°C	-0.3 to +3.9	V
Power Supply Voltage 5	V <sub>HF</sub>	Ta = 25°C	-0.3 to +3.9	V
Power Supply Voltage 6	V <sub>CH</sub>	Ta = 25°C	-0.3 to +3.9	V
Power Supply Voltage 7	V <sub>XT</sub>	Ta = 25°C	-0.3 to +3.9	V
Input Voltage 1	V <sub>IN1</sub>	V <sub>DD</sub> input, Ta = 25°C	-0.3 to V <sub>DD</sub> +0.3	V
Output Voltage 1	V <sub>OUT1</sub>	V <sub>DD1</sub> input, Ta = 25°C	-0.3 to V <sub>DD1</sub> +0.3	V
Output Voltage 2	V <sub>OUT2</sub>	V <sub>DD2</sub> input, Ta = 25°C	-0.3 to V <sub>DD2</sub> +0.3	V
Output Voltage 3	V <sub>OUT3</sub>	V <sub>DD3</sub> input, Ta = 25°C	-0.3 to V <sub>DD3</sub> +0.3	V
Output Voltage 4	V <sub>OUT4</sub>	V <sub>DD</sub> input, Ta = 25°C	-0.3 to V <sub>DD</sub> +0.3	V
Power Dissipation	P <sub>D</sub>	Ta = 25°C	8	mW
Storage Temperature	T <sub>STG</sub>	—	-55 to +150	°C

**Recommended Operating Conditions**

(V <sub>SS</sub> = 0 V)				
Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T <sub>OP</sub>	—	-20 to +70	°C
Operating Voltage	V <sub>DD</sub>	—	1.8 to 3.6	V
Crystal Oscillation Frequency	f <sub>XT</sub>	C <sub>G</sub> = 5 to 25 pF	32.768k	Hz
High-Speed RC Oscillator Frequency	f <sub>CRH</sub>	V <sub>DD</sub> = 1.8 to 3.6 V, R <sub>OSH</sub> = 75 kΩ	700k ±30%	Hz
High-Speed Ceramic Oscillation Frequency	f <sub>CH</sub>	V <sub>DD</sub> = 1.8 to 3.6 V	700k Max.	Hz



**DC Characteristics (1)**

The regulator for the LCD bias reference is not used.

( $V_{DD} = V_{DD2} = 3.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , 1/3 bias, DSPCNT = 0H,  $T_a = -20$  to  $+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	$I_{DD1}$	CPU in HALT state, LCD is turned OFF (High-speed clock oscillation stopped)	—	0.53	1.2	$\mu\text{A}$	1
Supply Current 2	$I_{DD2}$	CPU in HALT state, LCD in Power Down mode (High-speed clock oscillation stopped)	—	0.45	0.9	$\mu\text{A}$	
Supply Current 3	$I_{DD3}$	CPU operating, LCD is turned OFF (Low-speed clock oscillation; 32.768 kHz crystal oscillation)	—	2	4	$\mu\text{A}$	
Supply Current 4	$I_{DD4}$	CPU operating (High-speed clock oscillation; approx. 700 kHz RC oscillation)	—	450	700	$\mu\text{A}$	

The regulator for the LCD bias reference is used

( $V_{DD} = 3.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , 1/3 bias, DSPCNT = 0H,  $T_a = -20$  to  $+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	$I_{DD1}$	CPU in HALT state, LCD is turned OFF (High-speed clock oscillation stopped)	—	0.70	1.4	$\mu\text{A}$	1
Supply Current 2	$I_{DD2}$	CPU in HALT state, LCD in Power Down mode (High-speed clock oscillation stopped)	—	0.45	0.9	$\mu\text{A}$	
Supply Current 3	$I_{DD3}$	CPU operating, LCD is turned OFF (Low-speed clock oscillation; 32.768 kHz crystal oscillation)	—	2.2	4.5	$\mu\text{A}$	
Supply Current 4	$I_{DD4}$	CPU operating (High-speed clock oscillation; approx. 700 kHz RC oscillation)	—	450	700	$\mu\text{A}$	

**DC Characteristics (2)**

The regulator for the LCD bias reference is not used

( $V_{DD} = V_{DD2} = 3.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20$  to  $+70^\circ\text{C}$  unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
$V_{DD1}$ Voltage	$V_{DD1}$	1/3 bias, 1/2 bias	Typ.-0.1	$1/2 \times V_{DD}$	Typ.+0.1	V	1
$V_{DD2}$ Voltage	$V_{DD2}$	1/3 bias, 1/2 bias	Typ.-0.1	$V_{DD}$	Typ.+0.1	V	
$V_{DD3}$ Voltage	$V_{DD3}$	1/3 bias	Typ.-0.2	$3/2 \times V_{DD}$	Typ.+0.2	V	
		1/2 bias (connected to $V_{DD2}$ )	Typ.-0.1	$V_{DD}$	Typ.+0.1	V	

The regulator for the LCD bias reference is used

( $V_{DD} = 3.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20$  to  $+70^\circ\text{C}$  unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
$V_{DD1}$ Voltage	$V_{DD1}$	1/3 bias, 1/2 bias ( $T_a = 25^\circ\text{C}$ )	0.85	0.95	1.05	V	1
$V_{DD1}$ Voltage Temperature Deviation	$\Delta V_{DD1}$	—	—	-4	—	mV/ $^\circ\text{C}$	
$V_{DD2}$ Voltage	$V_{DD2}$	1/3 bias	Typ.-0.3	$2 \times V_{DD1}$	Typ.+0.3	V	
		1/2 bias (connected to $V_{DD1}$ )	Typ.-0.2	$V_{DD1}$	Typ.+0.2	V	
$V_{DD3}$ Voltage	$V_{DD3}$	1/3 bias	Typ.-0.4	$3 \times V_{DD1}$	Typ.+0.4	V	
		1/2 bias	Typ.-0.3	$2 \times V_{DD1}$	Typ.+0.3	V	

**DC Characteristics (3)**(V<sub>DD</sub> = 3.0 V, V<sub>SS</sub> = 0 V, Ta = -20 to +70°C unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V <sub>HF</sub> Voltage	V <sub>HF</sub>	—	—	1/2 × V <sub>DD</sub>	—	V	1
V <sub>CH</sub> Voltage	V <sub>CH</sub>	(under a normal load)	0.8	1.15	1.5	V	
		(under a heavy load)	V <sub>DD</sub> -0.2	V <sub>DD</sub>	V <sub>DD</sub> +0.1	V	
Crystal Oscillation Start Voltage	V <sub>STA</sub>	Oscillation start time: within 5 seconds	1.8	—	—	V	
Crystal Oscillation Hold Voltage	V <sub>HOLD</sub>	—	1.8	—	—	V	
External Crystal Oscillator Capacitance	C <sub>G</sub>	—	5	—	25	pF	
Internal Crystal Oscillator Capacitance	C <sub>D</sub>	—	20	25	30	pF	
External Ceramic Oscillator Capacitance	C <sub>LO</sub> , C <sub>L1</sub>	700kHz	—	33	—	pF	
Internal RC Oscillator Capacitance	C <sub>OS</sub>	—	8	12	16	pF	
BLD Judgment Voltage	V <sub>BLDC</sub>	LD1 = 1, LD0 = 1, Ta = 25°C	2.5	2.6	2.7	V	
		LD1 = 1, LD0 = 0, Ta = 25°C	2.3	2.4	2.5	V	
		LD1 = 0, LD0 = 1, Ta = 25°C	1.9	2.0	2.1	V	
		LD1 = 0, LD0 = 0, Ta = 25°C	1.7	1.8	1.9	V	
BLD Judgment Voltage Temperature Deviation	ΔV <sub>BLDC</sub>	Ta = -20 to +25°C	—	1.70	2.10	mV/°C	
		Ta = +25 to +70°C	—	1.50	2.00	mV/°C	

## DC Characteristics (4)

( $V_{DD} = 3.0\text{ V}$ ,  $V_{DD1} = 1.50\text{ V}$ ,  $V_{DD2} = 3.00\text{ V}$ ,  $V_{DD3} = 4.50\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }+70^\circ\text{C}$  unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	$I_{OH1}$	$V_{OH1} = V_{DD} - 0.5\text{ V}$	-6.0	-3.5	-1.0	mA	2
	$I_{OL1}$	$V_{OL1} = 0.5\text{ V}$	1.0	3.5	6.0	mA	
Output Current 2 (MD, MDB)	$I_{OH2}$	$V_{OH2} = V_{DD} - 0.7\text{ V}$	-20.0	-11.0	-3.5	mA	
	$I_{OL2}$	$V_{OL2} = 0.7\text{ V}$	1.0	3.5	6.0	mA	
Output Current 3 (L0 to L63)	$I_{OH3}$	$V_{OH3} = V_{DD3} - 0.2\text{ V}$ ( $V_{DD3}$ level)	—	—	-4	$\mu\text{A}$	
	$I_{OMH3}$	$V_{OMH3} = V_{DD2} + 0.2\text{ V}$ ( $V_{DD2}$ level)	4	—	—	$\mu\text{A}$	
	$I_{OMH3S}$	$V_{OMH3S} = V_{DD2} - 0.2\text{ V}$ ( $V_{DD2}$ level)	—	—	-4	$\mu\text{A}$	
	$I_{OML3}$	$V_{OML3} = V_{DD1} + 0.2\text{ V}$ ( $V_{DD1}$ level)	4	—	—	$\mu\text{A}$	
	$I_{OML3S}$	$V_{OML3S} = V_{DD1} - 0.2\text{ V}$ ( $V_{DD1}$ level)	—	—	-4	$\mu\text{A}$	
	$I_{OL3}$	$V_{OL3} = V_{SS} + 0.2\text{ V}$ ( $V_{SS}$ level)	4	—	—	$\mu\text{A}$	
Output Current 4* (L32 to L35)	$I_{OH4}$	$V_{OH4} = V_{DD} - 0.5\text{ V}$	-12.0	-6.5	-2.0	mA	
	$I_{OL4}$	$V_{OL4} = 0.5\text{ V}$	1.0	3.5	6.0	mA	
Output Current 5 (OSC1)	$I_{OH5R}$	$V_{OH5R} = V_{DD} - 0.5\text{ V}$ (RC oscillation)	-2.5	-1.3	-0.25	mA	
	$I_{OL5R}$	$V_{OL5R} = 0.5\text{ V}$ (RC oscillation)	0.25	1.5	2.5	mA	
	$I_{OH5C}$	$V_{OH5C} = V_{DD} - 0.5\text{ V}$ (ceramic oscillation)	-500	-250	-100	$\mu\text{A}$	
	$I_{OL5C}$	$V_{OL5C} = 0.5\text{ V}$ (ceramic oscillation)	200	500	800	$\mu\text{A}$	
Output Current 6 (RT0, RT1, RS0, RS1, CRT0, CS0, CS1)	$I_{OH6}$	$V_{OH6} = V_{DD} - 0.1\text{ V}$	-2.5	-0.8	-0.3	mA	
	$I_{OL6}$	$V_{OL6} = 0.1\text{ V}$	0.3	1.3	2.5	mA	
Output Leakage Current (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	$I_{OOH}$	$V_{OH} = V_{DD}$	—	—	0.3	$\mu\text{A}$	
	$I_{OOL}$	$V_{OL} = V_{SS}$	-0.3	—	—	$\mu\text{A}$	

\* Applies only when L32 to L35 are selected as the output port in a mask option.

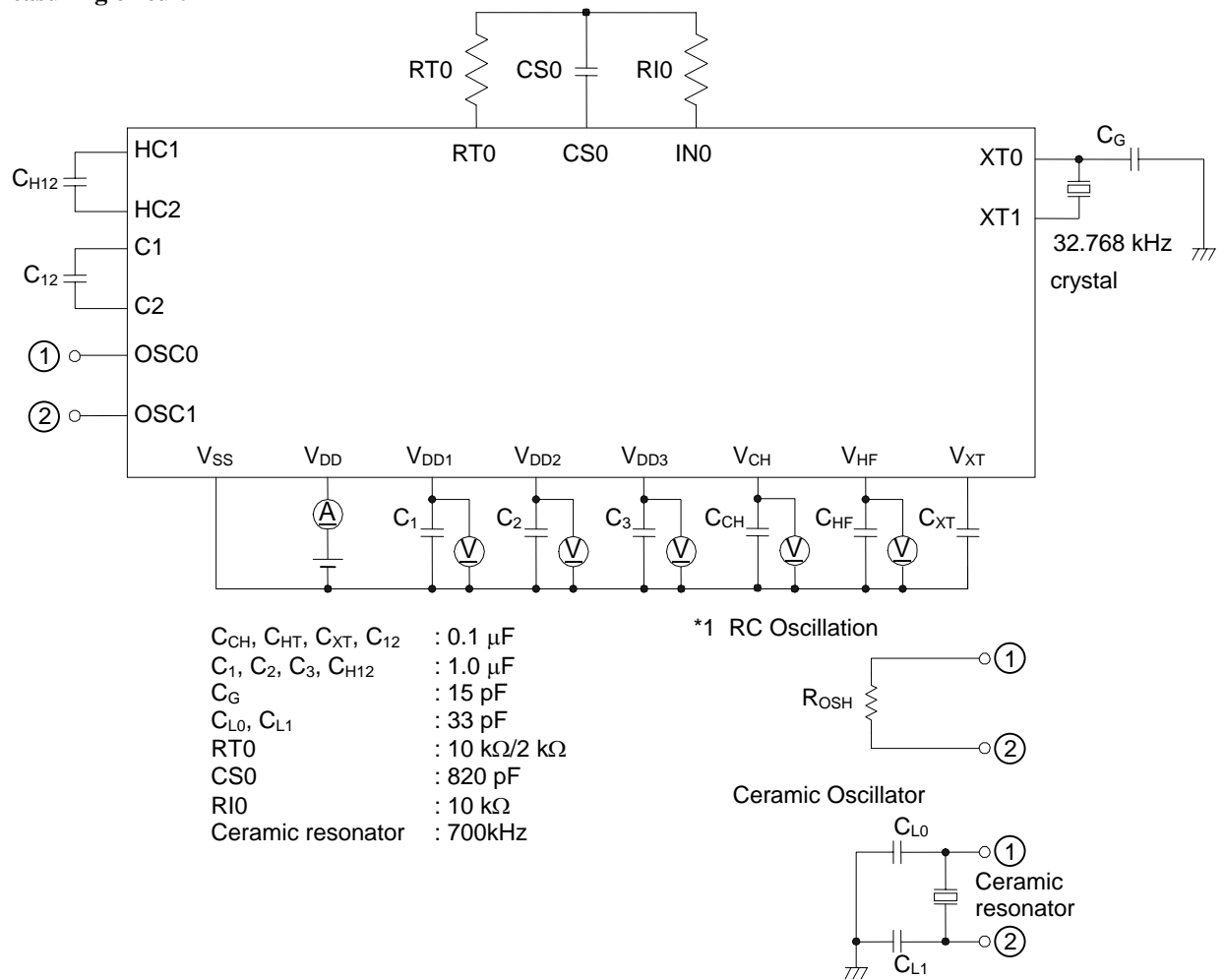
**DC Characteristics (5)**(V<sub>DD</sub> = 3.0 V, V<sub>DD1</sub> = 1.50 V, V<sub>DD2</sub> = 3.00 V, V<sub>DD3</sub> = 4.50 V, V<sub>SS</sub> = 0 V, Ta = -20 to +70°C unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P0.0 to P0.3) (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	I <sub>IH1</sub>	V <sub>IH1</sub> = V <sub>DD</sub> (when pulled down)	7.5	50	100	μA	3
	I <sub>IL1</sub>	V <sub>IL1</sub> = V <sub>SS</sub> (when pulled up)	-100	-50	-7.5	μA	
	I <sub>IH1Z</sub>	V <sub>IH1</sub> = V <sub>DD</sub> (in a high impedance state)	0	—	1	μA	
	I <sub>IL1Z</sub>	V <sub>IL1</sub> = V <sub>SS</sub> (in a high impedance state)	-1	—	0	μA	
Input Current 2 (OSC0)	I <sub>IL2</sub>	V <sub>IL2</sub> = V <sub>SS</sub> (when pulled up)	-350	-170	-30	μA	
	I <sub>IH2R</sub>	V <sub>IH2R</sub> = V <sub>DD</sub> (RC oscillation)	0	—	1	μA	
	I <sub>IL2R</sub>	V <sub>IL2R</sub> = V <sub>SS</sub> (RC oscillation)	-1	—	0	μA	
	I <sub>IH2C</sub>	V <sub>IH2C</sub> = V <sub>DD</sub> (ceramic oscillation)	0.5	1.8	4.0	μA	
	I <sub>IL2C</sub>	V <sub>IL2C</sub> = V <sub>SS</sub> (ceramic oscillation)	-4.0	-1.8	-0.5	μA	
Input Current 3 (IN0, IN1)	I <sub>IH3</sub>	V <sub>IH3</sub> = V <sub>DD</sub> (when pulled down)	80	250	500	μA	
	I <sub>IH3Z</sub>	V <sub>IH3</sub> = V <sub>DD</sub> (in a high impedance state)	0	—	1	μA	
	I <sub>IL3Z</sub>	V <sub>IL3</sub> = V <sub>SS</sub> (in a high impedance state)	-1	—	0	μA	
Input Current 4 (RESET)	I <sub>IH4</sub>	V <sub>IH4</sub> = V <sub>DD</sub>	150	1100	2400	μA	
	I <sub>IL4</sub>	V <sub>IL4</sub> = V <sub>SS</sub>	-1	—	0	μA	
Input Current 5 (TST1, TST2)	I <sub>IH5</sub>	V <sub>IH5</sub> = V <sub>DD</sub>	0.5	3.0	5.5	mA	
	I <sub>IL5</sub>	V <sub>IL5</sub> = V <sub>SS</sub>	-1.0	—	0	μA	

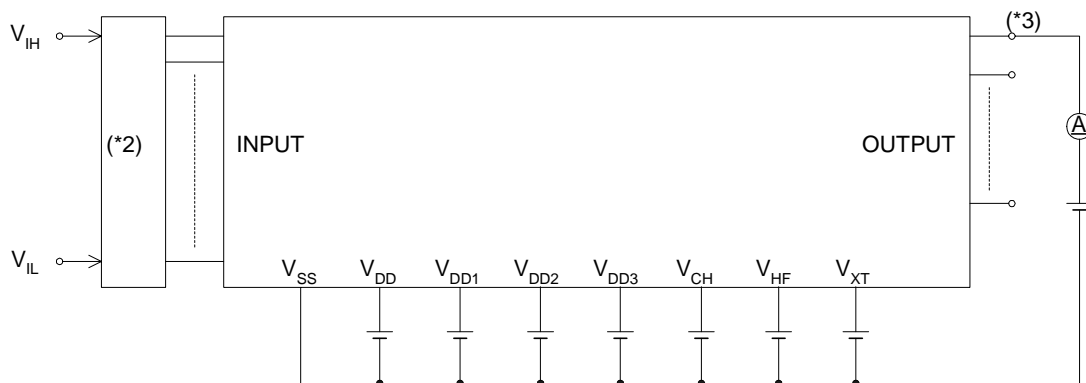
**DC Characteristics (6)**(V<sub>DD</sub> = 3.0 V, V<sub>DD1</sub> = 1.50 V, V<sub>DD2</sub> = 3.00 V, V<sub>DD3</sub> = 4.50 V, V<sub>SS</sub> = 0 V, Ta = -20 to +70°C unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Voltage 1 (P0.0 to P0.3) (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	V <sub>IH1</sub>	—	2.4	—	3.0	V	4
	V <sub>IL1</sub>	—	0	—	0.6	V	
Input Voltage 2 (OSC0)	V <sub>IH2</sub>	—	2.4	—	3.0	V	
	V <sub>IL2</sub>	—	0	—	0.6	V	
Input Voltage 3 (IN0, IN1)	V <sub>IH3</sub>	—	2.4	—	3.0	V	
	V <sub>IL3</sub>	—	0	—	0.6	V	
Input Voltage 4 (RESET, TST1, TST2)	V <sub>IH4</sub>	—	2.4	—	3.0	V	
	V <sub>IL4</sub>	—	0	—	0.6	V	
Hysteresis Width 1 (P0.0 to P0.3) (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	ΔV <sub>T1</sub>	—	0.2	0.5	1.0	V	
Hysteresis Width 2 (RESET, TST1, TST2)	ΔV <sub>T2</sub>	—	0.2	0.5	1.0	V	
Input Pin Capacitance (P0.0 to P0.3) (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	C <sub>IN</sub>	—	—	—	5	pF	—

**Measuring circuit 1**



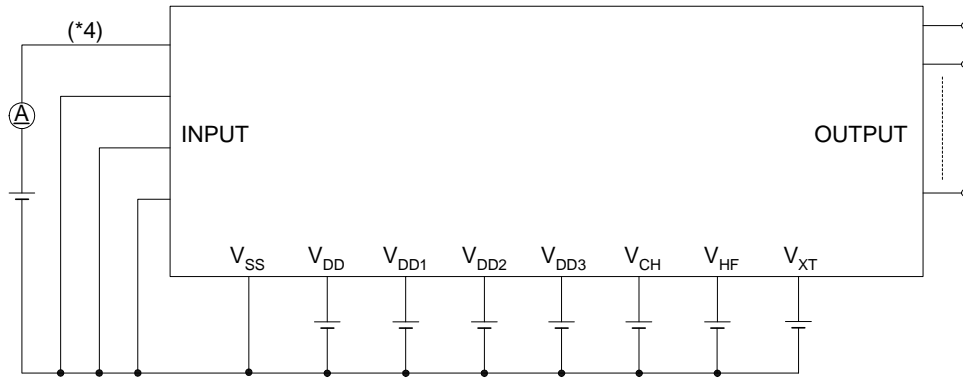
**Measuring circuit 2**



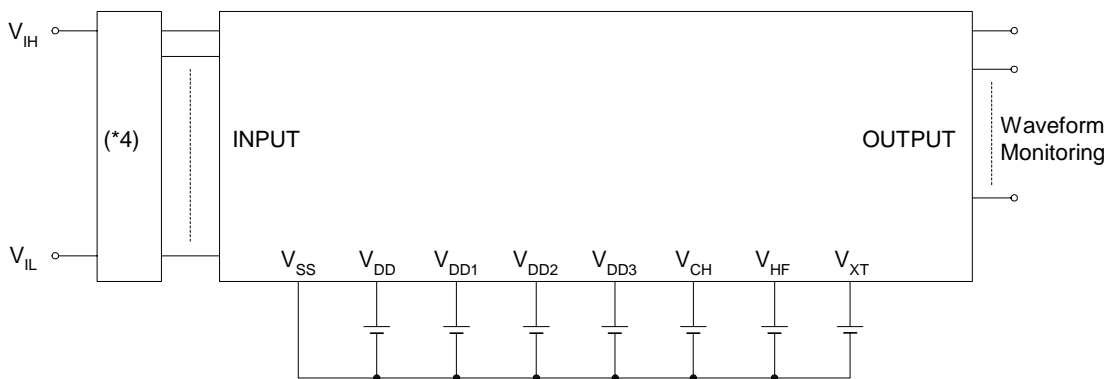
\*2 Input logic circuit to determine a specified state.

\*3 To be repeated for the specified output pins.

**Measuring circuit 3**



**Measuring circuit 4**



\*4 To be repeated for the specified input pins.



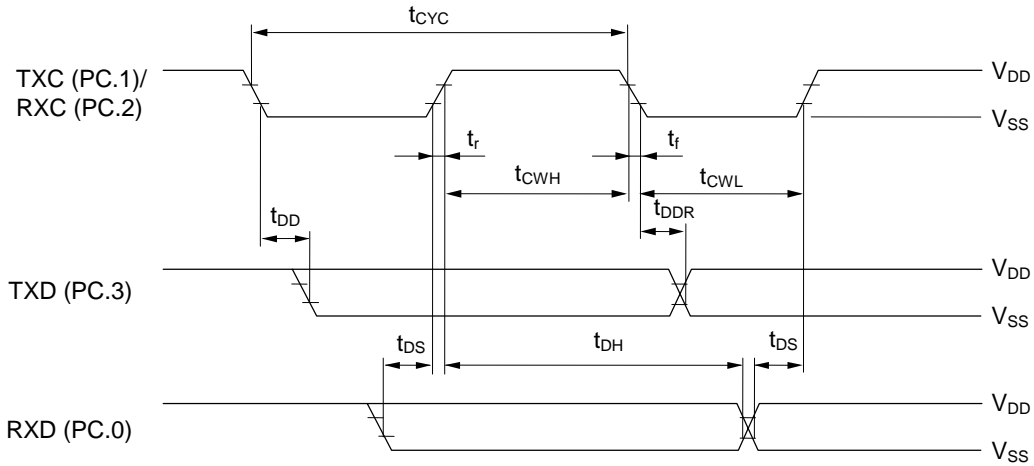
**AC Characteristics (Serial Interface, Serial Port)**

( $V_{DD} = 3.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }+70^\circ\text{C}$  unless otherwise specified)

Synchronous Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TXC/RXC Input Fall Time	$t_f$	—	—	—	1	$\mu\text{s}$
TXC/RXC Input Rise Time	$t_r$	—	—	—	1	$\mu\text{s}$
TXC/RXC Input “L” Level Pulse Width	$t_{CWL}$	—	0.8	—	—	$\mu\text{s}$
TXC/RXC Input “H” Level Pulse Width	$t_{CWH}$	—	0.8	—	—	$\mu\text{s}$
TXC/RXC Input Cycle Time	$t_{CYC}$	—	2	—	—	$\mu\text{s}$
TXC/RXC Output Cycle Time	$t_{CYC(0)}$	CPU operating at 32.768 kHz	—	30.5	—	$\mu\text{s}$
TXD Output Delay Time	$t_{DDR}$	Output load capacitance 10 pF	—	—	0.4	$\mu\text{s}$
RXD Input Setup Time	$t_{DS}$	—	0.5	—	—	$\mu\text{s}$
RXD Input Hold Time	$t_{DH}$	—	0.8	—	—	$\mu\text{s}$

Synchronous communication timing  
 (“H” level = 2.4 V, “L” level = 0.6 V)

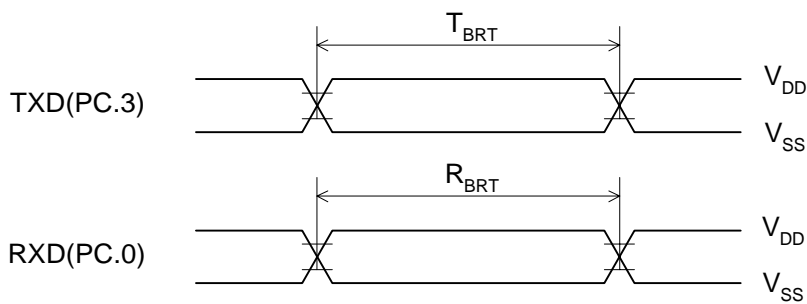


UART Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit Baud Rate	$T_{BRT}$	$T_{BRT} = 1/f_{BRT}$ $T_{CR} = 1/f_{OSC}$	$T_{BRT} - T_{CR}$	$T_{BRT}$	$T_{BRT} + T_{CR}$	s
Receive Baud Rate	$R_{BRT}$	$R_{BRT} = 1/f_{BRT}$	$R_{BRT} \times 0.97$	$R_{BRT}$	$R_{BRT} \times 1.03$	s

$f_{BRT}$ : Baud rates (9600, 4800, 2400 and 1200 bps)

UART communication timing  
 (“H” level = 2.4 V, “L” level = 0.6 V)



**AC Characteristics (RC Oscillation Type A/D Converter)**

(V<sub>DD</sub> = 3.0 V, V<sub>SS</sub> = 0 V, Ta = -20 to +70°C unless otherwise specified)

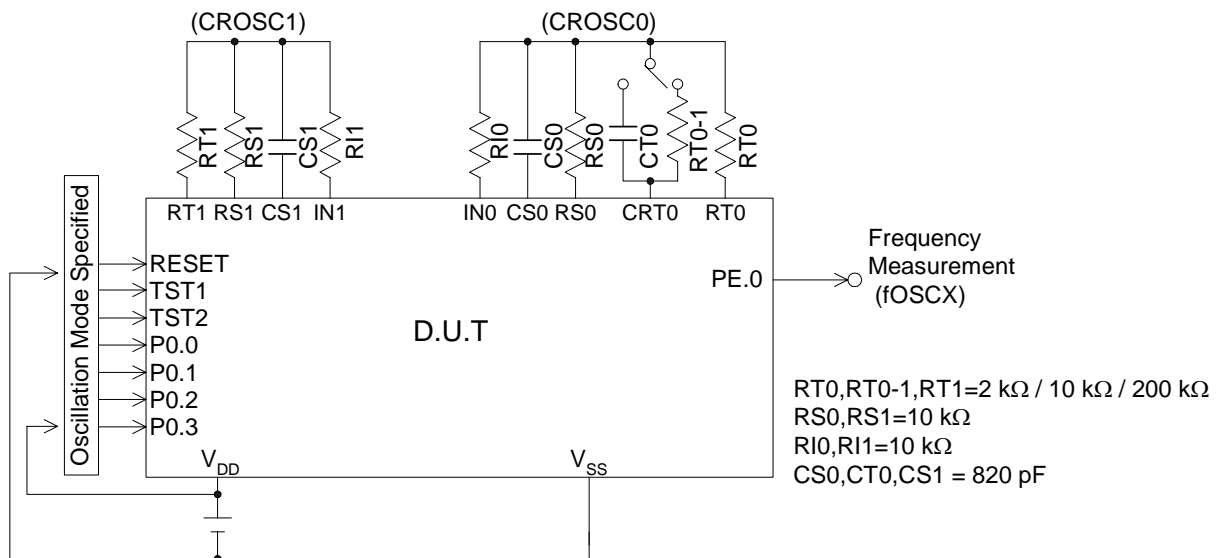
Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Resistor for Oscillation	RS0, RS1, RT0, RT0-1, RT1	CS0, CT0, CS1 ≥ 740 pF	1	—	—	kΩ	5
Input Current Limiting Resistor	RI0, RI1	—	1	10	—	kΩ	
Oscillation Frequency	f <sub>osc1</sub>	Resistor for oscillation = 2 kΩ	170	210	250	kHz	
	f <sub>osc2</sub>	Resistor for oscillation = 10 kΩ	38.0	47.0	56.0	kHz	
	f <sub>osc3</sub>	Resistor for oscillation = 200 kΩ	2.30	2.80	3.30	kHz	
RS•RT Oscillation Frequency Ratio (*)	Kf1	RT0, RT0-1, RT1 = 2 kΩ	3.9	4.2	4.5	—	
	Kf2	RT0, RT0-1, RT1 = 10 kΩ	0.990	1.0	1.010	—	
	Kf3	RT0, RT0-1, RT1 = 200 kΩ	0.057	0.061	0.065	—	

\* Kfx is the ratio of the oscillation frequency by a sensor resistor to the oscillation frequency by a reference resistor in the same condition.

$$\frac{f_{oscx} \text{ (RT0 - CS0 Oscillation)}}{f_{oscx} \text{ (RS0 - CS0 Oscillation)}}, \quad \frac{f_{oscx} \text{ (RT0-1 - CS0 Oscillation)}}{f_{oscx} \text{ (RS0 - CS0 Oscillation)}}, \quad \frac{f_{oscx} \text{ (RT1 - CS1 Oscillation)}}{f_{oscx} \text{ (RS1 - CS1 Oscillation)}}$$

(x = 1, 2, 3)

**Measuring circuit 5**



**ELECTRICAL CHARACTERISTICS (1.5 V)****Absolute Maximum Ratings**(V<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V <sub>DD1</sub>	Ta = 25°C	-0.3 to +1.8	V
Power Supply Voltage 2	V <sub>DD2</sub>	Ta = 25°C	-0.3 to +3.4	V
Power Supply Voltage 3	V <sub>DD3</sub>	Ta = 25°C	-0.3 to +5.1	V
Power Supply Voltage 4	V <sub>DD</sub>	Ta = 25°C	-0.3 to +2.0	V
Power Supply Voltage 5	V <sub>CH</sub>	Ta = 25°C	-0.3 to +2.0	V
Power Supply Voltage 6	V <sub>XT</sub>	Ta = 25°C	-0.3 to +2.0	V
Input Voltage 1	V <sub>IN1</sub>	V <sub>DD</sub> input, Ta = 25°C	-0.3 to V <sub>DD</sub> +0.3	V
Output Voltage 1	V <sub>OUT1</sub>	V <sub>DD1</sub> input, Ta = 25°C	-0.3 to V <sub>DD1</sub> +0.3	V
Output Voltage 2	V <sub>OUT2</sub>	V <sub>DD2</sub> input, Ta = 25°C	-0.3 to V <sub>DD2</sub> +0.3	V
Output Voltage 3	V <sub>OUT3</sub>	V <sub>DD3</sub> input, Ta = 25°C	-0.3 to V <sub>DD3</sub> +0.3	V
Output Voltage 4	V <sub>OUT4</sub>	V <sub>DD</sub> input, Ta = 25°C	-0.3 to V <sub>DD</sub> +0.3	V
Power Dissipation	P <sub>D</sub>	Ta = 25°C	1	mW
Storage Temperature	T <sub>STG</sub>	—	-55 to +150	°C

**Recommended Operating Conditions**(V<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T <sub>OP</sub>	—	-20 to +70	°C
Operating Voltage	V <sub>DD</sub>	—	1.3 to 1.7	V
Crystal Oscillation Frequency	f <sub>XT</sub>	C <sub>G</sub> = 5 to 25 pF	32.768 k	Hz
High-Speed RC Oscillator Frequency	f <sub>CRH</sub>	V <sub>DD</sub> = 1.3 to 1.7V, R <sub>OSH</sub> = 200 kΩ	200 k ± 30 %	Hz

**DC Characteristics (1)**

The regulator for the LCD bias reference is not used.

( $V_{DD} = V_{DD1} = 1.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , 1/3 bias, DSPCNT = 0H,  $T_a = -20\text{ to }+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	$I_{DD1}$	CPU in HALT state, LCD is turned OFF (High-speed clock oscillation stopped)	—	1.4	2.8	$\mu\text{A}$	1
Supply Current 2	$I_{DD2}$	CPU in HALT state, LCD in Power Down mode (High-speed clock oscillation stopped)	—	0.9	1.8	$\mu\text{A}$	
Supply Current 3	$I_{DD3}$	CPU operating, LCD is turned OFF (Low-speed clock oscillation; 32.768 kHz crystal oscillation)	—	4.0	8.0	$\mu\text{A}$	
Supply Current 4	$I_{DD4}$	CPU operating (High-speed clock oscillation; approx. 200 kHz RC oscillation)	—	80	150	$\mu\text{A}$	

The regulator for the LCD bias reference is used.

( $V_{DD} = 1.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , 1/3 bias, DSPCNT = 0H,  $T_a = -20\text{ to }+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	$I_{DD1}$	CPU in HALT state, LCD is turned OFF (High-speed clock oscillation stopped)	—	1.6	3.0	$\mu\text{A}$	1
Supply Current 2	$I_{DD2}$	CPU in HALT state, LCD in Power Down mode (High-speed clock oscillation stopped)	—	0.9	1.8	$\mu\text{A}$	
Supply Current 3	$I_{DD3}$	CPU operating, LCD is turned OFF (Low-speed clock oscillation; 32.768 kHz crystal oscillation)	—	4.2	8.5	$\mu\text{A}$	
Supply Current 4	$I_{DD4}$	CPU operating (High-speed clock oscillation; approx. 200 kHz RC oscillation)	—	80	150	$\mu\text{A}$	

**DC Characteristics (2)**

The regulator for the LCD bias reference is not used.

( $V_{DD} = V_{DD1} = 1.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }+70^\circ\text{C}$  unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
$V_{DD1}$ Voltage	$V_{DD1}$	1/3 bias, 1/2 bias	Typ.-0.1	$V_{DD}$	Typ.+0.1	V	1
$V_{DD2}$ Voltage	$V_{DD2}$	1/3 bias	Typ.-0.2	$2 \times V_{DD}$	Typ.+0.2	V	
		1/2 bias (connected to $V_{DD1}$ )	Typ.-0.1	$V_{DD}$	Typ.+0.1	V	
$V_{DD3}$ Voltage	$V_{DD3}$	1/3 bias	Typ.-0.3	$3 \times V_{DD}$	Typ.+0.3	V	
		1/2 bias	Typ.-0.2	$2 \times V_{DD}$	Typ.+0.2	V	

The regulator for the LCD bias reference is used.

( $V_{DD} = 1.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }+70^\circ\text{C}$  unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
$V_{DD1}$ Voltage	$V_{DD1}$	1/3 bias, 1/2 bias ( $T_a = 25^\circ\text{C}$ )	0.85	0.95	1.05	V	1
$V_{DD1}$ Voltage Temperature Deviation	$\Delta V_{DD1}$	—	—	-4	—	mV/ °C	
$V_{DD2}$ Voltage	$V_{DD2}$	1/3 bias	Typ.-0.3	$2 \times V_{DD1}$	Typ.+0.3	V	
		1/2 bias (connected to $V_{DD1}$ )	Typ.-0.2	$V_{DD1}$	Typ.+0.2	V	
$V_{DD3}$ Voltage	$V_{DD3}$	1/3 bias	Typ.-0.4	$3 \times V_{DD1}$	Typ.+0.4	V	
		1/2 bias	Typ.-0.3	$2 \times V_{DD1}$	Typ.+0.3	V	

**DC Characteristics (3)**(V<sub>DD</sub> = 1.5 V, V<sub>SS</sub> = 0 V, Ta = -20 to +70°C unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V <sub>CH</sub> Voltage	V <sub>CH</sub>	(under a normal load)	0.8	1.15	1.5	V	1
		(under a heavy load)	V <sub>DD</sub> -0.2	V <sub>DD</sub>	V <sub>DD</sub> +0.1	V	
Crystal Oscillation Start Voltage	V <sub>STA</sub>	Oscillation start time: within 5 seconds	1.3	—	—	V	
Crystal Oscillation Hold Voltage	V <sub>HOLD</sub>	—	1.3	—	—	V	
External Crystal Oscillator Capacitance	C <sub>G</sub>	—	5	—	25	pF	
Internal Crystal Oscillator Capacitance	C <sub>D</sub>	—	20	25	30	pF	
Internal RC Oscillator Capacitance	C <sub>OS</sub>	—	8	12	16	pF	

**DC Characteristics (4)**(V<sub>DD</sub> = 1.5 V, V<sub>DD1</sub> = 1.50 V, V<sub>DD2</sub> = 3.00 V, V<sub>DD3</sub> = 4.50 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -20 to +70°C unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	I <sub>OH1</sub>	V <sub>OH1</sub> = V <sub>DD</sub> - 0.5 V	-2.5	-1.4	-0.4	mA	2
	I <sub>OL1</sub>	V <sub>OL1</sub> = 0.5 V	0.4	1.4	2.5	mA	
Output Current 2 (MD, MDB)	I <sub>OH2</sub>	V <sub>OH2</sub> = V <sub>DD</sub> - 0.7 V	-4.0	-2.0	-0.5	mA	
	I <sub>OL2</sub>	V <sub>OL2</sub> = 0.7 V	0.5	2.0	4.0	mA	
Output Current 3 (L0 to L63)	I <sub>OH3</sub>	V <sub>OH3</sub> = V <sub>DD3</sub> - 0.2 V (V <sub>DD3</sub> level)	—	—	-4	μA	
	I <sub>OMH3</sub>	V <sub>OMH3</sub> = V <sub>DD2</sub> + 0.2 V (V <sub>DD2</sub> level)	4	—	—	μA	
	I <sub>OMH3S</sub>	V <sub>OMH3S</sub> = V <sub>DD2</sub> - 0.2 V (V <sub>DD2</sub> level)	—	—	-4	μA	
	I <sub>OML3</sub>	V <sub>OML3</sub> = V <sub>DD1</sub> + 0.2 V (V <sub>DD1</sub> level)	4	—	—	μA	
	I <sub>OML3S</sub>	V <sub>OML3S</sub> = V <sub>DD1</sub> - 0.2 V (V <sub>DD1</sub> level)	—	—	-4	μA	
	I <sub>OL3</sub>	V <sub>OL3</sub> = V <sub>SS</sub> + 0.2 V (V <sub>SS</sub> level)	4	—	—	μA	
Output Current 4* (L32 to L35)	I <sub>OH4</sub>	V <sub>OH4</sub> = V <sub>DD</sub> - 0.5 V	-3.5	-1.7	-0.6	mA	
	I <sub>OL4</sub>	V <sub>OL4</sub> = 0.5 V	0.4	1.4	2.5	mA	
Output Current 5 (OSC1)	I <sub>OH5R</sub>	V <sub>OH5R</sub> = V <sub>DD</sub> - 0.5 V (RC oscillation)	-1.4	-0.7	-0.1	mA	
	I <sub>OL5R</sub>	V <sub>OL5R</sub> = 0.5 V (RC oscillation)	0.1	0.8	1.4	mA	
Output Current 6 (RT0, RT1, RS0, RS1, CRT0, CS0, CS1)	I <sub>OH6</sub>	V <sub>OH6</sub> = V <sub>DD</sub> - 0.1 V	-1.1	-0.4	-0.1	mA	
	I <sub>OL6</sub>	V <sub>OL6</sub> = 0.1 V	0.1	0.6	1.2	mA	
Output Leakage Current (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	I <sub>OOH</sub>	V <sub>OH</sub> = V <sub>DD</sub>	—	—	0.3	μA	
	I <sub>OOL</sub>	V <sub>OL</sub> = V <sub>SS</sub>	-0.3	—	—	μA	

\* Applies only when L32 to L35 are selected as the output port in a mask option.



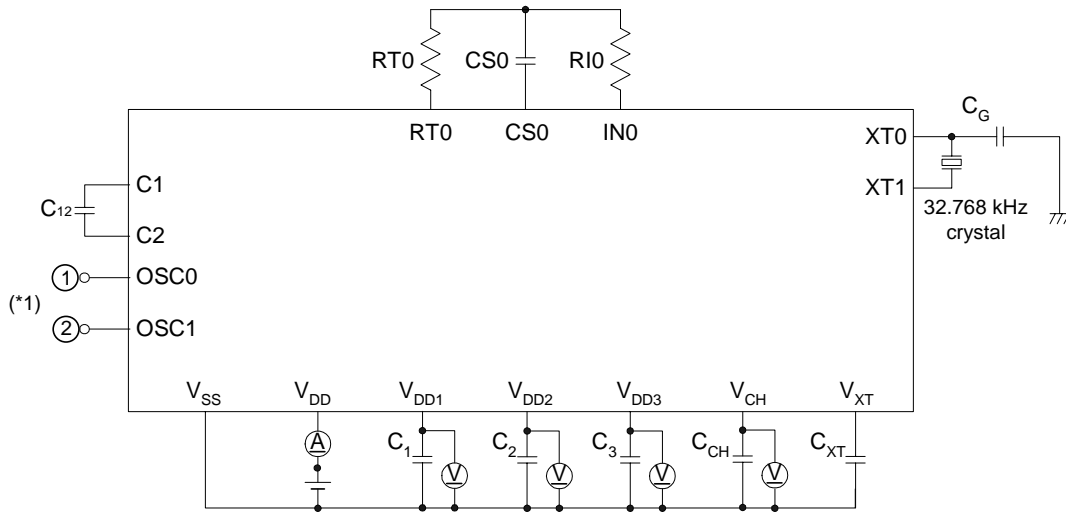
**DC Characteristics (5)**(V<sub>DD</sub> = 1.5 V, V<sub>DD1</sub> = 1.50 V, V<sub>DD2</sub> = 3.00 V, V<sub>DD3</sub> = 4.50 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -20 to +70°C unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P0.0 to P0.3) (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	I <sub>IH1</sub>	V <sub>IH1</sub> = V <sub>DD</sub> (when pulled down)	1.2	5.0	11.0	μA	3
	I <sub>IL1</sub>	V <sub>IL1</sub> = V <sub>SS</sub> (when pulled up)	-11.0	-5.0	-1.2	μA	
	I <sub>IH1Z</sub>	V <sub>IH1</sub> = V <sub>DD</sub> (in a high impedance state)	0	—	1	μA	
	I <sub>IL1Z</sub>	V <sub>IL1</sub> = V <sub>SS</sub> (in a high impedance state)	-1	—	0	μA	
Input Current 2 (OSC0)	I <sub>IL2</sub>	V <sub>IL2</sub> = V <sub>SS</sub> (when pulled up)	-100	-50	-10	μA	
	I <sub>IH2R</sub>	V <sub>IH2R</sub> = V <sub>DD</sub> (RC oscillation)	0	—	1	μA	
	I <sub>IL2R</sub>	V <sub>IL2R</sub> = V <sub>SS</sub> (RC oscillation)	-1	—	0	μA	
Input Current 3 (IN0, IN1)	I <sub>IH3</sub>	V <sub>IH3</sub> = V <sub>DD</sub> (when pulled up)	10	50	100	μA	
	I <sub>IH3Z</sub>	V <sub>IH3</sub> = V <sub>DD</sub> (in a high impedance state)	0	—	1	μA	
	I <sub>IL3Z</sub>	V <sub>IL3</sub> = V <sub>SS</sub> (in a high impedance state)	-1	—	0	μA	
Input Current 4 (RESET)	I <sub>IH4</sub>	V <sub>IH4</sub> = V <sub>DD</sub>	10	180	350	μA	
	I <sub>IL4</sub>	V <sub>IL4</sub> = V <sub>SS</sub>	-1	—	0	μA	
Input Current 5 (TST1, TST2)	I <sub>IH5</sub>	V <sub>IH5</sub> = V <sub>DD</sub>	50	750	1500	μA	
	I <sub>IL5</sub>	V <sub>IL5</sub> = V <sub>SS</sub>	-1.0	—	0	μA	

**DC Characteristics (6)**(V<sub>DD</sub> = 1.5 V, V<sub>DD1</sub> = 1.50 V, V<sub>DD2</sub> = 3.00 V, V<sub>DD3</sub> = 4.50 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -20 to +70°C unless otherwise specified)

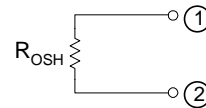
Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Voltage 1 (P0.0 to P0.3) (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	V <sub>IH1</sub>	—	1.2	—	1.5	V	4
	V <sub>IL1</sub>	—	0	—	0.3	V	
Input Voltage 2 (OSC0)	V <sub>IH2</sub>	—	1.2	—	1.5	V	
	V <sub>IL2</sub>	—	0	—	0.3	V	
Input Voltage 3 (IN0, IN1)	V <sub>IH3</sub>	—	1.2	—	1.5	V	
	V <sub>IL3</sub>	—	0	—	0.3	V	
Input Voltage 4 (RESET, TST1, TST2)	V <sub>IH4</sub>	—	1.2	—	1.5	V	
	V <sub>IL4</sub>	—	0	—	0.3	V	
Hysteresis Width 1 (P0.0 to P0.3) (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	ΔV <sub>T1</sub>	—	0.05	0.1	0.3	V	
Hysteresis Width 2 (RESET, TST1, TST2)	ΔV <sub>T2</sub>	—	0.05	0.1	0.3	V	
Input Pin Capacitance (P0.0 to P0.3) (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	C <sub>IN</sub>	—	—	—	5	pF	—

**Measuring circuit 1**

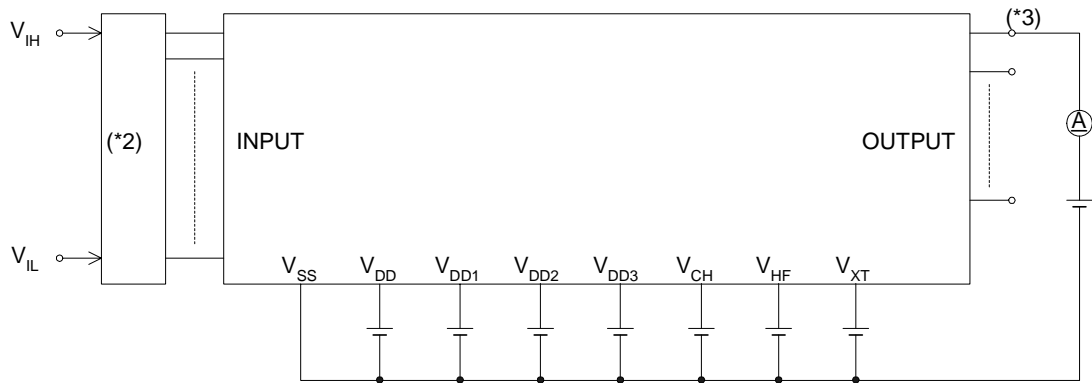


- $C_{CH}, C_{XT}$  : 0.1  $\mu$ F
- $C_1, C_2, C_3, C_{12}$  : 1.0  $\mu$ F
- $C_G$  : 15 pF
- $RT0$  : 10 k  $\Omega$  / 2 k  $\Omega$
- $CS0$  : 820 pF
- $RI0$  : 10 k  $\Omega$

\*1 RC Oscillation



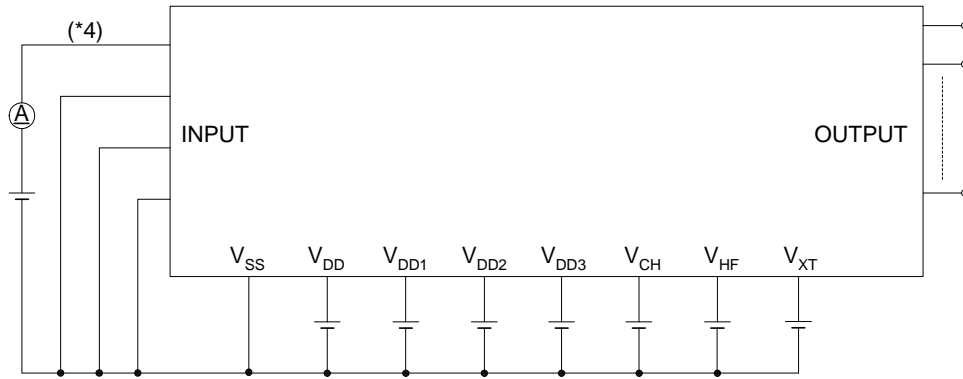
**Measuring circuit 2**



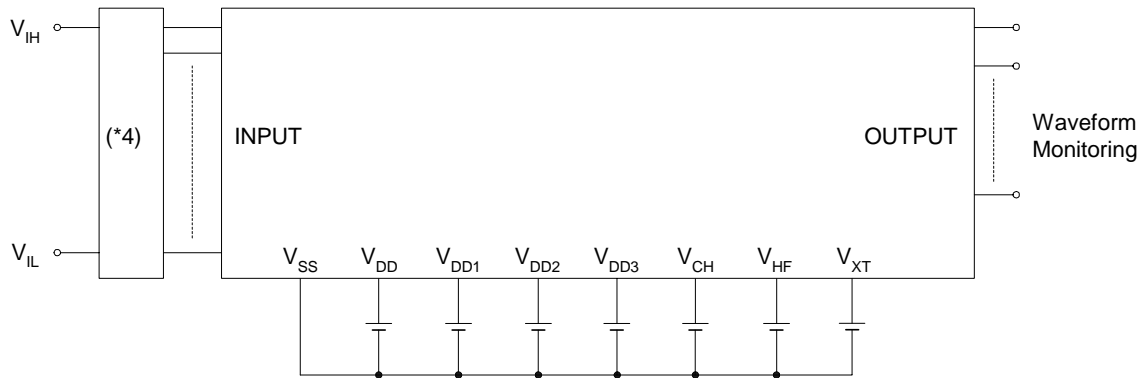
\*2 Input logic circuit to determine a specified state.

\*3 To be repeated for the specified output pins.

**Measuring circuit 3**



**Measuring circuit 4**



\*4 To be repeated for the specified input pins.

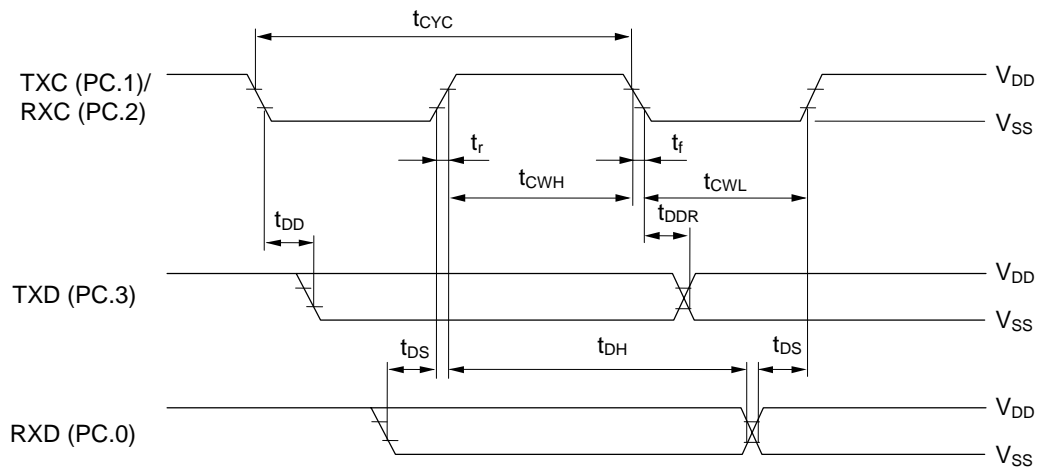
**AC Characteristics (Serial Interface, Serial Port)**

( $V_{DD} = 1.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }+70^\circ\text{C}$  unless otherwise specified)

Synchronous Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TXC/RXC Input Fall Time	$t_f$	—	—	—	1	$\mu\text{s}$
TXC/RXC Input Rise Time	$t_r$	—	—	—	1	$\mu\text{s}$
TXC/RXC Input “L” Level Pulse Width	$t_{CWL}$	—	0.8	—	—	$\mu\text{s}$
TXC/RXC Input “H” Level Pulse Width	$t_{CWH}$	—	0.8	—	—	$\mu\text{s}$
TXC/RXC Input Cycle Time	$t_{CYC}$	—	2	—	—	$\mu\text{s}$
TXC/RXC Output Cycle Time	$t_{CYC(O)}$	CPU operating at 32.768 kHz	—	30.5	—	$\mu\text{s}$
TXD Output Delay Time	$t_{DDR}$	Output load capacitance 10 pF	—	—	0.4	$\mu\text{s}$
RXD Input Setup Time	$t_{DS}$	—	0.5	—	—	$\mu\text{s}$
RXD Input Hold Time	$t_{DH}$	—	0.8	—	—	$\mu\text{s}$

Synchronous communication timing  
 (“H” level = 1.2 V, “L” level = 0.3 V)



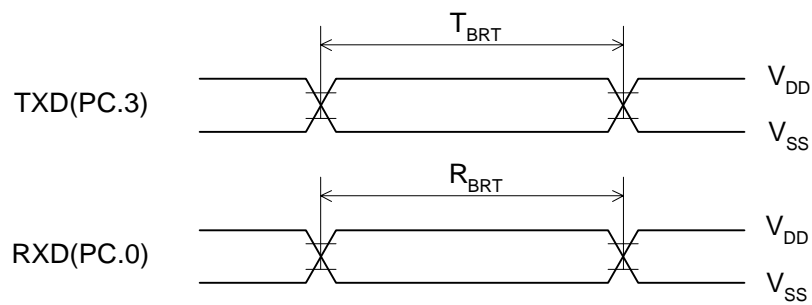
## UART Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit Baud Rate	$T_{BRT}$	$T_{BRT} = 1/f_{BRT}$ $T_{CR} = 1/f_{OSC}$	$T_{BRT} - T_{CR}$	$T_{BRT}$	$T_{BRT} + T_{CR}$	s
Receive Baud Rate	$R_{BRT}$	$R_{BRT} = 1/f_{BRT}$	$R_{BRT} \times 0.97$	$R_{BRT}$	$R_{BRT} \times 1.03$	s

$f_{BRT}$ : Baud rates (9600, 4800, 2400 and 1200bps)

## UART communication timing

("H" level = 1.2 V, "L" level = 0.3 V)



**AC Characteristics (RC Oscillation Type A/D Converter)**

(V<sub>DD</sub> = 1.5 V, V<sub>SS</sub> = 0 V, Ta = -20 to +70°C unless otherwise specified)

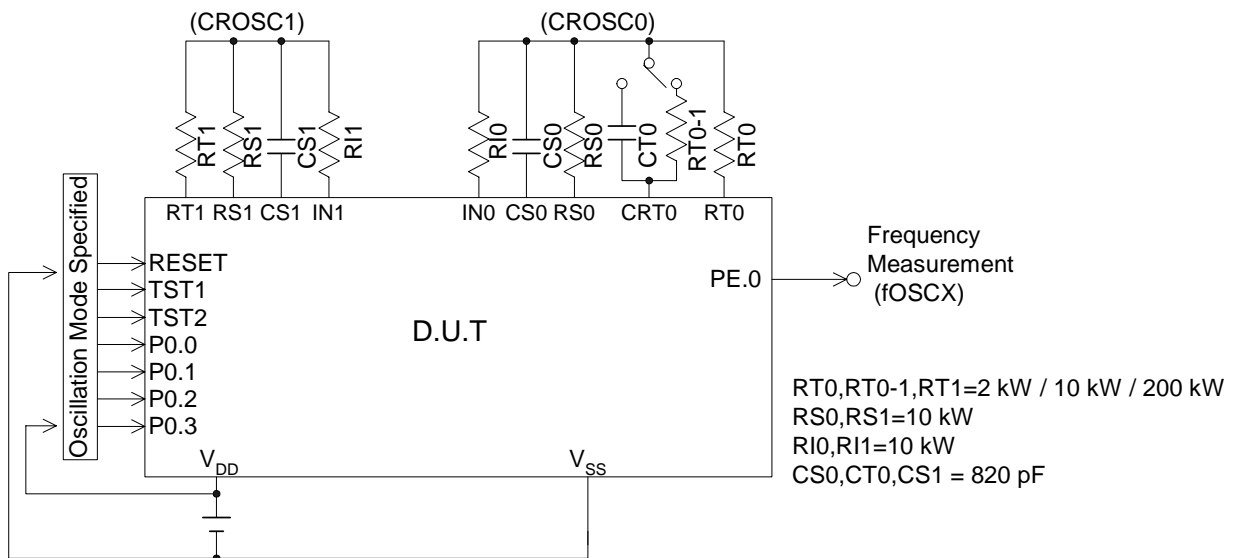
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Resistor for Oscillation	RS0, RS1, RT0, RT0-1, RT1	CS0, CT0, CS1 ≥ 740 pF	1	—	—	kΩ	5
Input Current Limiting Resistor	RI0, RI1	—	1	10	—	kΩ	
Oscillation Frequency	f <sub>osc1</sub>	Resistor for Oscillation = 2 kΩ	180	220	260	kHz	
	f <sub>osc2</sub>	Resistor for Oscillation = 10 kΩ	41.0	50.0	59.0	kHz	
	f <sub>osc3</sub>	Resistor for Oscillation = 200 kΩ	2.30	2.80	3.30	kHz	
RS•RT Oscillation Frequency Ratio (*)	Kf1	RT0, RT0-1, RT1 = 2 kΩ	3.9	4.2	4.5	—	
	Kf2	RT0, RT0-1, RT1 = 10 kΩ	0.990	1.0	1.010	—	
	Kf3	RT0, RT0-1, RT1 = 200 kΩ	0.053	0.057	0.061	—	

Kfx is the ratio of the oscillation frequency by a sensor resistor to the oscillation frequency by a reference resistor in the same condition.

$$Kfx = \frac{f_{oscx} (RT0 - CS0 \text{ Oscillation})}{f_{oscx} (RS0 - CS0 \text{ Oscillation})}, \quad \frac{f_{oscx} (RT0-1 - CS0 \text{ Oscillation})}{f_{oscx} (RS0 - CS0 \text{ Oscillation})}, \quad \frac{f_{oscx} (RT1 - CS1 \text{ Oscillation})}{f_{oscx} (RS1 - CS1 \text{ Oscillation})}$$

(x = 1, 2, 3)

**Measuring circuit 5**



**REVISION HISTORY**

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL63611A-01	Jan 28. 2004	-	-	Final edition 1



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