FEDL66525-02
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OKI Semiconductor

ML66525 Family

16-Bit Microcontroller

GENERAL DESCRIPTION

The ML66525 family devices are high-performance 16-bit CMOS microcontrollers that utilize the nX-8/500S, Oki's proprietary CPU core.

Data from a personal computer with a USB connector can be automatically, quickly written or read to and from NAND type Flash Memory via USB I/F and NAND Flash Memory I/F.

The ML66525 family devices support clock gear functions, a sub-clock and HALT/STOP mode, which are suitable for low power applications.
The ML66525 family devices are provided with interfaces to external devices such as a 4-channel multi-functional serial interface with internal 32-byte FIFO and a high-speed bus interface that has separate address and data buses and does not require external address latches.
A wide variety of internal multi-functional timers enable various timing controls such as periodic and timed measurements.

With a 16-bit CPU core that enables high-speed arithmetic computations and a variety of bit processing functions, these general-purpose microcontrollers are optimally suited for Digital Audio devices such as MP3 players, voice recorders, handy games, and PC peripheral control systems (to control devices that can be connected to USB and store data into memory).

The ML66525 family devices also include the flash ROM version device (ML66Q525B) that is programmable with a single 3 V power supply (2.4 to 3.6 V).

[Note] ML66525A/ML66Q525A are supplied as stock lasts.

APPLICATIONS

- Small-sized handy systems that require USB control and Storage control (Digital Audio players, etc)
- PC Peripheral Control Systems

ORDERING INFORMATION

Order Code or Product Name	Package	Remark
ML66525B-xxTB *1	100-pin plastic TQFP (TQFP100-P-1414-0.50-K)	mask ROM version (2.4 to 3.6 V)
ML66Q525B-NTB *2		ML66525B flash ROM version (2.4 to 3.6 V)
ML66525B-xxLA *1	144-pin plastic LFBGA (P-LFBGA144-1111-0.80)	ML66525B BGA package version (2.4 to 3.6 V)
ML66Q525B-NLA *2		ML66Q525B BGA package version (2.4 to 3.6 V)

*1 : The "xx" of "-xx" stands for the code number.
*2 : The "N" of "-N" stands for the flash ROM blank version.
When OKI programs and ship the flash ROM, the part number is changed from "–N" to "–XX" (code number) , for example, ML66Q525B-999TB.

FEATURES

Parameter	ML66525B
Operating temperature	–30 to +70°C
Power supply voltage/ Maximum operating frequency	V_{DD} = 2.4 to 3.6 V / f = 24 MHz
Minimum instruction execution time	83 nsec@24 MHz
	61 μsec@32.768 kHz
Internal ROM size (max. external)	128 KB (1 MB)
Internal RAM size (max. external)	6 KB (1 MB)
I/O ports	64 I/O pins (with programmable pull-up resistors)
	6 input-only pins
	1 output-only pin
Timers	16-bit auto-reload timer × 2ch
	8-bit auto-reload timer × 1ch
	8-bit auto-reload timer
	8-bit auto-reload timer (also functions as watchdog timer) × 1ch
	Watch timer × 1ch
	8-bit PWM × 2ch (can also be used as 16-bit PWM × 1ch)
Serial port	Synchronous (with 32-byte FIFO) × 1ch
	Synchronous (Shift register type) × 1ch
	Synchronous/UART × 2ch
A/D converter	10-bit × 4ch
External interrupts	Non-maskable × 1ch
	Maskable × 6ch
USB control	Compliant with USB spec. version 1.1
	High-speed transfer at 12 Mbps
	Internal PLL(x2 , x3 , x4) -> 48 MHz
	Internal transceiver
	Vbus detection circuit (connection to USB host : detect/non-detect)
	Bus power available
	EP0 (IN 32 bytes, OUT 32 bytes), control transfer
	EP1 (64 bytes × 2), bulk/interrupt transfer
	EP2 (64 bytes × 2), bulk/interrupt transfer
	EP3 (32 bytes), bulk/interrupt transfer
	EP4 (64 bytes × 2), bulk/isochronous/interrupt transfer
	EP5 (64 bytes × 2), bulk/isochronous/interrupt transfer
	Automatic, high-speed data transfer
NAND Flash Memory control	ECC circuit
	Automatic, high-speed 512-byte data transfer
Interrupt priority	3 levels
Others	External bus Interface (separate address and data buses)
	Dual clocks function
	Clock gear function
	Different power available among USB, CPU core, and I/O port
Flash ROM version	ML66Q525B

FUNCTIONAL DESCRIPTION

1. **High-performance CPU**
   The ML66525 family devices include the high-performance CPU, powerful bit manipulation instruction set, a variety of symmetrical addressing modes, and ROM WINDOW function, and also supports the best-optimized C compiler.

2. **A variety of power saving modes**
   Attaching a 32.768-kHz crystal produces a real time clock signal from the internal clock timer. A single clock can be used in place of dual clocks.
   Switching the CPU clock to the dual clocks (1/2 or 1/4 of the main clock) enables operation in a low power consumption mode. The clock gear function allows a 1/2 or 1/4 clock signal of the main clock to be selected as the CPU operating clock.
   The ML66525 family devices are provided with a wide range of standby control functions such as the STOP mode that stops the oscillation circuit, the quick restart STOP mode that stops the CPU and peripherals while the oscillation circuit is operating, and the HALT mode that shuts down the CPU while peripherals are operating.

3. **USB control**
   The family include USB controller which compliant with USB specification version 1.1 and can be transferred data with 12Mbps circuit.
   Also, USB controller have 6 kinds of endpoint and apply for control/bulk/isochronous/interrupt transfer.
   With NAND Flash Memory control circuit, high speed data transfer is possible.

4. **NAND Flash Memory control**
   The family include control circuit of NAND Flash Memory. Automatically data read from and write to outside NAND Flash Memory with 528 byte.
   Also, include ECC circuit which detect data error and correct data error.

5. **ML66Q525B with flash memory programmable with single power supply**
   In addition to mask ROM version devices, the ML66525 family devices include the ML66Q525B with internal 128 Kbytes of flash memory that can be programmed with a single power supply. The flash memory of the ML66Q525B can be programmed with a low power supply (2.4 to 3.6 V) using the internal voltage booster circuit.

6. **Multifunctional, high-precision analog-to-digital converter**
   The family devices include a high-precision 10-bit analog-to-digital converter with four channels and are ideal for such analog control functions as processing audio signals, processing sensor inputs, detecting key switch states, and controlling battery use in portable equipment. Each channel has its own result register readily accessible from the software.

7. Multifunctional PWM

The family devices support both 8- and 16-bit PWM operations. Choosing between the time base counter output and the overflow from an 8-bit auto-reload time as the PWM counter clock source provides a great number of possibilities over a broad frequency range. The 16-bit PWM configuration supports a high-speed synchronization mode that generates a high-precision output signal with less ripple suitable for digital-to-analog applications.

8. Programmable pull-up resistors

Building the pull-up resistors into the chip contributes overall design compactness.
Making them programmable on a per-bit basis allows complete flexibility in circuit board layout and system design. These programmable pull-up resistors are available for all I/O pins except ports that have specific functions such as oscillator connection pins.

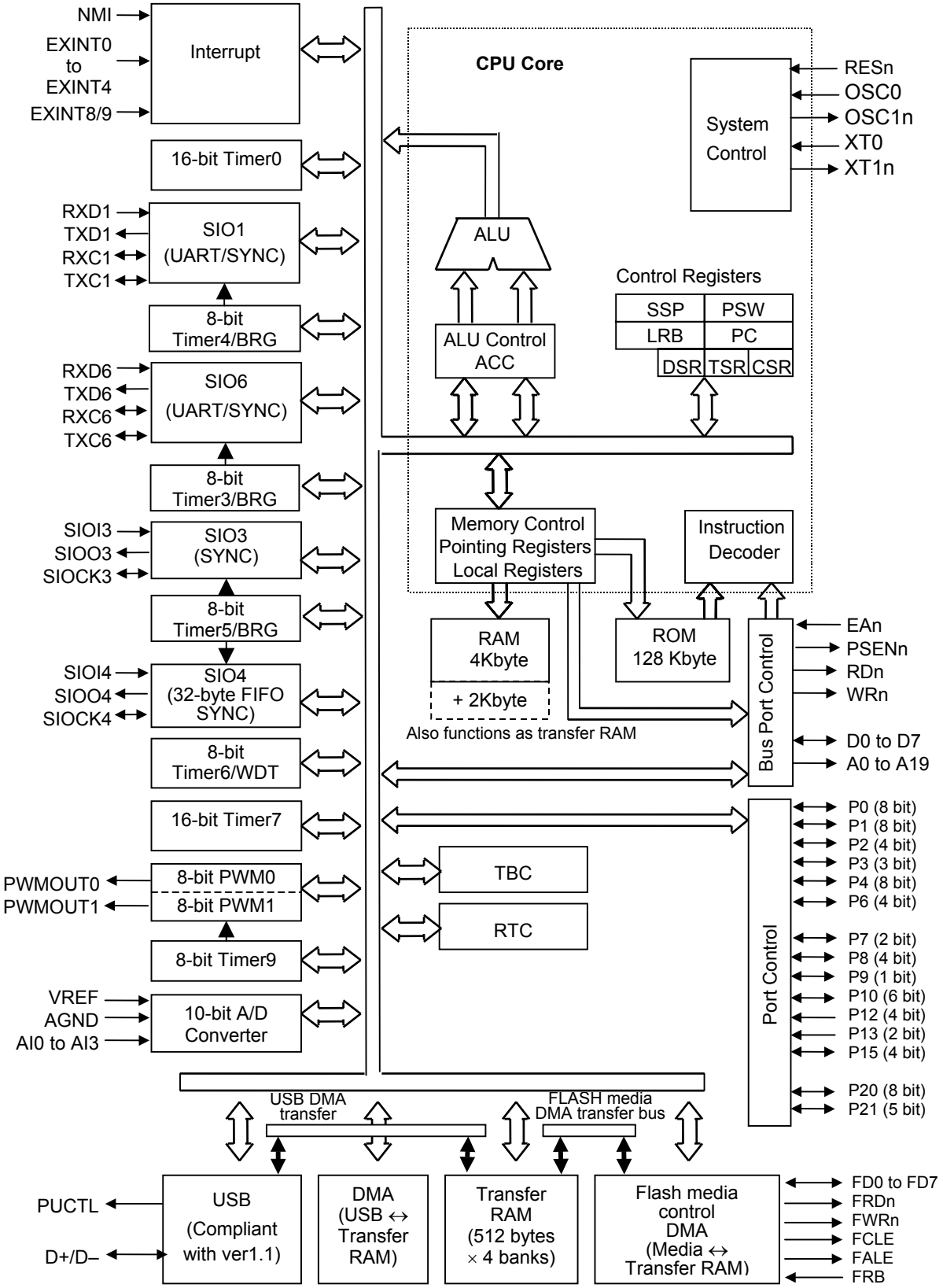
9. High-speed bus interface

The interface to external devices uses separate data and address buses.
This arrangement permits a rapid bus access for controlling the system from the microcontroller.

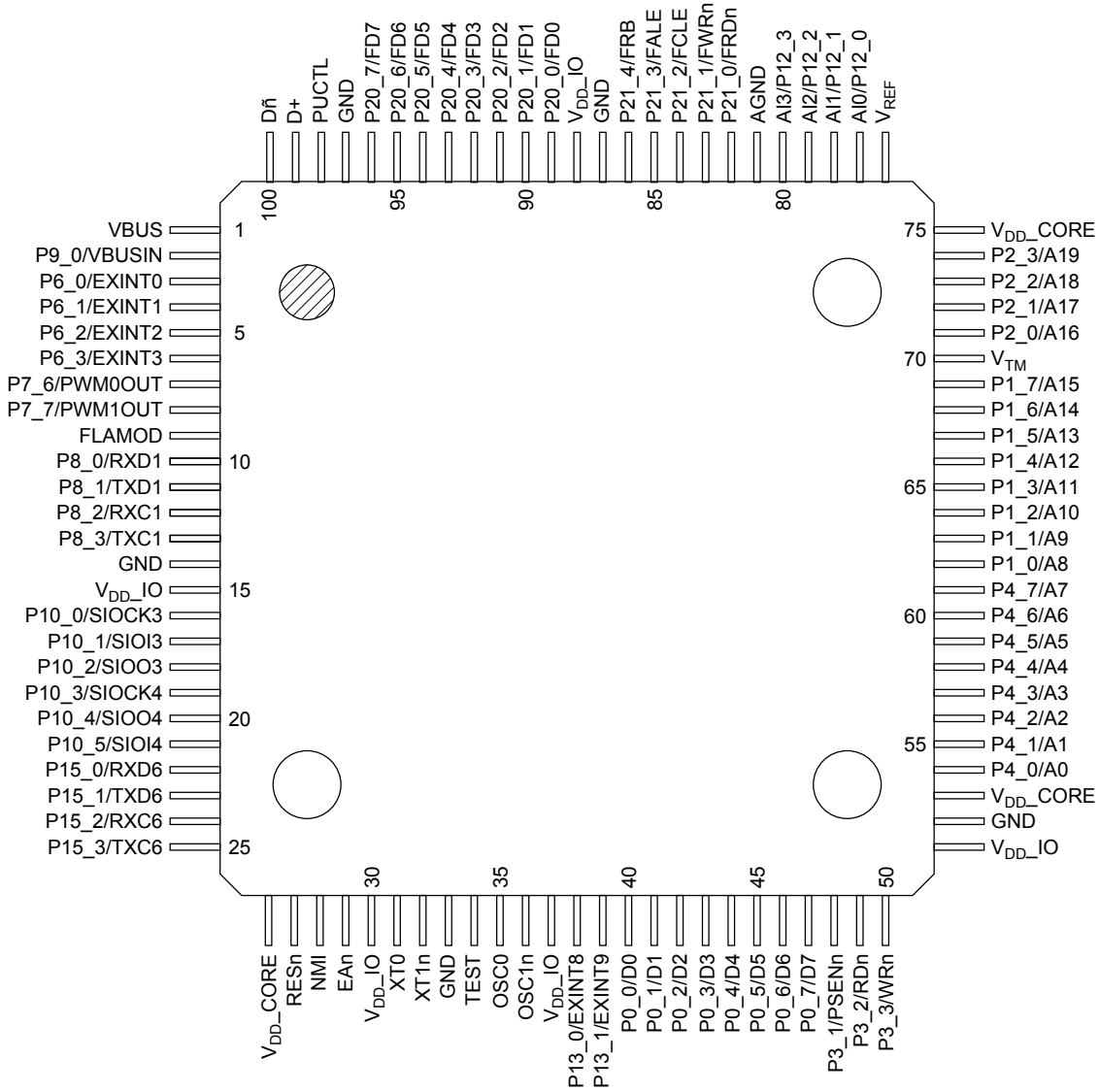
10. A variety of external interrupts

There are a total of seven interrupt channels for use in communicating with external devices; six channels for maskable interrupts and one channel for non-maskable interrupts.

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



100-pin Plastic TQFP

A symbol with “n” suffixed indicates an active Low pin.

PIN CONFIGURATION (TOP VIEW)

NC	V_{DD}_IO	P3_2/ RDn	NC	P0_5/ D5	P0_3/ D3	P13_1/ EXINT9	OSC0	GND	XT0	NMI	V_{DD}_ CORE	NC	N
GND	P3_3/ WRn	P3_1/ PSENn	P0_4/ D4	P0_2/ D2	P0_1/ D1	V_{DD}_IO	OSC1n	TEST	XT1n	V_{DD}_IO	P15.2/ RXC6	P15_3/ TXC6	M
P4_0/ A0	NC	V_{DD}_ CORE	P0_7/ D7	P0_6/ D6	P0_0/ D0	P13_0/ EXINT8	NC	NC	EAn	RESn	P15_0/ RXD6	P15_1/ TXD6	L
P4_2/ A2	NC	P4_1/ A1	NC	NC	NC	NC	NC	NC	NC	P10_4/ SIOO4	P10_2/ SIOO3	P10_5/ SIOI4	K
P4_4/ A4	P4_5/ A5	P4_3/ A3	NC						NC	P10_3/ SIOCK4	NC	NC	J
P4_6/ A6	P4_7/ A7	P1_0/ A8	NC						NC	V_{DD}_IO	P10_0/ SIOCK3	P10_1/ SIOI3	H
NC	P1_1/ A9	P1_2/ A10	NC						NC	P8_3/ TXC1	P8_2/ RXC1	GND	G
P1_5/ A13	P1_4/ A12	P1_3/ A11	NC						NC	P8_1/ TXD1	P8_0/ RXD1	NC	F
NC	NC	P1_7/ A15	NC						NC	P7_6/ PWM0OUT	FLAMOD	P7_7/ PWM1OUT	E
NC	P1_6/ A14	V_{TM}	NC	NC	NC	NC	NC	NC	NC	P6_2/ EXINT2	NC	P6_3/ EXINT3	D
P2_1/ A17	P2_0/ A16	V_{REF}	P12_1/ AI1	P12_3/ AI3	P21_4/ FRB	V_{DD}_IO	P20_1/ FD1	P20_7/ FD7	NC	P6_0/ EXINT0	NC	P6_1/ EXINT1	C
P2_3/ A19	P2_2/ A18	NC	AGND	P21_1/ FWRn	P21_3/ FALE	GND	P20_2/ FD2	P20_3/ FD3	P20_5/ FD5	PUCTL	D-	P9_0/ VBUSIN	B
NC	V_{DD}_ CORE	P12_0/ AI0	P12_2/ AI2	P21_0/ FRDn	P21_2 /FCLE	P20_0 /FD0	P20_4/ FD4	P20_6/ FD6	GND	D+	VBUS	NC	A
13	12	11	10	9	8	7	6	5	4	3	2	1	

144-pin Plastic LFBGA

A symbol with “n” suffixed indicates an active Low pin.

[Note] Don’t connect NC pins with others.

PIN DESCRIPTIONS

In the Type column, "I" indicates an input pin, "O" indicates an output pin, and "I/O" indicates an I/O pin.
A symbol with "n" suffixed indicates an active Low pin.

Classification	Symbol	Description			
		Type	Primary function	Type	Secondary function
Port	P0_0/D0 to P0_7/D7	I/O	8-bit I/O port Pull-up resistors can be specified for each bit.	I/O	External memory access data I/O port
	P1_0/A8 to P1_7/A15	I/O	8-bit I/O port Pull-up resistors can be specified for each bit.	O	External memory access address output port
	P2_0/A16 to P2_3/A19	I/O	4-bit I/O port Pull-up resistors can be specified for each bit.	O	External memory access address output port
	P3_1/PSENn	I/O	1-bit I/O port Pull-up resistors can be specified.	O	External program memory access read strobe output pin
	P3_2/RDn	O	1-bit output port	O	External data memory access read strobe output pin
	P3_3/WRn	I/O	1-bit I/O port Pull-up resistors can be specified.	O	External data memory access write strobe output pin
	P4_0/A0 to P4_7/A7	I/O	8-bit I/O port Pull-up resistors can be specified for each bit.	O	External memory access address output port
	P6_0/EXINT0	I/O	4-bit I/O port Pull-up resistors can be specified for each bit.	I	External interrupt 0 input pin
	P6_1/EXINT1			I	External interrupt 1 input pin
	P6_2/EXINT2			I	External interrupt 2 input pin
	P6_3/EXINT3			I	External interrupt 3 input pin
	P7_6/PWM0OUT	I/O	2-bit I/O port Pull-up resistors can be specified for each bit.	O	PWM0 output pin
	P7_7/PWM1OUT			O	PWM1 output pin
	P8_0/RXD1	I/O	4-bit I/O port Pull-up resistors can be specified for each bit.	I	SIO1 receive data input pin
	P8_1/TXD1			O	SIO1 transmit data output pin
	P8_2/RXC1			I/O	SIO1 receive clock I/O pin
	P8_3/TXC1			I/O	SIO1 transmit clock I/O pin

Classification	Symbol	Description			
		Type	Primary function	Type	Secondary function
Port	P9_0/VBUSIN	I/O	1-bit I/O port Pull-up resistors can be specified.	I	Vbus detect external interrupt input pin (5V tolerant input)
	P10_0/SIOCK3	I/O	6-bit I/O port Pull-up resistors can be specified for each bit.	I/O	SIO3 transmit-receive clock I/O pin
	P10_1/SIOI3			I	SIO3 receive data input pin
	P10_2/SIOO3			O	SIO3 transmit data input pin
	P10_3/SIOCK4			I/O	SIO4 (with internal 32-byte FIFO) transmit-receive clock I/O pin
	P10_4/SIOO4			O	SIO4 (with internal 32-byte FIFO) transmit data output pin
	P10_5/SIOI4			I	SIO4 (with internal 32-byte FIFO) receive data output pin
	P12_0/AI0 to P12_3/AI3	I	4-bit input port	I	A/D converter analog input port
	P13_0/EXINT8	I	2-bit input port	I	External interrupt 8 input pin
	P13_1/EXINT9			I	External interrupt 9 input pin
	P15_0/RXD6	I/O	4-bit I/O port Pull-up resistors can be specified for each bit.	I	SIO6 receive data input pin
	P15_1/TXD6			O	SIO6 transmit data output pin
	P15_2/RXC6			I/O	SIO6 receive clock I/O pin
	P15_3/TXC6			I/O	SIO6 transmit clock I/O pin
	P20_0/FD0 to P20_7/FD7	I/O	8-bit I/O port Pull-up resistors can be specified for each bit.	I/O	NAND Flash Memory access data I/O port
	P21_0/FRDn	I/O	5-bit I/O port Pull-up resistors can be specified for each bit.	O	NAND Flash Memory access read strobe output pin
	P21_1/FWRn	I/O		O	NAND Flash Memory access write strobe output pin
	P21_2/FCLE	I/O		O	NAND Flash Memory access CLE strobe output pin
	P21_3/FALE	I/O		O	NAND Flash Memory access ALE strobe output pin
	P21_4/FRB	I/O		I	NAND Flash Memory access Ready/Busy input pin

Classification	Symbol	Type	Description
Power supply	V_{DD}_IO	I	IO Power supply pin Connect all the V_{DD} _IO pins.*
	V_{DD}_CORE	I	Core Power supply pin Connect all the V_{DD} _CORE pins.*
	VBUS	I	USB Power supply pin (Vbus input pin)
	GND	I	GND pin Connect all the GND pins to GND.*
	V_{REF}	I	Analog reference voltage pin (Connect to the V_{DD} pin when A/D converter is not used.)
	AGND	I	Analog GND pin (Connect to the GND pin when A/D converter is not used.)
Oscillation	XT0	I	Sub-clock oscillation input pin Connect to a crystal of f = 32.768 kHz.
	XT1n	O	Sub-clock oscillation output pin Connect to a crystal of f = 32.768 kHz. The clock output is opposite in phase to XT0.
	OSC0	I	Main clock oscillation input pin Connect to a crystal or ceramic oscillator. When an external clock is used, this pin is configured to be clock input.
	OSC1n	O	Main clock oscillation output pin Connect to a crystal or ceramic oscillator. The clock output is opposite in phase to OSC0. Leave this pin unconnected when an external clock is used.
USB I/F	D+	I/O	D+ pin
	D–	I/O	D– pin
	PUCTL	O	External control output pin
Reset	RESn	I	Reset input pin
Others	NMI	I	Non-maskable interrupt input pin
	TEST	I	Test pin Connect to the GND pin for normal operation.
	V_{TM}	I	Test pin Connect to the GND pin for normal operation.
	FLAMOD	I	Flash ROM programming mode input pin When the FLAMOD pin is set to “L”, the device enters a programming mode. Connect to the V_{DD}_IO pin when using as normal operation.
	EAn	I	External program memory access input pin When the EA pin is enabled (low level), the internal program memory is masked and the CPU executes the program code in external program memory through all address space.

* Connect all V_{DD}_IO pins, all V_{DD}_CORE pins and all GND pins.
If a device has one or more V_{DD}_IO, V_{DD}_CORE, or GND pins to which the power supply or the ground potential is not connected, the family devices are not guaranteed to have normal operations.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition		Rated value	Unit
Digital power supply voltage	V_{DD}_CORE V_{DD}_IO VBUS	GND = AGND = 0 V Ta = 25°C		–0.3 to +4.6	V
Input voltage	V_I	Other than P9_0		–0.3 to V_{DD}_IO + 0.3	V
		P9_0 (5 V tolerant input)		–0.3 to +0.6	V
Output voltage	V_O			–0.3 to V_{DD}_IO + 0.3	V
Analog reference voltage	V_{REF}			–0.3 to +4.6	V
Analog input voltage	V_{AI}			–0.3 to V_{REF}	V
Power dissipation	P_D	Ta = 70°C per package	100-pin TQFP	680	mW
			144-pin LFBGA	595	mW
Storage temperature	T_{STG}	—		–50 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Range	Unit
Digital power supply voltage	V_{DD}_CORE V_{DD}_IO	$f_{OSC} \leq 24$ MHz V_{DD}_CORE ≤ V_{DD}_IO		2.4 to 3.6	V
Analog reference voltage	V_{REF}	V_{DD}_CORE ≤ V_{REF}		2.4 to 3.6	V
Analog input voltage	V_{AI}	—		AGND to V_{REF}	V
VBUS input voltage	VBUS	—		3.0 to 3.6	V
Memory hold voltage	V_{DDH}	f_{OSC} = 0 Hz		2.0 to 3.6	V
Operating frequency	f_{OSC}	USB is used		12, 16, 24	MHz
		USB is unused		2 to 24	
	f_{XT}	—		32.768	kHz
Ambient temperature	Ta	—		–30 to +70	°C
Fan out	N	MOS load		20	—
		TTL load	P7, P10_0 to P10_2	6	—
			P0, P1, P2, P3, P4, P6, P8, P9, P10_3 to P10_5, P15, P20, P21	1	—

ALLOWABLE OUTPUT CURRENT VALUES

(V_{DD}_IO = 2.4 to 3.6 V, Ta = –30 to +70°C)

Parameter	Pin	Symbol	Min.	Typ.	Max.	Unit
"H" output pin (1 pin)	All output pins	I_{OH}	—	—	–10	mA
"H" output pins (sum total)	Sum total of all output pins	$\sum I_{OH}$	—	—	–70	
"L" output pin (1 pin)	All output pins	I_{OL}	—	—	10	
"L" output pins (sum total)	Sum total of P0, P3	$\sum I_{OL}$	—	—	35	
	Sum total of P1, P2, P4					
	Sum total of P6, P7, P8, P9					
	Sum total of P10, P15					
	Sum total of P20, P21				70	
	Sum total of all output pins				160	

[Note] Connect all V_{DD}_CORE and V_{DD}_IO pins to the power supply voltage and all GND pins to the ground voltage. If there is a pin or pins that are not connected to the power supply voltage on ground voltage, the device cannot be guaranteed for normal operation.

INTERNAL FLASH ROM PROGRAMMING CONDITIONS

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}_CORE V_{DD}_IO	V_{DD}_CORE ≤ V_{DD}_IO	2.4 to 3.6	V
Ambient temperature	Ta	During Read	–30 to +70	°C
		During Programming	+0 to +50	°C
Endurance	CEP	—	100	Cycles
Blocks size	—	—	128	bytes

ELECTRICAL CHARACTERISTICS

DC Characteristics 1 (Except USB port)

(V_{DD}_CORE = V_{DD}_IO = V_{REF} = 2.4 to 3.6 V, GND = AGND = 0 V, Ta = –30 to +70°C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	*1	V_{IH}	—	0.80 V_{DD}	—	5.5	V
"H" input voltage				0.80 V_{DD}	—	V_{DD} + 0.3	
"L" input voltage		V_{IL}	—	–0.3	—	0.2V_{DD}	
"H" output voltage	*2	V_{OH}	I_O = –400 μA	V_{DD} – 0.4	—	—	
			I_O = –2.0 mA	V_{DD} – 0.8	—	—	
"H" output voltage	*3		I_O = –200 μA	V_{DD} – 0.4	—	—	
			I_O = –1.0 mA	V_{DD} – 0.8	—	—	
"L" output voltage	*2	V_{OL}	I_O = 3.2 mA	—	—	0.5	
			I_O = 5.0 mA	—	—	0.9	
"L" output voltage	*3		I_O = 1.6 mA	—	—	0.5	
			I_O = 2.5 mA	—	—	0.9	
Input leakage current	*4, *6	I_{IH}/I_{IL}	V_I = V_{DD}/0 V	—	—	1/–1	μA
Input current	*5			—	—	1/–90	
Input current	*7			—	—	15/–15	
Output leakage current	*2, *3	I_{LO}	V_O = V_{DD}/0 V	—	—	±10	μA
Pull-up resistance		R_{pull}	V_I = 0 V	40	100	200	kΩ
Input capacitance		C_I	f_{OSC} = 1 MHz, Ta = 25°C	—	5	—	pF
Output capacitance		C_O		—	7	—	
Analog reference supply current		I_{REF}	During A/D operation	—	1.8	5	mA
			When A/D is stopped	—	—	5	μA

V_{DD} = V_{DD}_IO

*1. Applicable to P9_0 (5 V tolerant input)
*2. Applicable to P7 and P10_0 to P10_2
*3. Applicable to P0, P1, P2, P3, P4, P6, P8, P9, P10_3 to P10_5, P15, P20 and P21
*4. Applicable to P12 and P13
*5. Applicable to RESn and FLAMOD
*6. Applicable to EAn, NMI, and TEST
*7. Applicable to OSC0

Supply Current

• Mask ROM version

(V_{DD}_CORE = V_{DD}_IO = V_{REF} = 2.4 to 3.6 V, VBUS = 3.0 to 3.6 V, GND = AGND = 0 V, Ta = –30 to +70°C)

Mode	Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable power supply
CPU operation mode	I_{DD}	fosc = 24 MHz, No load		—	28	60	mA	V_{DD}_CORE + V_{DD}_IO
		fosc = 24 MHz, DMA/media control stopped. No load			18	50		
		f_{XT} = 32.768 kHz, DMA/media control stopped. No load *1		—	100	300	μA	
USB operation mode	I_{BUS}	Setting of 48 MHz for multiplication selection. No Load		—	25	45	mA	VBUS
HALT mode	I_{DDH}	fosc = 24 MHz, DMA/media control stopped. No load		—	9	18	mA	V_{DD}_CORE + V_{DD}_IO
STOP mode	I_{DDS}	OSC is stopped *1	XT is used *2	—	15	160	μA	V_{DD}_CORE + V_{DD}_IO
			XT is not used *2	—	10	150		
Suspend current	I_{SUSP}	Suspend state OSC is stopped, XT is not used * 1		—	1	100	μA	VBUS

The values in the Typ. Column indicate reference values at 25°C and 3.0 V (The VBUS currents indicate values at 3.3 V).

*1: The temperature condition ranges from –30 to +50°C

*2: The ports used as inputs are at V_{DD}_IO or 0 V. Other ports are unloaded.

• Flash ROM version

(V_{DD}_CORE = V_{DD}_IO = V_{REF} = 2.4 to 3.6 V, VBUS = 3.0 to 3.6 V, GND = AGND = 0 V, Ta = –30 to +70°C)

Mode	Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable power supply
CPU operation mode	I_{DD}	fosc = 24 MHz, No load		—	28	60	mA	V_{DD}_CORE + V_{DD}_IO
		fosc = 24 MHz, DMA/media control stopped. No load			18	50		
		f_{XT} = 32.768 kHz, DMA/media control stopped. No load *1		—	100	300	μA	
USB operation mode	I_{BUS}	Setting of 48 MHz for multiplication selection No Load		—	25	45	mA	VBUS
HALT mode	I_{DDH}	fosc = 24 MHz, DMA/media control stopped. No load		—	10	20	mA	V_{DD}_CORE + V_{DD}_IO
STOP mode	I_{DDS}	OSC is stopped *1	XT is used *2	—	15	160	μA	V_{DD}_CORE + V_{DD}_IO
			XT is not used *2	—	10	150		
Suspend current	I_{SUSP}	Suspend state, D+/D– fixed OSC is stopped, XT is not used * 1		—	1	100	μA	VBUS

The values in the Typ. Column indicate reference values at 25°C and 3.0 V (The VBUS currents indicate values at 3.3 V).

*1: The temperature condition ranges from –30 to +50°C

*2: The ports used as inputs are at V_{DD}_IO or 0 V. Other ports are unloaded.

DC Characteristics 2 (USB port)

(VBUS = 3.0 to 3.6V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Differential input sensitivity	V_{DI}	|(D+) – (D–)|	0.2	—	—	V	D+, D–
Differential common mode range	V_{CM}	Includes VDI	0.8	—	2.5		
Single ended receiver threshold	V_{SE}		0.8	—	2.0		
"H" output voltage	V_{OH}	15 kΩ to GND	2.8	—	—	V	D+, D–
		I_{OH} = –100 μA	VBUS – 0.2	—	—	V	PUCTL
		IOH = –4 mA	2.4	—	—		
"L" output voltage	V_{OL}	1.5 kΩ to 3.6 V	—	—	0.3	V	D+, D–
Output leakage current	I_{LO}	V_O = VBUS/0 V	—	—	±10	μA	D+, D–
		V_O = VBUS/0 V	—	—	±10		PUCTL

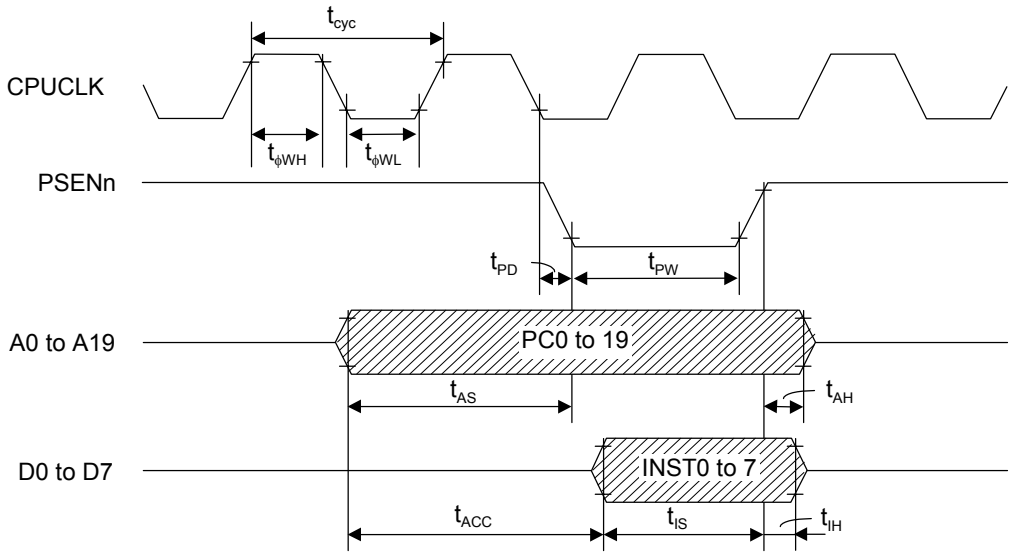
AC Characteristics (Except USB port)

(1) External program memory control

(V_{DD}_CORE = V_{DD}_IO = V_{REF} = 2.4 to 3.6 V, GND = AGND = 0 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 24 MHz	41.67	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	V_{DD}_CORE = C_L = 50 pF	16.25	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		16.25	—	
PSENn pulse width	t_{PW}		(2 + 2n)tϕ – 25	—	
PSENn pulse delay time	t_{PD}		—	55	
Address setup time	t_{AS}		2tϕ – 25	—	
Address hold time	t_{AH}		–10	—	
Instruction setup time	t_{IS}		40	—	
Instruction hold time	t_{IH}		0	—	
Read data access time	t_{ACC}		—	(3 + 2n)tϕ – 50	

(Note) tϕ = t_{cyc}/2
n = 0 to 3 (n wait cycles inserted)



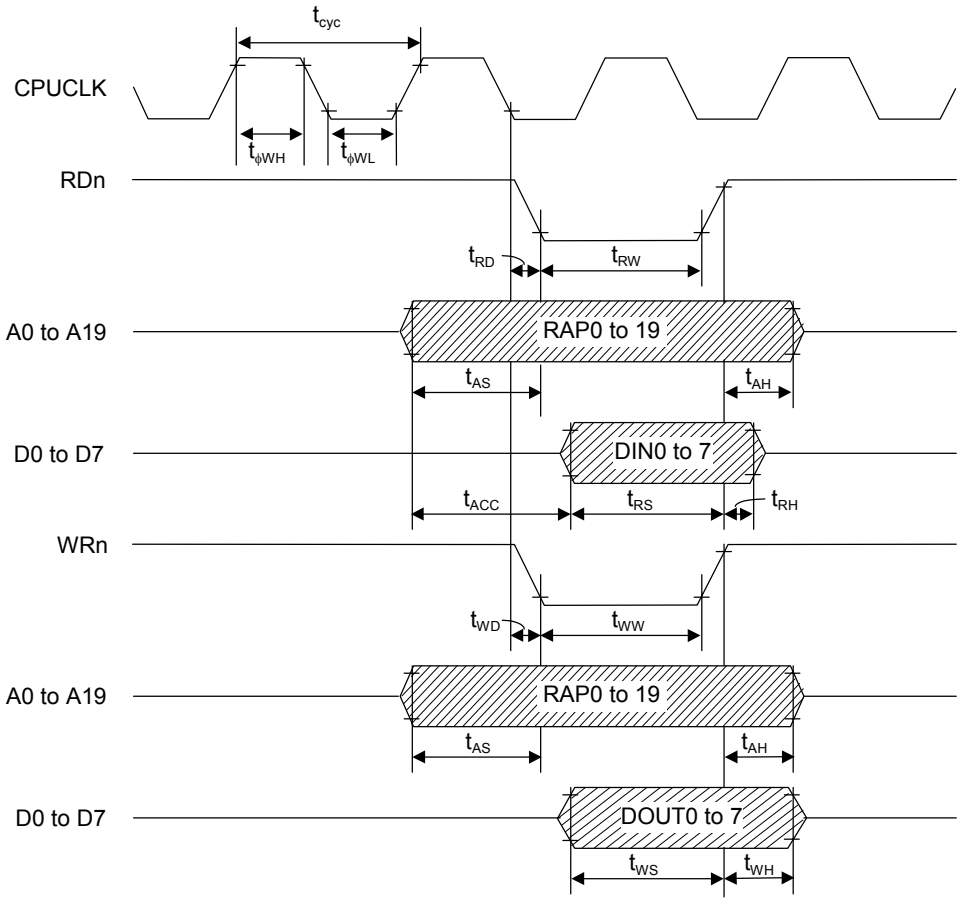
Bus timing during no wait cycle time

(2) External data memory control

(V_{DD}_CORE = V_{DD}_IO = V_{REF} = 2.4 to 3.6 V, GND = AGND = 0 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 24 MHz	41.67	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	16.25	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		16.25	—	
RDn pulse width	t_{RW}		(2 + 2n)tϕ – 25	—	
WRn pulse width	t_{WW}		(2 + 2n)tϕ – 25	—	
RDn pulse delay time	t_{RD}		—	55	
WRn pulse delay time	t_{WD}		—	55	
Address setup time	t_{AS}		tϕ – 20	—	
Address hold time	t_{AH}		tϕ – 20	—	
Read data setup time	t_{RS}		40	—	
Read data hold time	t_{RH}		0	—	
Read data access time	t_{ACC}		—	(3 + 2n)tϕ – 50	
Write data setup time	t_{WS}		2tϕ – 30	—	
Write data hold time	t_{WH}		tϕ – 6	—	

(Note) tϕ = t_{cyc}/2
n = 0 to 7 (n wait cycles inserted)



Bus timing during no wait cycle time

(3) Serial port control

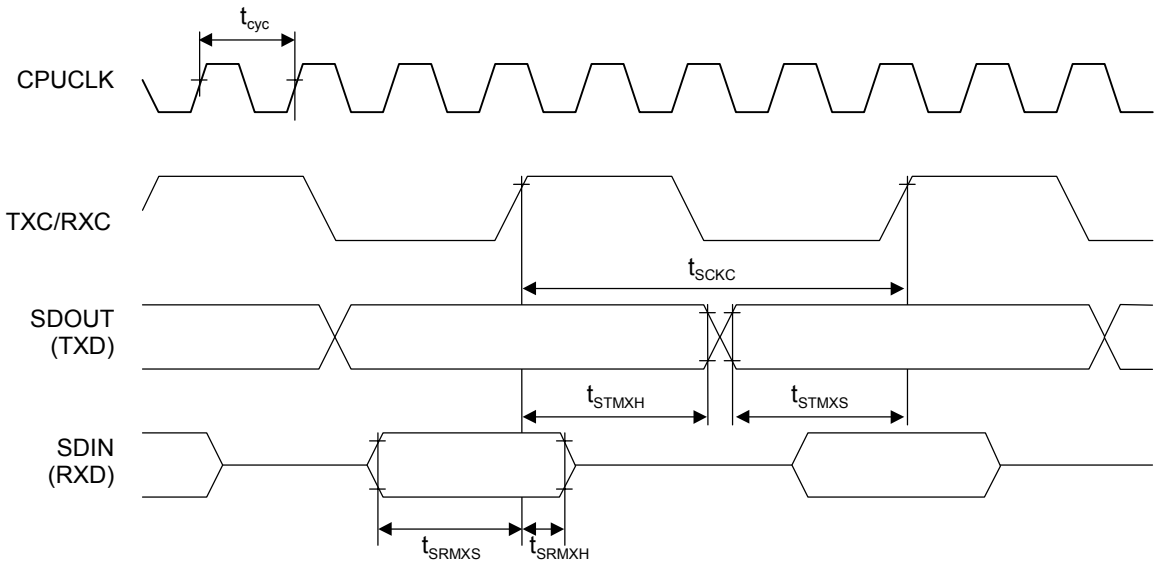
1. Serial port 1, 6 (SIO1, 6)

Master mode (Clock synchronous serial port)

(V_{DD}_CORE = V_{DD}_IO = V_{REF} = 2.4 to 3.6 V, GND = AGND = 0 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 24 MHz	41.67	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	4 t_{cyc}	—	
Output data setup time	t_{STMXS}		2tϕ – 10	—	
Output data hold time	t_{STMXH}		5tϕ – 20	—	
Input data setup time	t_{SRMXS}		21	—	
Input data hold time	t_{SRMXH}		0	—	

(Note) tϕ = t_{cyc}/2

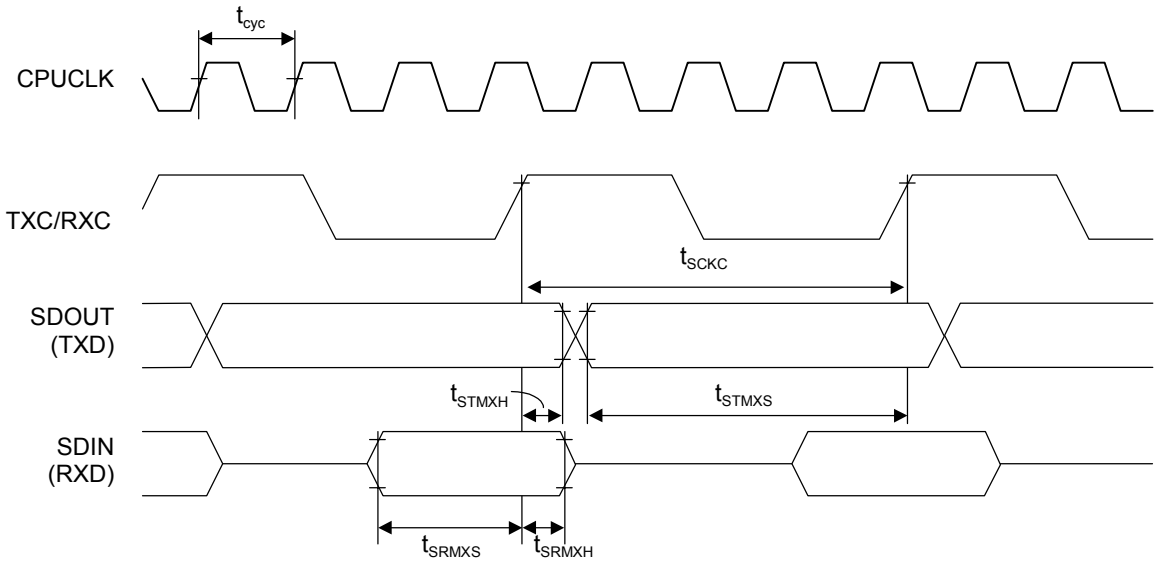


Slave mode (Clock synchronous serial port)

(V_{DD}_CORE = V_{DD}_IO = V_{REF} = 2.4 to 3.6 V, GND = AGND = 0 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 24 MHz	41.67	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	$4t_{cyc}$	—	
Output data setup time	t_{STMXS}		$2t\phi - 30$	—	
Output data hold time	t_{STMXH}		$4t\phi - 20$	—	
Input data setup time	t_{SRMXS}		21	—	
Input data hold time	t_{SRMXH}		7	—	

(Note) $t\phi = t_{cyc}/2$

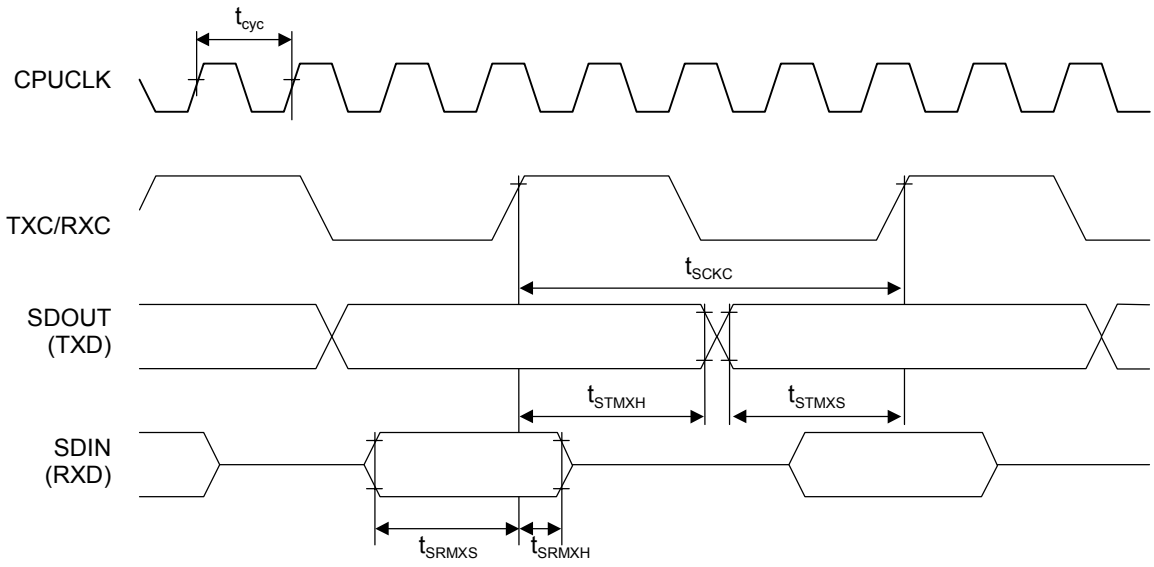


2. Serial port 4 (SIO4)

Master mode (Clock synchronous serial port)

(V_{DD}_CORE = V_{DD}_IO = V_{REF} = 2.4 to 3.6 V, GND = AGND = 0 V, Ta = –30 to +70°C)

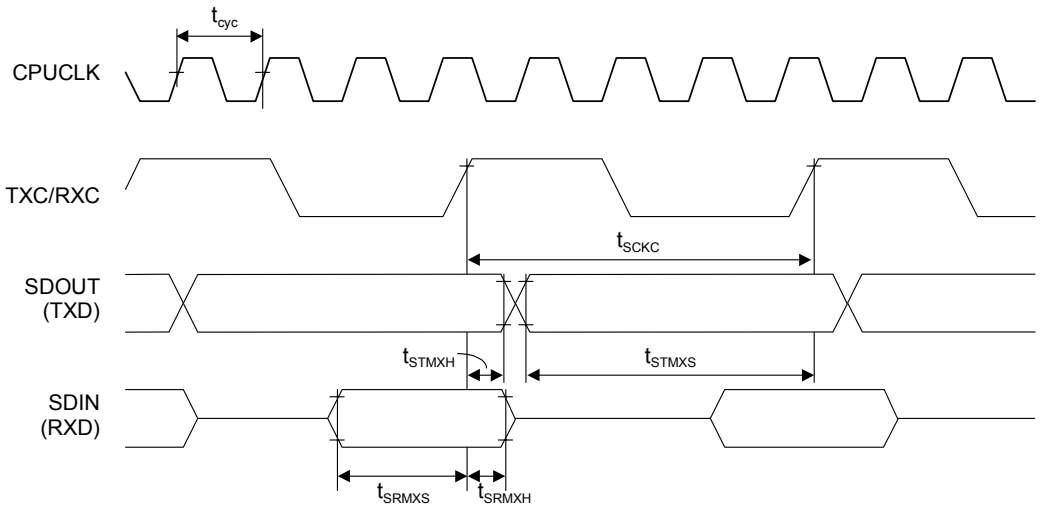
Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 24 MHz	41.67	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	400	—	
Output data setup time	t_{STMXS}		190	—	
Output data hold time	t_{STMXH}		130	—	
Input data setup time	t_{SRMXS}		21	—	
Input data hold time	t_{SRMXH}		0	—	



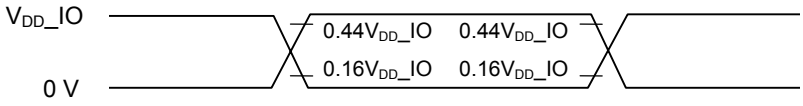
Slave mode (Clock synchronous serial port)

(V_{DD}_CORE = V_{DD}_IO = V_{REF} = 2.4 to 3.6 V, GND = AGND = 0 V, Ta = –30 to +70°C)

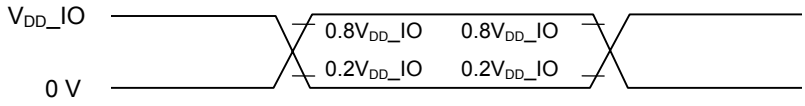
Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 24 MHz	41.67	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	400	—	
Output data setup time	t_{STMXS}		70	—	
Output data hold time	t_{STMXH}		180	—	
Input data setup time	t_{SRMXS}		21	—	
Input data hold time	t_{SRMXH}		7	—	



Measurement points for AC timing (except the serial port)



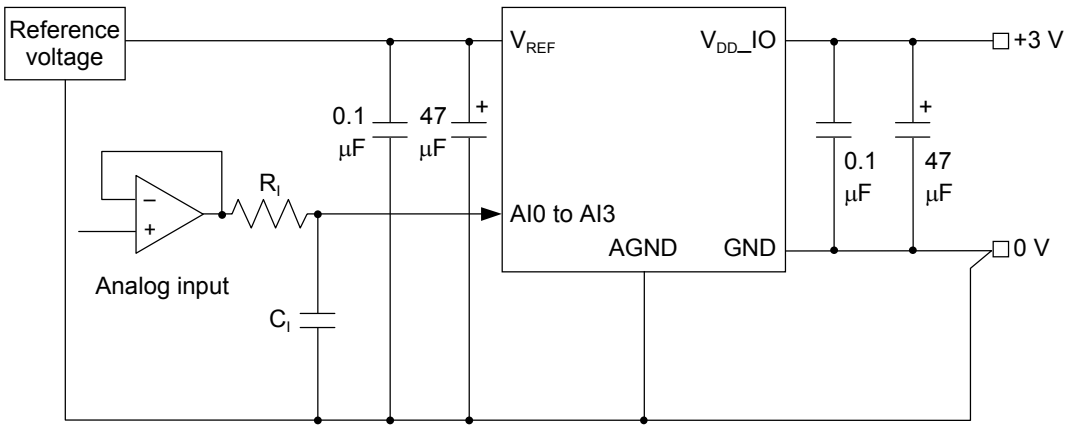
Measurement points for AC timing (the serial port)



A/D Converter Characteristics

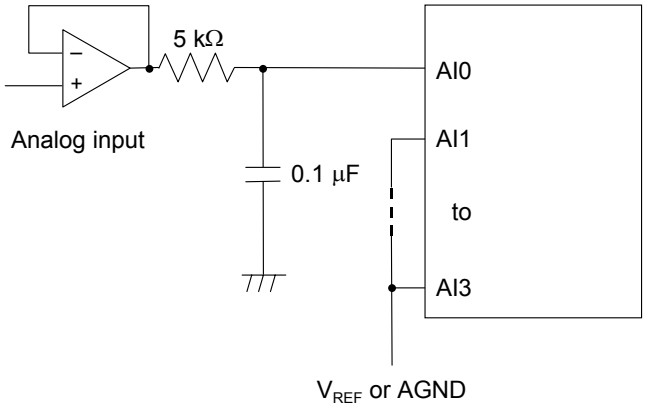
(Ta = –30 to +70°C, V_{REF} = 2.4 to 3.6 V, AGND = GND = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to measurement circuit 1 Analog input source impedance $R_I \leq 5\ k\Omega$	—	10	—	Bit
Linearity error	E_L		—	—	±3	LSB
Differential Linearity error	E_D		—	—	±2	
Zero scale error	E_{ZS}		—	—	+3	
Full-scale error	E_{FS}		—	—	–3	
Cross talk	E_{CT}	Refer to measurement circuit 2	—	—	±1	
Conversion time	t_{CONV}	Set according to ADTM set data	16	—	3906.3	µs/ch



R_I (impedance of analog input source) ≤ 5 kΩ
C_I ≅ 0.1 µF

Measurement Circuit 1



Cross talk is the difference between the A/D conversion results when the same analog input is applied to AI0 through AI3 and the A/D conversion results of the circuit to the left.

Measurement Circuit 2

Definition of Terminology

1. Resolution
   Resolution is the value of minimum discernible analog input.
   With 10 bits, since $2^{10} = 1024$, resolution of $(V_{REF} - AGND) \div 1024$ is possible.

2. Linearity error
   Linearity error is the difference between ideal conversion characteristics and actual conversion characteristics of a 10-bit A/D converter (not including quantization error).
   Ideal conversion characteristics can be obtained by dividing the voltage between V_{REF} and AGND into 1024 equal steps.

3. Differential linearity error
   Differential linearity error indicates the smoothness of conversion characteristics. Ideally, the range of analog input voltage that corresponds to 1 converted bit of digital output is $1LSB = (V_{REF} - AGND) \div 1024$. Differential error is the difference between this ideal bit size and bit size of an arbitrary point in the conversion range.

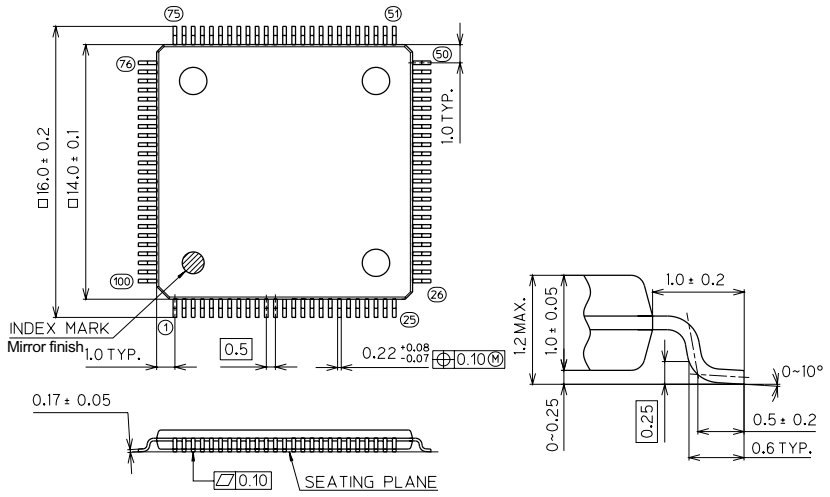
4. Zero scale error
   Zero scale error is the difference between ideal conversion characteristics and actual conversion characteristics at the point where the digital output changes from 000H to 001H.

5. Full-scale error
   Full-scale error is the difference between ideal conversion characteristics and actual conversion characteristics at the point where the digital output changes from 3FEH to 3FFH.

PACKAGE DIMENSIONS

(Unit: mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

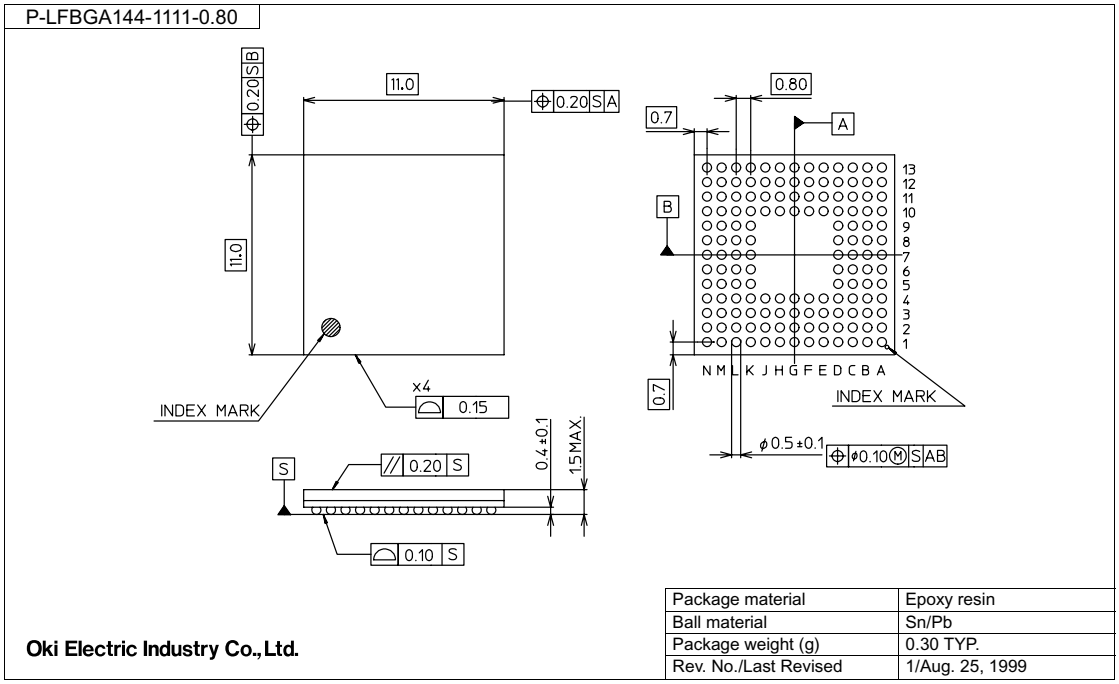
Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Packages

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

PACKAGE DIMENSIONS

(Unit: mm)



Package material	Epoxy resin
Ball material	Sn/Pb
Package weight (g)	0.30 TYP.
Rev. No./Last Revised	1/Aug. 25, 1999

Notes for Mounting the Surface Mount Type Packages

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REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL66525-01	Oct. 2000	–	–	Preliminary edition 1
PEDL66525-02	Mar. 2001	–	–	- Modified contents of P3_2 and P3_3 in the table on Page 8. - Added contents of P9_0 in the table on Page 9. - Modified contents of PUCTL in the table on Page 10. - Partially added contents of “ABSOLUTE MAXIMUM RATINGS”. - Partially added contents of “RECOMMENDED OPERATING CONDITIONS”. - Partially added contents of “ALLOWABLE OUTPUT CURRENT VALUES”. - Partially added contents of “INTERNAL FLASH ROM PROGRAMMING CONDITIONS”. - Partially added contents of “ELECTRICAL CHARACTERISTICS”.
FEDL66525-01	Oct. 2001	–	–	- Changed the name from ML66525 to ML66525A. - Changed the name from ML66Q525 to ML66Q525A. - Modified supply current values for ML66Q525 on Page 14. - Modified contents of the table on Page 21.
FEDL66525-02	Jul. 19, 2002	–	–	- Changed the name from ML66525A to ML66525B. - Changed the name from ML66Q525A to ML66Q525B.

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