System Reset (with watchdog timer+battery back-up)
Monolithic IC MM1106

Outline

This IC combines the popular watchdog timer with a battery back-up, resulting in an IC that is easier to use. The watchdog timer has a built-in power ON reset function, and both the timer and the battery back-up section have low current consumption.

Features

1. Low current consumption — 270μA typ.
2. Watchdog timer
   - Detection voltage — 4.2V typ.
   - C_T charging current — −0.24μA typ.
3. CS
   - CS detection voltage — 4.4V typ.
   - Output voltage low level — 0.1V typ.
4. Battery back-up
   - Power supply switching voltage — 3.3V typ.
   - Input/output voltage difference (normal) — 0.3V typ.
   - Input/output voltage difference (back-up) — 0.3V typ.
   - Loss current (current consumption for back-up) — 0.1μA typ.

Package

SOP-14B (MM1106XF)
DIP-14A (MM1106XD)

Applications

1. Fax machines
2. Photocopiers
3. Air conditioners
4. Control equipment
5. Sequencers, etc.

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Power supply voltage	V_{CC} max.	−0.3~+7	V
Voltage applied to input pin	V_{IN}	−0.3~V_{CC}+0.3 (≦ +7)	V
Voltage applied to output pin	V_{OUT}	−0.3~V_{CC}+0.3 (≦ +7)	V
V_{OUT} output current 1	I_{L1}	50	mA
V_{OUT} output current 2	I_{L2}	120	μA
Allowable loss	Pd	300	mW
Storage temperature	T_{STG}	−40~+125	°C

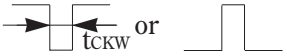
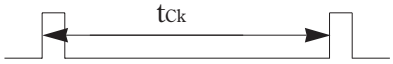
Note: I_{L1} expresses output current value from main power supply (V_{CC}) and I_{L2} expresses output current value from battery (V_{BAT}).

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Power supply voltage	V_{CC}	+2.5~+6.5	V
$\overline{\text{RESET}}$ sink current	I_{OLR}	0~1.0	mA
CS sink current	I_{OLC}	0~500	µA
V_{OUT} output current 1	I_{L1}	0~30	mA
V_{OUT} output current 2	I_{L2}	0~80	µA
Clock input high level voltage	V_{CKH}	2.0<	V
Clock input low level voltage	V_{CKL}	<0.4	V
Clock monitoring time setting	T_{WD}	1~1000	mS
Clock rise and fall times	T_{RCK}, T_{FCK}	<100	µS
Power supply voltage rise times	T_{RVCC}	100<	µS
Power supply voltage fall times	T_{FVCC}	50<	µS
TC pin capacitance	C_T	0.0002~2	µF
Operating temperature	T_{OP}	–25~+75	℃

Electrical Characteristics (Except where noted otherwise, Ta=25°C, V_{CC}=5.0V, V_{BAT}=3.0V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Consumption current	I_{CC}	V_{CC}=5.0V, I_O=0µA		270	400	µA
$\overline{\text{RESET}}$ detection voltage	V_{SLR}	V_{CC} : Hi → Lo	4.00	4.20	4.40	V
Detection voltage temperature coefficient R	$\frac{\Delta V_{SR}}{\Delta T}$			±0.01	±0.05	%/℃
Hysteresis voltage R	V_{HYSR}	V_{CC} : Lo → Hi	0.05	0.10	0.20	V
CK input threshold	V_{TH}		0.8	1.2	2	V
CK input current	I_{IH}	V_{CK}=5.0V		0	1	µA
	I_{IL}	V_{CK}=0V	–15	–7	–2	
Output voltage R H	V_{OHR}	$I_{\overline{RESET}}$=–5µA	4.0	4.5		V
Output voltage R L	V_{OLR}	$I_{\overline{RESET}}$=1.0mA		0.3	0.5	V
Output sync current R	I_{OLR}	V_{CC}=3.5V, $V_{\overline{RESET}}$=1V	1	2		mA
Output source current R	I_{OHR}	$V_{\overline{RESET}}$=4.5V	8	15		µA
C_T charge current	I_{CT1}	V_{TC}=0.7V during watchdog timer operation	–0.48	–0.24	–0.16	µA
	I_{CT2}	V_{TC}=0.7V during power ON reset operation	–0.48	–0.24	–0.16	µA
CS detection voltage	V_{SLC}	V_{CC} : Hi→Lo	4.20	4.40	4.60	V
Detection voltage temperature coefficient C	$\frac{\Delta V_{SC}}{\Delta T}$			±0.01	±0.05	%/°C
Hysteresis voltage C	V_{HYSC}	V_{CC} : Hi→Lo	0.05	0.10	0.20	V
Output voltage C H	V_{OHC}	V_{CC}=5.0V, I_{CS}=1µA	4.50	4.65		V
Output voltage C L	V_{OLC}	V_{CC}=3.5V, I_{CS}=1µA		0.1	0.4	V
Output sync current C	I_{OLC}	V_{CC}=3.5V, V_{CS}=0.3µA	0.5	1.0		mA
Output source current C	I_{OHC}	V_{CC}=5.0V, V_{CS}=4.5V	50	75		µA
Power supply switching voltage	V_{BB}	V_{CC} : Hi→Lo	3.15	3.30	3.45	V
Detection voltage temperature coefficient B	$\frac{\Delta V_{BB}}{\Delta T}$			±0.01	±0.05	%/℃
Hysteresis voltage B	V_{HYSB}	V_{CC} : Lo→Hi	0.05	0.10	0.20	V
I/O voltage difference 1 (normal)	V_{SAT1}	V_{CC}=5.0V, I_O=–30mA		0.3	0.5	V
I/O voltage difference 2 (backup)	V_{SAT2}	I_O=–80µA, V_{BAT}=3.0V		0.3	0.4	V

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Loss current	I_{LOSS}	V_{CC}=0V, I_O=0μA, V_{BAT}=3V			0.1	μA
Reverse current	I_{OREV}	V_{CC}=5.0V, I_O=0μA, V_{BAT}=0V			0.1	μA
External PNP transistor base-driving current	I_{BASE}	V_{CC}=5.0V, V_{OUT}=4.2V, V_{TB}=4.3V	2	5		mA
V_{CC} input pulse width	T_{PI}	V_{CC} 5.0V / 4.0V 	8			μS
CK input pulse width	T_{CKW}	CK  t_{CKW} or	20			μS
CK input cycle	T_{CK}	CK  t_{CK}	20			μS
Watchdog timer monitoring time *1	T_{WD}	C_T=0.02μF	50	100	150	mS
Watchdog timer reset time *2	T_{WR}	C_T=0.02μF	1	2	3	mS
Reset hold time for power supply rise *3	T_{PR}	V_{CC} : Lo→Hi (100μS), C_T=0.02μF	50	100	150	mS
$\overline{\text{RESET}}$ delay time	T_{PDR}	V_{CC} : Hi→Lo (50μS), C_{LR}=15pF, R_{LR}=22kΩ		10		μS
CS delay time	T_{PDC}	V_{CC} : Hi→Lo (50μS), C_{LC}=15pF		10		μS
$\overline{\text{RESET}}$ rise time	T_{RR}	C_{LR}=15pF, R_{LR}=22kΩ		4		μS
$\overline{\text{RESET}}$ fall time	T_{FR}	C_{LR}=15pF, R_{LR}=22kΩ		4		μS
CS rise time	T_{RC}	C_{LC}=15pF		4		μS
CS fall time	T_{FC}	C_{LC}=15pF		4		μS

Notes:

*1 Monitoring time is the time from the last pulse (negative edge) of the timer clear clock pulse until reset pulse output. In other words, reset output is output if a clock pulse is not input during this time.

*2 Reset time means reset pulse width. However, this does not apply to power ON reset.

*3 Reset hold time is the time from when V_{CC} exceeds detection voltage (V_{SHR}) during power ON reset until reset release ($\overline{\text{RESET}}$ output high).

*4 Watchdog timer monitoring time (T_{WD}), watchdog timer reset time (T_{WR}) and reset hold time (T_{PR}) during power supply rise can be changed by varying C_T capacitance. The times are expressed by the following formulae.

Example : when C_T=0.02μF

T_{PR} (mS) ≒ 5000 × C_T (μF) T_{PR} ≒ 100mS

T_{WD} (mS) ≒ 5000 × C_T (μF) T_{WD} ≒ 100mS

T_{WR} (mS) ≒ 100 × C_T (μF) T_{WR} ≒ 2mS

*5 The voltage range when measuring output rise and fall time is 10~90%.

*6 The IC can be made to operate only as a reset IC with delay during Vcc rise by connecting the RCT pin to GND.

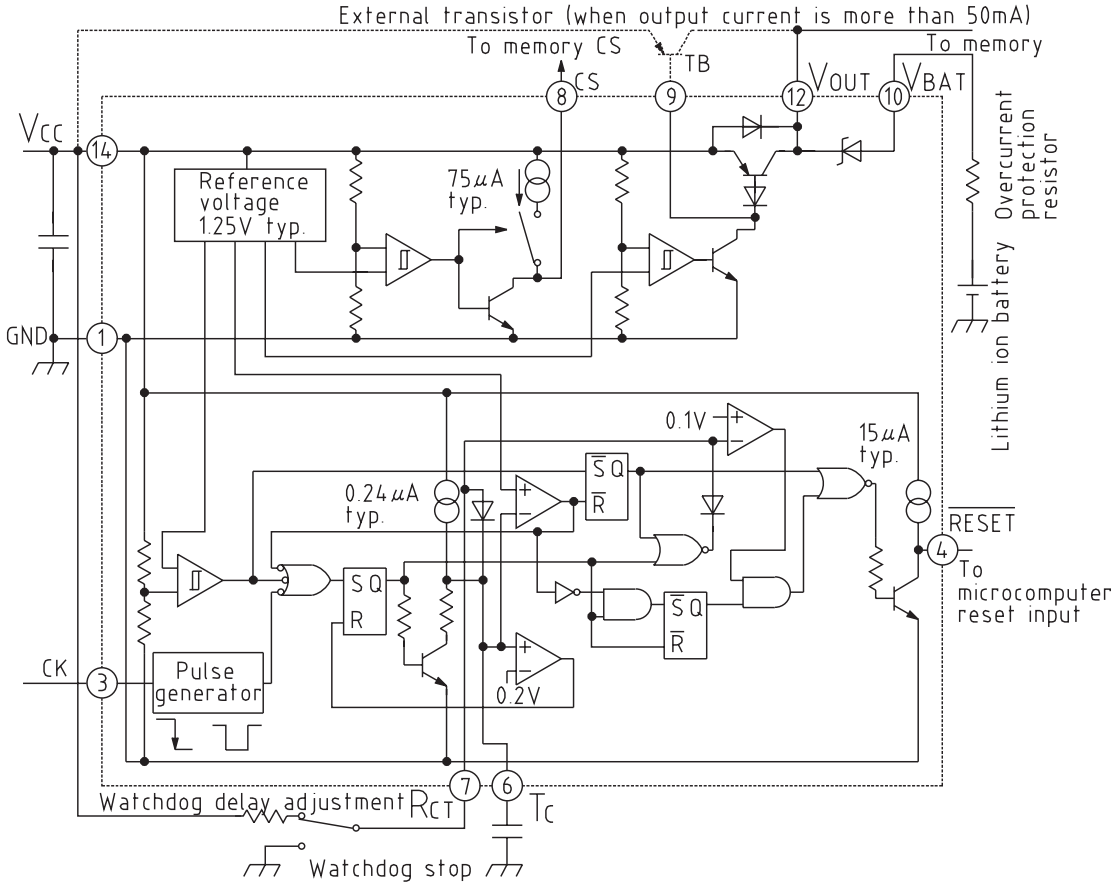
*7 V_{CC} rise time should be 100μS or more, and fall time should be 50μS or more.

Pin Description

Pin No.	Pin name	Function
1	GND	Ground
2	N.C	NON CONNECT
3	CK	Clock input
4	$\overline{\text{RESET}}$	Reset output
5	N.C	NON CONNECT
6	TC	Capacitor for setting power ON delay and timer monitoring times
7	RCT	Watchdog timer stop (when connected to GND); timer time adjustment
8	CS	Chip select output
9	TB	External power transistor drive pin
10	V_{BAT}	Back-up power supply input
11	N.C	NON CONNECT
12	V_{OUT}	Back-up voltage output
13	N.C	NON CONNECT
14	V_{CC}	Main power supply

Note : Connect external transistor when output current is more than 50mA.

Block Diagram



Timing Chart