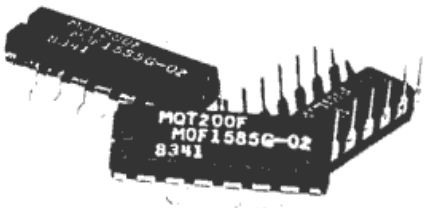
LeCroy

Monolithic Model MQT200F
Charge-to-Time Converter



- Current integrating
- Programmable sensitivity
- Quasi-differential input
- Monolithic design

The LeCroy MQT200F is a monolithic charge-to-time converter circuit. It is intended for use as the front end of a current-integrating Wilkenson ADC. It can be used for 10-bit operation with a conversion time of 2.5 μsec; however, similar performance can be achieved with slower conversion rates. It is ideal for those applications where exceptionally high packaging density is required. The MQT200F offers maximum flexibility while requiring a minimum of support components.

The MQT200F has a direct-coupled virtual-ground (low impedance) input, accepting fast 0 to −30 mA current pulses. A Gate signal enables the input causing it to integrate the analog signal at the input for the duration of the GATE. The charge resulting from this integration is stored on an external capacitor. The time duration required for this charge to be removed by a reference current is proportional to the input charge. A T^2L Output of this duration is provided. Internal opening and closing time of the Gate is less than 5 nsec with normal gate drive, and recommended gate duration is 25 to 500 nsec. An example of the typical operation sequence is shown in Figure 1.

The full scale output duration may be externally programmed over a wide range with little change in operating characteristics, but the specifications are shown optimized for a full scale output time of 2.5 μsec.

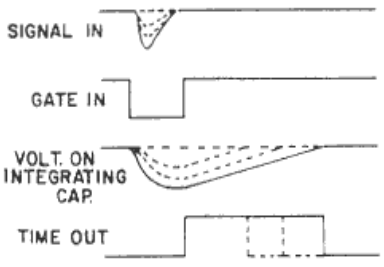


Figure 1

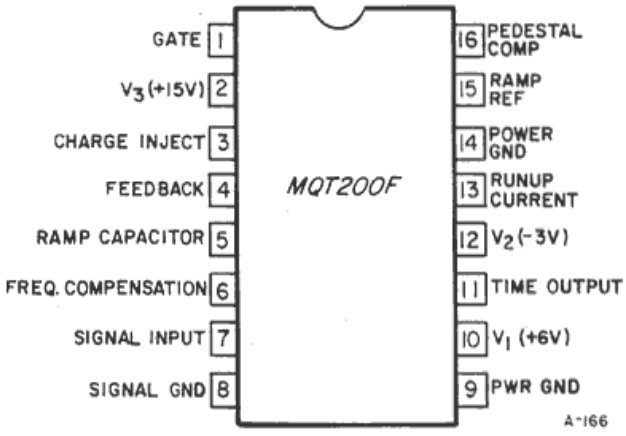


Figure 2

SPECIFICATIONS
Model MQT200F
CHARGE-TO-TIME CONVERTER

DC CHARACTERISTICS

Parameter	Min.	Nom.	Max.	Units	Comments
V_1 voltage Requirement	+ 5.8	+ 6	+ 6.2	V	
V_2 Voltage Requirement	− 2.8	− 3.0	− 3.2	V	
V_3 Voltage Requirement	+14.5	+15	+ 15.5	V	
V_1 Current Requirement	—	—	12	mA	Static Condition
V_2 Current Requirement	—	—	14	mA	Static Condition
V_3 Current Requirement	—	—	3	mA	Static Condition
Power Dissipation	—	—	166	mW	Static Condition

INPUT REQUIREMENTS AND PERFORMANCE CHARACTERISTICS*

Parameter	Min.	Typ.	Max.	Units	Comments
Input Signal, Negative	—	—	− 30	mA	
Input Signal, Positive	—	—	100	μA	May be extended (see text)
Input Impedance	—	0.05	0.15	Ω	0 to − 30 mA DC
Input Offset Voltage	− 3	0	+ 3	mV	
Temp. Coefficient of above	—	0.08	0.20	mV/°C	
Full-Scale Charge	—	256	1024	pC	Determined by value of Ramp Capacitor
Gate Duration	25	—	500	nsec	
Gate Amplitude—isolate	7.3	7.5	8.0	V	
Gate Amplitude—integrate	4.8	5.0	5.2	V	
Gate Open/Close Time	—	—	5	nsec	Gate must precede input by at least 5 nsec
Program Current	10	100	250	μA	(V_G/R_G) See Figure 3
Non-linearity	± 0.25 (1 + reading/full scale)			pC	Best straight line
Noise	—	0.075	0.25	pC(rms)	With 50 nsec gate, 100 Ω source (i.e., 50 Ω series termination plus 50 Ω cable)

*At recommended operating voltage and 25°C ambient temperature unless otherwise noted.

SPECIFICATIONS SUBJECT TO CHANGE

PIN ASSIGNMENTS (See Figure 2)

Pin #	Description	Comments
1	Gate Input	Direct-coupled. Input impedance greater than 5 kΩ. Logic States: Isolate 7.3-8.0 V, Integrate 4.8-5.2 V.
2	V_3	+15 V ±500 mV.
3	Charge Inject	Connect a 3-18 pF capacitor between Pin 1 and Pin 3 to adjust offset. (Dependent on amplitude of gate signal. See Text.)
4	Feedback	Tie to Pin 7 (Provides the required feedback for the input amplifier.)
5	Ramp Capacitor	Requires 33 pF to V_3 for 256 pC Full Scale (increasing to 200 pF for 1024 pC full scale).
6	Freq. Compensation	Requires 3-18 pF trimmer and series 30 Ω resistor to signal ground. Adjust trimmer for minimum perturbation on Pin 7.
7	Signal Input	Virtual ground. Signal should follow gate opening by more than 5 nsec. Should be series-terminated for proper impedance match. Input impedance 50 mΩ nominal. Higher for slew rates exceeding 2 mA/nsec.
8	Signal Ground	Voltage reference for the input amplifier. Normally connected to printed circuit ground plane, but may be used for quasi-differential input mode (see text).
9	Power Ground	Connect to printed ground plane.
10	V_1	+6 V ±200 mV.
11	Time output	Open collector T^2L, requires external pull-up resistor. Normally low. (max sink 2.5 mA). Trailing edge response time ≥ 70 nsec (decreases with an increase in programming current).
12	V_2	−3 V ±200 mV.
13	Runup Current	Runup ramp current typically 100 μA (see text).
14	Power Ground	Connect to printed circuit ground plane.
15	Ramp Ref	Used as reference for fast clearing of ramp.
16	Pedestal Compensation	Used to compensate time output dependence on gate width.

APPLICATION HINTS (See Figure 3)

Layout Guidelines

For the purpose of prototyping and evaluation, a test board with a minimum of support circuitry may be needed. Attached is a schematic suggested for a "test board." Continuous ground-plane construction should be used and lead lengths kept to a minimum. The MQT200F is powered by +6, −3, and +15 V supplies. All three power supply voltages and all reference levels should be bypassed to ground with high-frequency capacitors. If multiple channels are used on a circuit board, each supply should be decoupled by a separate series choke with a large value capacitor to ground. In addition, one or more references are employed to program the rundown current. Because of the sensitivity of gain to these voltages, separate supplies should be used.

Programming the Runup Current

The gain (output time vs. input charge) of the MQT200F is determined by the Runup Current. Because the Program Current input (Pin 13) is a 0 V referenced virtual ground, the current is most easily generated by connecting an appropriate stable resistor (R_G) to a stable positive voltage (V_G). The test and recommended operating conditions, optimized for fast conversion, use a full scale charge of 256 pC and a Program Current of 100 μA. This will provide 2.56 μsec (256 pC/100 μA) of usable output time. Gain therefore is 10 nsec/pC (1 count per pC if a 100 MHz gated digital counter is used). Reducing the Program Current will proportionally increase the full scale output time duration. Note: A 100 MHz clock is used as an example but requires a stable pickoff on the Time Output because of the output trailing edge response time of 70 nsec.

When the value of Runup Current used is in excess of 100 μA, a gate width dependent pedestal will result. This can be cancelled by injecting an equal but negative DC bias current into the Signal Input (Pin 7). This is most easily accomplished by connecting an appropriate stable resistor (R_B) to a negative voltage (V_B) on schematic.

Digital Processing

The time output of the MQT200F is proportional duration to the total charge input. The beginning of the valid time output occurs after the trailing edge of the gate signal. It is recommended that the time-to-digital conversion begin at approximately 5% of the

full scale time after the leading edge of the gate. The Charge Inject can then be set (with no input signal) to provide a near zero but positive Pedestal. (See Pedestal Adjust below).

Converting the time output to digital form is most easily accomplished by gating a stable oscillator with the MQT200F output, and counting the result with a digital counter. Fast conversion requires a fast counter (e.g., 100 MHz provides 8 bits in 2.54 μsec) but if speed is not important, a longer full scale conversion time makes the counting circuit simpler. Alternatively, a time-to-digital converter (TDC) may be used.

Pedestal Adjust (Charge Inject and Pedestal Compensation)

Pedestal in the MQT200F may be adjusted by means of an external trimmer capacitor between pins 1 and 3, which injects charge (equal to the value of the trimmer times the gate amplitude) into the ramp capacitor at the leading edge of the gate. Pedestal charge should be just enough to ensure low end linearity. It is normally set at 2% to 5% of full scale charge. It can be digitally subtracted by delaying the clock start time. A gate width dependent pedestal term is also present which can be minimized by proper adjustment of the Pedestal Compensation adjust (Pin 16). Set it (see Figure 3) so there is no change in pedestal for narrow or wide gates. If gates are narrow (< 200 nsec) and fixed width, Pin 16 can be left open.

Gate Input Driver Requirements

The gate input (Pin 1) has a resistance of about 5 kΩ in parallel with 5 pF plus the pedestal adjustment capacitor (up to 8 pF). Gate rise and falltimes should be less than 3 nsec to assure optimum stability of the effective gate width. Gate amplitude should be about 2.5 V and be stable to assure stable injected charge. Sufficiently large and fast input pulses may penetrate the "isolate" gate of the MQT200F and cause spurious outputs. The amplitude level at which this occurs is strongly dependent on the source impedance of the gate driver, the quiescent voltage level of the gate, and the risetime of the input pulse. To minimize punchthrough, the gate should be driven from a low-impedance source such as an emitter follower or (in a system) a low-impedance stripline (50 Ω or less) and the quiescent level of the gate should be set on the high side (+ 7.5 to 8 V). If careful attention is paid to minimizing gate source impedance (including lead inductance), punchthrough should not occur for inputs of greater than 4 nsec risetime up to − 3 V amplitude.

Differential Inputs

The MQT200F is basically a single-ended input device. Nevertheless, a quasi-differential input mode is provided that may aid in suppressing low-frequency (< 1 kHz) common mode pick-up in some applications. This is accomplished by bringing out the reference pin for the input amplifier separately, so that it may be separately grounded or connected to the shield of the input coaxial cable or the positive side of a twisted pair. The common mode range in this configuration is limited to a few hundred mV. The proper use of this input can be seen in Figure 3.

Input Pulse Shape

The MQT200F is designed for operation with normal photomultiplier anode pulses and pulses of similar shape. Its linear range extends in the negative direction to 30 mA, but in the positive direction to only about 100 μA. This limitation in the positive direction is imposed by the desire to minimize the front-end standing current, which in turn minimizes output pedestal dependence on gate width. If the input pulse is entirely negative, as is the case with unshaped standard PM pulses, the limited positive range is of no consequence. However, if the input pulse is coupled via a small capacitor or a pulse transformer, the resulting differentiation produces a positive overshoot on the trailing edge of the pulse which may exceed the positive linear range. This will result in a nonlinear response. For best linearity, differentiation of the input pulse should be avoided. Where this is not possible, the linear range in the positive direction can be extended by standing additional current in the input circuit by means of a resistor from the signal input (Pin 7) to a stable negative supply voltage. This additional current is integrated during the gate and will increase both the pedestal and the dependence of pedestal on the gate width. (For example, standing an additional 1 mA will allow linear operation with overshoots up to 50 mV, in a 50 Ω system, but will add 1 pC of pedestal per nsec of gate width which will cause a reduction in the pedestal stability and limits the useful range of the device). Except for extremely fast pulses, the impedance of the signal input is very low. If however, the input pulses have a rise or falltime in excess of 2 mA/nsec, it may be necessary to add about 10pF from the signal input to ground. This will effectively perform a short term integration, holding the change until the input can respond.

Fast Clear

If a fast clear is necessary, an FET can be [illegible]ted across the ramp and ramp reference. It should be held in its low impedance state from the time at which a Clear is asserted to the leading edge of the gate, then released fast and held in its high impedance state until the next clear.

Integrate and Hold

Under limited conditions, the MQT200F can be used as an integrate and hold circuit. This is accomplished by using the fast clear described above and reducing the Ramp Current to 1 μamp. The ramp voltage (Pin 5) is then monitored with a high impedance (> 10 MΩ), low leakage (< 1 μA), fast (< 10 μsec rise and transfer time) voltage buffer or FET. With a total of 200 pF on Pin 1 (1024 pC full scale), the voltage will have a quiescent value of about 11 V and will go negative about 4 mV/pC (approximately 4.1 volts total). The droop will be about 1% per 10 μsec, depending on the external components used, requiring the next stage to be relatively fast.

Time Output

Under certain loading conditions this output may have a low level oscillation on its baseline. The amplitude of the oscillation is smaller than T²L levels and should not cause a problem. If necessary, some integrating may be used to smooth the falltime. The

70-80 nsec trailing edge will require that a circuit with a stable threshold be used if high accuracy of the time interval is required for high speed conversion.

Power on Sequence

Ideally all three supplies (+15 V, +6 V, −3 V) should be applied simultaneously. However, due to different charging times associated with the power supply filter capacitors, it is likely that one supply might lead the other two. This might cause a temporary latch up condition in the MQT200F. The two diodes shown in Figure 3 should prevent this latch up from occurring. For PC boards containing multiple channels, only one pair of diodes is required per board.

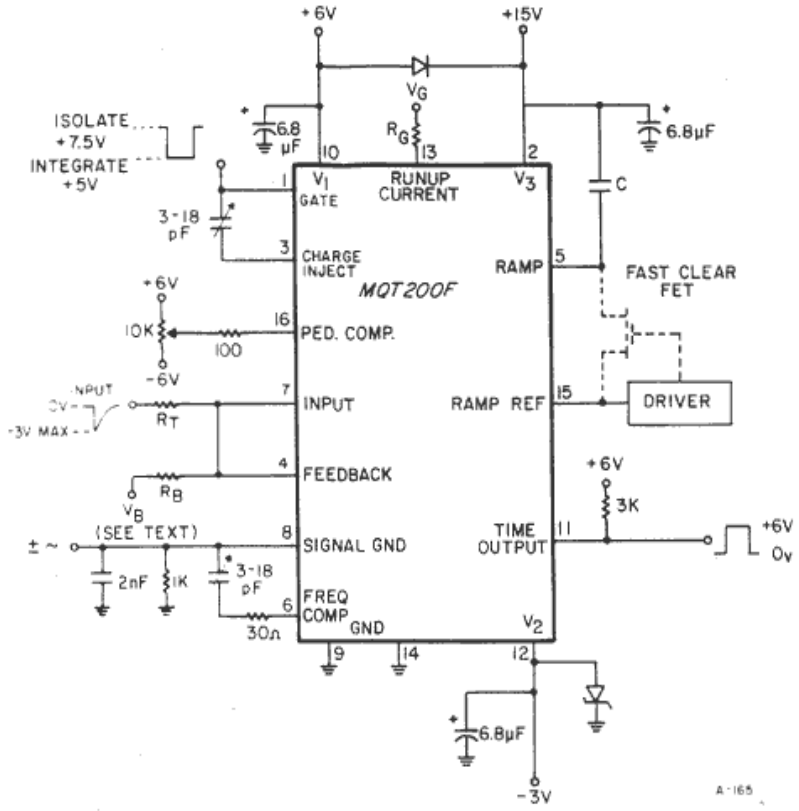


Figure 3

R_T Termination Resistor: 50 Ω for 50 Ω cable.

R_B Bias Resistor: R_B selected to cancel Program Current. Omit R_B and V_B for program currents less than 100 µA.

V_B Bias Voltage: V_B more negative than −6 V.

R_G Gain Resistor: R_G selected to generate Runup Current = V_G/R_G.

V_G Gain Voltage: V_G greater than +6 V.

Omit Pedestal Comp for narrow, fixed gate operation (leave pin 16 open).

Tie pin 8 to ground, omitting 1 kΩ resistor and 2 nF capacitor for non-quasi-differential operation.

Select Ramp Capacitor and program current from table below for optimum full scale charge and full scale output time.

FULL SCALE INPUT Q (pC)	RAMP CAPACITOR (pF)	FULL SCALE OUTPUT TIME (µsec)	PROGRAM CURRENT (µA)
256	33	2.56	100
1024	200	10.24	100
1024	200	102.4	10