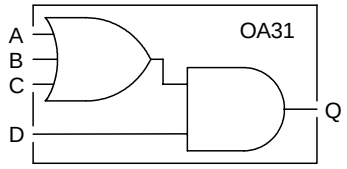
OA31 is an OR/AND circuit providing the logical function Q = [(A+B+C).D].

Truth Table

A	B	C	D	Q
L	L	L	X	L
X	X	X	L	L
X	X	H	H	H
X	H	X	H	H
H	X	X	H	H



Capacitance

	Ci (pF)
A	0.055
B	0.055
C	0.063
D	0.032

Area

0.81 mils^2

Power

2.40 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(L) with L = Output Load [pF]

AC Characteristics : Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.1	L = 0.7	L = 1.0	L = 0.1	L = 0.7	L = 1.0
Delay A to Q	tpdar	0.68	2.06	2.78	0.78	2.15	2.79
	tpdaf	0.74	1.86	2.40	0.86	1.97	2.53
Delay B to Q	tpdbr	0.63	2.01	2.69	0.73	2.06	2.73
	tpdbf	0.72	1.86	2.37	0.90	2.01	2.56
Delay C to Q	tpdcr	0.57	1.96	2.59	0.64	1.96	2.65
	tpdcf	0.65	1.77	2.33	0.91	2.04	2.58
Delay D to Q	tpddr	0.63	2.02	2.70	0.80	2.19	2.85
	tpddf	0.64	1.80	2.34	0.99	2.15	2.70
Output Slope A to Q	op_slar	1.00	5.37	7.36	0.96	5.21	7.52
	op_slaf	0.77	3.67	4.98	0.76	3.57	5.07
Output Slope B to Q	op_slbr	1.00	5.17	7.61	0.93	5.30	7.50
	op_slbf	0.77	3.63	5.05	0.78	3.73	4.98
Output Slope C to Q	op_slcr	0.98	5.27	7.56	0.95	5.26	7.52
	op_slcf	0.77	3.51	5.05	0.76	3.61	4.95
Output Slope D to Q	op_sldr	1.00	5.37	7.61	0.95	5.30	7.53
	op_sldf	0.80	3.65	5.35	0.86	3.81	5.33