PIC18F2420/2520/4420/4520 Rev. A1 Silicon Errata Sheet

The PIC18F2420/2520/4420/4520 Rev. A1 parts you have received conform functionally to the Device Data Sheet (DS39631), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2420/2520/4420/4520 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

All the problems listed here will be addressed in future revisions of the PIC18F2420/2520/4420/4520 silicon.

The following silicon errata apply only to PIC18F2420/2520/4420/4520 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2420	01 0001 010	00001
PIC18F2520	01 0001 000	00001
PIC18F4420	01 0000 110	00001
PIC18F4520	01 0000 100	00001

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: MSSP

In its current implementation, the I^2C™ Master mode operates as follows:

a) The Baud Rate Generator for I^2C in Master mode is slower than the rates specified in Table 17-3 of the Device Data Sheet.

For this revision of silicon, use the values shown in Table 1 in place of those shown in Table 17-3 of the Device Data Sheet. The differences are shown in **bold** text.

b) Use the following formula in place of the one shown in Register 17-4 (SSPCON1) of the Device Data Sheet for bit description SSPM3:SSPM0 = `1000`.

SSPADD = INT((FCY/FSCL) – (FCY/1.111 MHz)) – 1

Date Codes that pertain to this issue:

All engineering and production devices.

TABLE 1: I^2C™ CLOCK RATE w/BRG

FOSC	FCY	FCY * 2	BRG Value	FSCL (2 Rollovers of BRG)
40 MHz	10 MHz	20 MHz	**0Eh**	400 kHz(1)
40 MHz	10 MHz	20 MHz	**15h**	312.5 kHz
40 MHz	10 MHz	20 MHz	**59h**	100 kHz
16 MHz	4 MHz	8 MHz	**05h**	400 kHz(1)
16 MHz	4 MHz	8 MHz	**08h**	308 kHz
16 MHz	4 MHz	8 MHz	**23h**	100 kHz
4 MHz	1 MHz	2 MHz	**01h**	333 kHz(1)
4 MHz	1 MHz	2 MHz	**08h**	100 kHz
4 MHz	1 MHz	2 MHz	00h	1 MHz(1)

Note 1: The I^2C™ interface does not conform to the 400 kHz I^2C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

2. Module: MSSP

When the MSSP is configured for SPI™ Master mode, the SDO pin cannot be disabled by setting the TRISC<5> bit. The SDO pin always outputs the content of SSPBUF regardless of the state of the TRIS bit.

In Slave mode with Slave Select enabled, SSPM3:SSPM0 = 0010 (SSPCON1<3:0>), the SDO pin can be disabled by placing a logic high level on the $\overline{SS}$ pin (RA5).

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: MSSP

After an I^2C transfer is initiated, the SSPBUF register may be written for up to 10 T_{CY} before additional writes are blocked. The data transfer may be corrupted if SSPBUF is written during this time.

The WCOL bit is set any time an SSPBUF write occurs during a transfer.

Work around

Avoid writing SSPBUF until the data transfer is complete, indicated by the setting of the SSPIF bit (PIR1<3>).

Verify the WCOL bit (SSPCON1<7>) is clear after writing SSPBUF to ensure any potential transfer in progress is not corrupted.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: MSSP

In 10-bit Addressing mode, when a Repeated Start is issued, followed by the high address byte and a write command ($R/\overline{W}$ = 0), an ACK is not issued.

Work around

There are two work arounds available:

1. Single-Master Environment:
   In a single-master environment, the user must issue a Stop, then a Start, followed by a write to the address high, then the address low followed by the data.
2. Multi-Master Environment:
   In a multi-master environment, the user must issue a Repeated Start, send a dummy write command to a different address, issue another Repeated Start and then send a write to the original address. This procedure will help maintain control of the bus.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: MSSP

I^2C Receive mode should be enabled (i.e., RCEN bit should be set) only when the system is idle (i.e., when ACKEN, RCEN, PEN, RSEN and SEN all equal zero). It should not be possible to set the RCEN bit when the system is not idle, however, the RCEN bit can be set under this circumstance.

Work around

Wait for the system to become idle before setting the RCEN bit. This requires a check for the following bits to be clear:

ACKEN, RCEN, PEN, RSEN and SEN.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: ECCP

When the ECCP1 auto-shutdown feature is configured for automatic restart by setting the PRSEN bit (PWM1CON<7>), the pulse terminates immediately in a shutdown event. In addition, the pulse may restart within the period if the shutdown condition expires. This may result in the generation of short pulses on the PWM output(s).

Work around

Configure the auto-shutdown for software restart by clearing the PRSEN bit (PWM1CON<7>). The PWM can be re-enabled by clearing the ECCPASE bit (ECCP1AS<7>) after the shutdown condition expires.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: ECCP

When monitoring a shutdown condition using a bit test on the ECCPASE bit (ECCP1AS<7>), or performing a bit operation on the ECCPASE bit, the device may produce unexpected results.

Work around

Before performing a bit test or bit operation on the ECCPASE bit, copy the ECCP1AS register to the working register and perform the operation there.

By avoiding these operations on the ECCPASE bit in the ECCP1AS register, the module will operate normally.

In Example 1, ECCPASE bit operations are performed on the W register.

EXAMPLE 1:

```
MOVF    ECCP1AS, W
BTFSC   WREG, ECCPASE
BRA     SHUTDOWN_ROUTINE
```

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: ECCP

The auto-shutdown source, FLT0, has inverse polarity from the description in **Section 16.4.7 "Enhanced PWM Auto-Shutdown"** of the Device Data Sheet. A logic high-voltage level on FLT0 will generate a shutdown on ECCP1.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

9. Module: ECCP and CCP

The CCP1 and CCP2 configured for PWM mode, with 1:1 Timer2 prescaler and duty cycle set to the period minus 1, may result in the PWM output(s) remaining at a logic low level.

Clearing the PR2 register to select the fastest period may also result in the output(s) remaining at a logic low output level.

Work around

To ensure a reliable waveform, verify that the selected duty cycle does not equal the 10-bit period minus 1 prior to writing these locations, or use 1:4 or 1:16 Timer2 prescale. Also, verify the PR2 register is not written to 00h.

All other duty cycle and period settings will function as described in the Device Data Sheet.

The ECCP and CCP modules remain capable of 10-bit accuracy.

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: ECCP

ECCP1 configured for auto-shutdown with Comparator 1 corrupts the PWM duty cycle pulse. In addition, it does not always synchronize the pulse to the beginning of the period and the end of the pulse can occur at any time within the period.

Work around

Use FLT0 for the auto-shutdown source. Applications which can tolerate a shutdown response time of several TCYS may use the comparator interrupt flag to detect a shutdown event and disable the PWM by clearing the EECPASE bit (ECCP1AS<7>).

Date Codes that pertain to this issue:

All engineering and production devices.

11. Module: ECCP

When the shutdown state of the PWM pin(s) is configured to tri-state the outputs, the device may consume higher than expected current during the shutdown event.

Work around

Configure the PWM output for either a high or low logic state during the shutdown via the PSSAC1:PSSAC0 (ECCP1AS<3:2>) and PSSBD1:PSSBD0 (ECCP1AS<1:0>) bits. Clearing the auto-shutdown event will return the device to normal current consumption levels.

Date Codes that pertain to this issue:

All engineering and production devices.

12. Module: ECCP

The PWM pin(s) may change state if a breakpoint is encountered during emulation and an auto-shutdown event occurs via FLT0. This affects the MPLAB® ICD 2 debugger and the ICE 2000 and ICE 4000 emulators.

Work around

During emulation, use the comparator for auto-shutdown. Applications which can tolerate a shutdown response time of several TCYs may use the external interrupt flag, INT0IF, to detect a shutdown event and disable the PWM by clearing the ECCPASE bit (ECCP1AS<7>).

Date Codes that pertain to this issue:

All engineering and production devices.

13. Module: ECCP and CCP

When operating either Timer1 or Timer3 as a counter with a prescale value other than 1:1 and operating the ECCP in Compare mode with the Special Event Trigger (CCP1CON bits CCP1M3:CCP1M0 = 1011), the Special Event Trigger Reset of the timer occurs as soon as there is a match between TMRxH:TMRxL and CCPR1H:CCPR1L.

This differs from the PIC18F452, where the Special Event Trigger Reset of the timer occurs on the next prescaler output pulse after the match between TMRxH:TMRxL and CCPR1H:CCPR1L.

Work around

To achieve the same timer Reset period on the PIC18F4520 family as the PIC18F452 family for a given clock source, add 1 to the value in CCPR1H:CCPR1L. In other words, if CCPR1H:CCPR1L = x for the PIC18F452, to achieve the same Reset period on the PIC18F4520 family, CCPR1H:CCPR1L = x + 1, where the prescale is 1, 2, 4 or 8 depending on the T1CKPS1:T1CKPS0 bit values.

Date Codes that pertain to this issue:

All engineering and production devices.

14. Module: ECCP

When a shutdown condition occurs, the output port is made inactive for the duration of the event. After the event that caused the shutdown ends, the ECCP module enables the PWM output right away instead of waiting until the beginning of the next PWM cycle.

Work around

Disable the auto-restart feature in software, polling the Timer2 Interrupt Flag (TMR2IF) and wait until it is set before clearing the ECCPASE bit.

Date Codes that pertain to this issue:

All engineering and production devices.

15. Module: ECCP

When switching direction in Full-Bridge PWM mode, the modulated outputs will switch immediately instead of waiting for the next PWM cycle. This may generate unexpected short pulses on the modulated outputs.

Work around

Disable the PWM or set duty cycle to zero prior to switching directions.

Date Codes that pertain to this issue:

All engineering and production devices.

16. Module: A/D

The A/D offset is greater than the specified limit in Table 26-24 of the Device Data Sheet. The additional Parameter A06A and updated conditions and limits are shown in **bold** text in Table 2.

Work around

Three work arounds exist.

1. Configure the A/D to use the VREF+ and VREF- pins for the voltage references. This is done by setting the VCFG<1:0> bits (ADCON1<5:4>).
2. Perform a conversion on a known voltage reference voltage and adjust the A/D result in software.
3. Increase system clock speed to 40 MHz and adjust A/D settings accordingly. Higher system clock frequencies decrease offset error.

TABLE 2: A/D CONVERTER CHARACTERISTICS: PIC18FX42X/X52X (INDUSTRIAL, EXTENDED) PIC18LFX42X/X52X (INDUSTRIAL)

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
A06A	**EOFF**	**Offset Error**	**—**	**—**	**<±1.5**	**LSb**	**VREF = VREF+ and VREF-**
A06	EOFF	Offset Error	—	—	**<±3.5**	LSb	**VREF = VSS and VDD**

Date Codes that pertain to this issue:

All engineering and production devices.

17. Module: BOD

The BOD module may reset below the minimum operating voltage of the device when configured for BORV1:BORV0 = 11. The updated Reset voltage specifications are shown in **bold** in Table 3.

TABLE 3: BROWN-OUT RESET VOLTAGE

Param No.	Sym	Characteristic	Min	Typ	Max	Unit
D005	VBOR	**Brown-out Reset Voltage**				
		PIC18LF2420/2520/4420/4520				
		BORV1:BORV0 = 11	**N/A**	2.05	**N/A**	V

Work around

Use the next higher BOD voltage setting to ensure a low VDD is detected above 2.0V.

Date Codes that pertain to this issue:

All engineering and production devices.

18. Module: EUSART

When performing back-to-back transmission in 9-bit mode (TX9D bit in the TXSTA register is set), an ongoing transmission's timing can be corrupted if the TX9D bit (for the next transmission) is not written immediately following the setting of TXIF. This is because any write to the TXSTA register results in a reset of the baud rate timer which will effect any ongoing transmission.

Work around

Load TX9D just after TXIF is set, either by polling TXIF or by writing TX9D at the beginning of the Interrupt Service Routine, or only write to TX9D when a transmission is not in progress (TRMT = 1).

Date Codes that pertain to this issue:

All engineering and production devices.

19. Module: EUSART

When performing back-to-back transmission in 9-bit mode (TX9D bit in the TXSTA register is set), the second byte may be corrupted if it is written into TXREG immediately after the TMRT bit is set.

Work around

Execute a software delay, at least one-half the transmission's bit time, after TMRT is set and prior to writing subsequent bytes into TXREG.

Date Codes that pertain to this issue:

All engineering and production devices.

20. Module: Timer1/Timer3

When Timer1 or Timer3 is configured for external clock source, and the CCPxCON register is configured with 0x0B (Compare mode, trigger special event), the timer is not reset on a Special Event Trigger.

Work around

Modify firmware to reset the Timer1/Timer3 registers upon detection of the compare match condition — TMRxL and TMRxH.

Date Codes that pertain to this issue:

All engineering and production devices.

21. Module: Timer1/Timer3

When Timer1 or Timer3 is in External Clock Synchronized mode and the external clock period is between 1 and 2 TCY, interrupts will occasionally be skipped.

Work around

Avoid using an external clock with a period (1/frequency) between 1 and 2 TCY.

Date Codes that pertain to this issue:

All engineering and production devices.

22. Module: Timer1/Timer3

When Timer1/Timer3 is operating in 16-bit mode and the prescale setting is not 1:1, a write to the TMR1H/TMR3H Buffer registers may lengthen the duration of the period between the increments of the timer for the period in which TMR1H/TMR3H was written.

Work around

Two work arounds are available: 1) Stop Timer1/Timer3 before writing the TMR1H/TMR3H registers; 2) Write TMR1L/TMR3L immediately after writing TMR1H/TMR3H.

Date Codes that pertain to this issue:

All engineering and production devices.

23. Module: Interrupts

If an interrupt occurs during a two-cycle instruction that modifies the STATUS, BSR or WREG register, the unmodified value of the register will be saved to the corresponding Fast Return (Shadow) register and upon a fast return from the interrupt, the unmodified value will be restored to the STATUS, BSR or WREG register.

For example, if a high priority interrupt occurs during the instruction, `MOVFF TEMP, WREG`, the `MOVFF` instruction will be completed and WREG will be loaded with the value of `TEMP` before branching to ISR. However, the previous value of WREG will be saved to the Fast Return register during ISR branching. Upon return from the interrupt with a fast return, the previous value of WREG in the Fast Return register will be written to WREG. This results in WREG containing the value it had before execution of `MOVFF TEMP, WREG`.

Affected instructions are:

`MOVFF Fs, Fd`
where `Fd` is WREG, BSR or STATUS;

`MOVSF Zs, Fd`
where `Fd` is WREG, BSR or STATUS; and

`MOVSS [Zs], [Zd]`
where the destination is WREG, BSR or STATUS.

Work around

1. Assembly Language Programming:

a) If any two-cycle instruction is used to modify the WREG, BSR or STATUS register, do not use the `RETFIE FAST` instruction to return from the interrupt. Instead, save/restore WREG, BSR and STATUS via software per Example 9-1 in the Device Data Sheet. Alternatively, in the case of `MOVFF`, use the `MOVF` instruction to write to WREG instead. For example, use:

```
MOVF   TEMP, W
MOVWF  BSR
```

instead of: `MOVFF TEMP, BSR`.

b) As another alternative, the following work around shown in Example 2 can be used. This example overwrites the Fast Return register by making a dummy call to `Foo` with the fast option in the high priority service routine.

EXAMPLE 2:

```
ISR @ 0x0008
  CALL    Foo, FAST    ; store current value of WREG, BSR, STATUS for a second time
Foo:
  POP                  ; clears return address of Foo call
  :                    ; insert high priority ISR code here
  :
  RETFIE  FAST
```

2. C Language Programming: The exact work around depends on the compiler in use. Please refer to your C compiler documentation for details.

   If using the Microchip MPLAB® C18 C Compiler, define both high and low priority interrupt handler functions as “low priority” by using the `pragma interruptlow` directive. This directive instructs the compiler to not use the `RETFIE FAST` instruction. If the proper high priority interrupt bit is set in the IPRx register, then the interrupt is treated as high priority in spite of the `pragma interruptlow` directive.

   The code segment shown in Example 3 demonstrates the work around using the C18 compiler:

EXAMPLE 3:

```
#pragma interruptlow MyLowISR
void MyLowISR(void)
{
   // Handle low priority interrupts.
}

// Although MyHighISR is a high priority interrupt, use interruptlow pragma so that
// the compiler will not use retfie FAST.

#pragma interruptlow MyHighISR
void MyHighISR(void)
{
   // Handle high priority interrupts.
}

#pragma code highVector=0x08
void HighVector (void)
{
   _asm goto MyHighISR _endasm
}
#pragma code /* return to default code section */

#pragma code lowVector=0x18
void LowVector (void)
{
   _asm goto MyLowISR _endasm
}
#pragma code /* return to default code section */
```

Date Codes that pertain to this issue:

All engineering and production devices.

24. Module: EUSART

The EUSART auto-baud feature may periodically measure the incoming baud rate incorrectly. The rate of incorrect baud rate measurements will depend on the frequency of the incoming synchronization byte and the system clock frequency.

Work around

None.

25. Module: EUSART

In Synchronous mode (SYNC = 1) with clock polarity high (SCKP = 1), the EUSART transmits a shorter than expected clock on the CK pin for bit 0.

Work around

None.

26. Module: EUSART

In Synchronous mode, EUSART baud rates using SPBRG values of '0' and '1' may not function correctly.

Work around

Use another baud rate configuration to generate the desired baud rate.

27. Module: MSSP

In an I²C™ system with multiple slave nodes, an unaddressed slave may respond to bus activity when data on the bus matches its address. The first occurrence will set the BF bit. The second occurrence will set the BF and SSPOV bits. In both situations, the SSPIF bit is not set and an interrupt will not occur. The device will vector to the Interrupt Service Routine only if the interrupt is enabled and an address match occurs.

Work around

The I²C slave must clear the SSPOV bit after each I²C address match to maintain normal operation.

28. Module: MSSP

In I²C Master mode, the BRG value of '0' may not work correctly.

Work around

Use a BRG value greater than '0' by setting SSPADD ≥ 1.

29. Module: MSSP

In I²C Master mode, the RCEN bit is set by software to begin data reception and cleared by the peripheral after a byte is received. After a byte is received, the device may take up to 80 TCY to clear RCEN and 800 TCY when using MPLAB® ICD 2 and MPLAB ICE emulators.

Work around

Single byte receptions are typically not affected, since the delay between byte receptions is typically long enough for the RCEN bit to clear. For multiple byte receptions, the software must wait until the bit is cleared by the peripheral before the next byte can be received.

30. Module: MSSP

Setting the SEN bit initiates a Start sequence on the bus, after which, the SEN bit is cleared automatically by hardware. If the SEN bit is set again (without an address byte being transmitted), a Start sequence will not commence and the SEN bit will not be cleared. This condition causes the bus to remain in an active state. The system is Idle when ACKEN, RCEN, PEN, RSEN and SEN are clear.

Work around

Set the PEN or RSEN bit to transmit a Stop or Repeated Start sequence, although the SEN bit may still be set, indicating the bus is active. After the sequence has completed, the PEN, RSEN and SEN bit will be clear, indicating the bus is Idle. Clearing and setting the SSPEN bit will also reset the I²C peripheral and clear the PEN, RSEN and SEN status bits.

31. Module: MSSP

In SPI mode, the Buffer Full flag (BF bit in the SSPSTAT register), the Write Collision Detect bit (WCOL bit in SSPCON1) and the Receive Overflow Indicator bit (SSPOV in SSPCON1) are not reset upon disabling the SPI module (by clearing the SSPEN bit in the SSPCON1 register).

For example, if SSPBUF is full (BF bit is set) and the MSSP module is disabled and re-enabled, the BF bit will remain set. In SPI Slave mode, a subsequent write to SSPBUF will result in a write collision. Also, if a new byte is received, a receive overflow will occur.

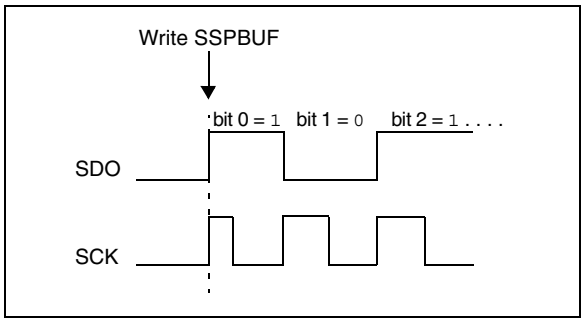
Work around

Ensure that if the buffer is full, SSPBUF is read (thus clearing the BF flag) and WCOL is clear before disabling the MSSP module. If the module is configured in SPI Slave mode, ensure that the SSPOV bit is clear before disabling the module.

32. Module: MSSP (SPI Mode)

When the SPI is using Timer2/2 as the clock source, a shorter than expected SCK pulse may occur on the first bit of the transmitted/received data (Figure 1).

FIGURE 1: SCK PULSE VARIATION USING TIMER2/2



Work around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPBUF with the data to transmit and then turn Timer2 back on. Refer to Example 4 for sample code.

EXAMPLE 4: AVOIDING THE INITIAL SHORT SCK PULSE

```
LOOP BTFSS  SSPSTAT, BF     ;Data received?
                            ;(Xmit complete?)
     BRA    LOOP            ;No
     MOVF   SSPBUF, W       ;W = SSPBUF
     MOVWF  RXDATA          ;Save in user RAM
     MOVF   TXDATA, W       ;W = TXDATA
     BCF    T2CON, TMR2ON   ;Timer2 off
     CLRF   TMR2            ;Clear Timer2
     MOVWF  SSPBUF          ;Xmit New data
     BSF    T2CON, TMR2ON   ;Timer2 on
```

33. Module: Timer1 (Asynchronous Counter)

When writing to the TMR1H register, under specific conditions, it is possible that the TMR1L register will miss a count while connected to the external oscillator via the T1OSO and T1OSI pins.

When Timer1 is started, the circuitry looks for a falling edge before a rising edge can increment the counter. Writing to the TMR1H register is similar to starting Timer1; therefore, the former logic stated applies any time the TMR1H register is written. If the TMR1H register is not completely written to during the high pulse of the external clock, then the TMR1L register will miss a count due to the circuit operation stated previously. The high pulse of a 32.768 kHz external clock crystal yields a 15.25 µs window for the write to TMR1H to occur. The amount of instructions that can be executed within this window is frequency dependent, as shown in Table 4 below.

Work around

Operating Conditions: FOSC ≥ 4 MHz, no wake-ups from Sleep, Timer1 interrupt enabled, global interrupts enabled.

The code excerpts in Example 5 and Example 6 show how the TMR1H register can be updated while the external clock (32.768 kHz) is still on its high pulse.

The importance of the code examples is that the **bold** instructions are executed within the first 15.25 µs high pulse on the external clock after the Timer1 overflow occurs. This will allow the TMR1L register to increment correctly.

TABLE 4: FREQUENCY DEPENDENT INSTRUCTION EXECUTION AMOUNTS

FOSC	TCY (µs)	TCY within 15.25 µs
1 MHz	4	3.81
2 MHz	2	7.63
4 MHz	1	15.25
8 MHz	0.5	30.5
16 MHz	0.25	61
20 MHz	0.2	76.25
40 MHz	0.1	152.5

EXAMPLE 5: PIC18 HIGH PRIORITY INTERRUPT SERVICE ROUTINE

```
ISR @ 0x0008                    ; (3-4Tcy), fixed interrupt latency

    BRA     HIGHINT             ; (2Tcy), go to high priority interrupt routine

HIGHINT
    BTFSC   PIR1, TMR1IF        ; (1Tcy), did a Timer1 overflow occur?
    BSF     TMR1H, 7            ; (1Tcy) Yes, reload for a 1 second overflow

    RETFIE  FAST
```

Total = 7-8 TCY (if Timer1 overflow occurred)

EXAMPLE 6: PIC18 LOW PRIORITY INTERRUPT SERVICE ROUTINE

```
ISR @ 0x0018                        ; (3-4Tcy), fixed interrupt latency

    MOVFF   STATUS, STATUS_TEMP     ; (2Tcy), save STATUS register
    MOVFF   WREG, WREG_TEMP         ; (2Tcy), save working register, refer to note 1
    MOVFF   BSR, BSR_TEMP           ; (2Tcy), save BSR register, refer to note 1

    BTFSS   PIR1, TMR1IF            ; (2Tcy), did a Timer1 overflow occur?
    BRA     EXIT                    ; No
    BSF     TMR1H, 7                ; (1Tcy) Yes, reload for a 1 second overflow

EXIT
    MOVFF   BSR_TEMP, BSR           ;restore BSR register, refer to note 1
    MOVFF   WREG_TEMP, WREG         ;restore working register, refer to note 1
    MOVFF   STATUS_TEMP, STATUS     ;restore STATUS register
    RETFIE
```

Total = 12-13 TCY (if Timer1 overflow occurred)

Note: These instructions are required based on the function of the ISR. If the only code in the ISR is to reload Timer1, then they are not required, but may be required if additional code is added.

REVISION HISTORY

Rev A Document (9/2004)
First revision of this document which includes silicon issues 1-6 (ECCP), 7-11 (MSSP), 12 (ECCP and CCP), 13 (A/D), 14-15 (Timer1/Timer3) and 16 (BOD/HLVD).

Rev B Document (11/2004)
Changes made to silicon issue 7 (MSSP), 9 (MSSP) and 10 (MSSP). Added silicon issue 17 (EUSART), 18 (Interrupts), 19 (ECCP) and 20 (Timer1/Timer3).

Rev C Document (2/2005)
Added Date Code information to all issues, updated text and reordered issues for clarity. Issues in this revision are: 1-5 (MSSP), 6-8, 10-12, 14-15 (ECCP), 9, 13 (ECCP and CCP), 16 (A/D), 17 (BOD), 18-19 (EUSART), 20-22 (Timer1/Timer3) and 23 (Interrupts).

Rev D Document (12/2005)
Updated issues 4 (MSSP), 9 (ECCP and CCP) and 23 (Interrupts). Added issues 24-26 (EUSART), 27-31 (MSSP), 32 (MSSP – SPI Mode) and 33 (Timer1 – Asynchronous Counter).

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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