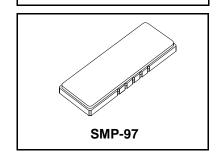
## **Preliminary**



SF1111A

## 160 MHz

# **SAW Filter**



- Designed for CDMA2000 BTS Applications
- Simple External Impedance Matching
- Hermetic SMP-97 Surface-Mount Case
- Unbalanced Input and Output
- Complies with Directive 2002/95/EC (RoHS)



#### **Absolute Maximum Ratings**

Rating	Value	Units
Maximum Incident Power in Passband	+10	dBm
Max. DC voltage between any 2 terminals	30	VDC
Storage Temperature Range	-40 to +85	°C
Suitable for lead-free soldering - Max. Soldering Profile	260°C	for 30 s

#### **Electrical Characteristics**

Characteristic			Notes	Min	Тур	Max	Units
Nominal Center Frequency			1		160.000		MHz
Passband	Insertion Loss at fc	IL			9	11.0	dB
	1.5 dB Passband	BW <sub>1.5</sub>	1, 2	±590			kHz
3 db Passband		BW <sub>3</sub>			±750		KITZ
Amplitude Ripple over fc±470 kHz			•		0.7	1.0	dB
	Phase Linearity over fc ±590 kHz				2	5	°rms
Rejection	fc-10.0 to fc-1.25 and fc+1.25 to fc+10.0 MHz		1, 2, 3	40			dB
	fc-20 to fc-10.0 and fc+10.0 to fc+20 MHz		1, 2, 3	50			uБ
Operating Temperature Range		T <sub>A</sub>	1	-20		+70	°C

Impedance Matching to 50 $\Omega$ Unbalanced	External L-C
Case Style	SMP-97 24.6 x 9 mm Nominal Footprint
Lid Symbolization (YY = year, WW = week)	RFM SF1111A YYWW

#### Notes:

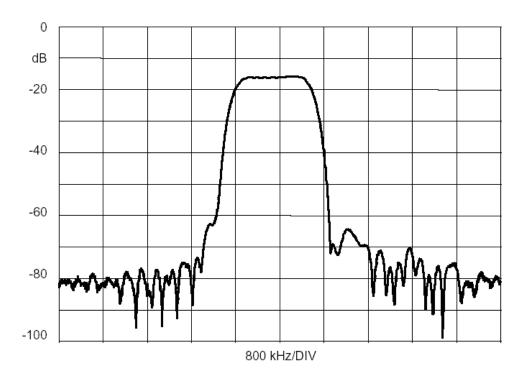
- Unless noted otherwise, all specifications apply over the operating temperature range with filter soldered to the specified demonstration board with impedance matching to 50  $\Omega$ and measured with 50  $\Omega$  network analyzer.
- Unless noted otherwise, all frequency specifications are referenced to the nominal center 2. frequency, fc.
- Rejection is measured as attenuation below the minimum IL point in the passband. Rejection in final user application is dependent on PCB layout and external impedance matching design. See Application Note No. 42 for details.
- "LRIP" or "L" after the part number indicates "low rate initial production" and "ENG" or "E" indicates "engineering prototypes."
- The design, manufacturing process, and specifications of this filter are subject to change.
- Either Port 1 or Port 2 may be used for either input or output in the design. However, impedances and impedance matching may vary between Port 1 and Port 2, so that the filter must always be installed in one direction per the circuit design.
- US and international patents may apply. 7.
- Electrostatic Sensitive Device. Observe precautions for handling.

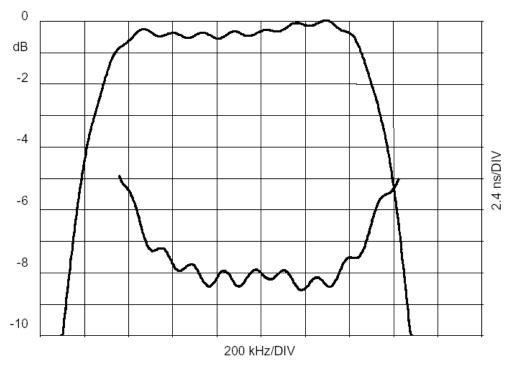


#### **Electrical Connections**

Connection	Terminals
Port 1 Hot	10
Port 1 Gnd Return	1
Port 2 Hot	5
Port 2 Gnd Return	6
Case Ground	All others

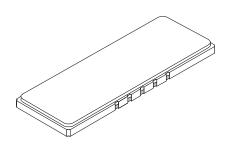
SF1111A-121504





### **SMP-97 Case**

# 10-Terminal Ceramic Surface-Mount Case 24.6 x 9 mm Nominal Footprint



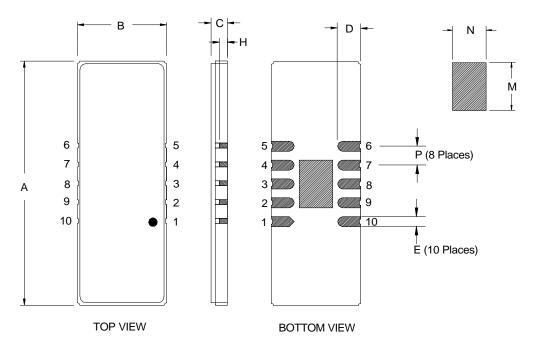
#### **Case Dimensions**

Dimension		mm			Inches	
Dilliension	Min	Nom	Max	Min	Nom	Max
Α	24.41	24.64	24.94	0.961	0.970	0.982
В	8.80	8.99	9.30	0.349	0.354	0.366
С		1.75	2.00		0.069	0.079
D		2.29			0.090	
E		1.02			0.040	
Н		1.0			0.039	
М		4.83			0.190	
N		3.40			0.134	
Р		1.905			0.075	

Materials				
Solder Pad Termination	Au plating 30 - 60 ulnches (76.2-152 uM) over 80- 200 ulnches (203-508 uM) Ni.			
Lid	Fe-Ni-Co Alloy Electroless Nickel Plate (8-11% Phosphorus) 100-200 ulnches Thick			
Body	Al <sub>2</sub> O <sub>3</sub> Ceramic			
Pb Free				

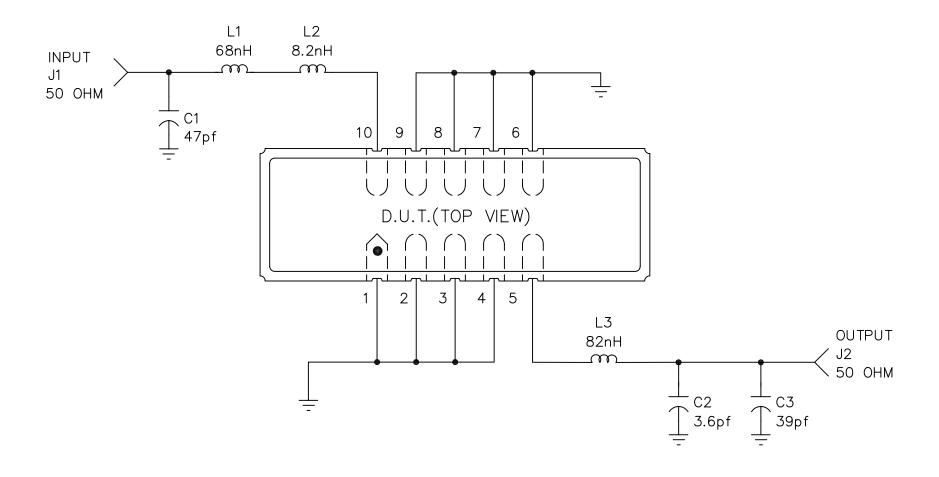
#### **Electrical Connections**

Connection		Terminals
Port 1	Input or Return	10
	Return or Input	1
Port 2	Output or Return	5
	Return or Output	6
	Ground	All others
Single E	Ended Operation	Return is ground
Differential Operation		Return is hot



RF Monolithics, Inc. Phone: (972) 233-2903 Fax: (972) 387-9148 RFM Europe Phone: 44 1963 251383 Fax: 44 1963 251510 ©2001 by RF Monolithics, Inc. The stylized RFM logo are registered trademarks of RF Monolithics, Inc.

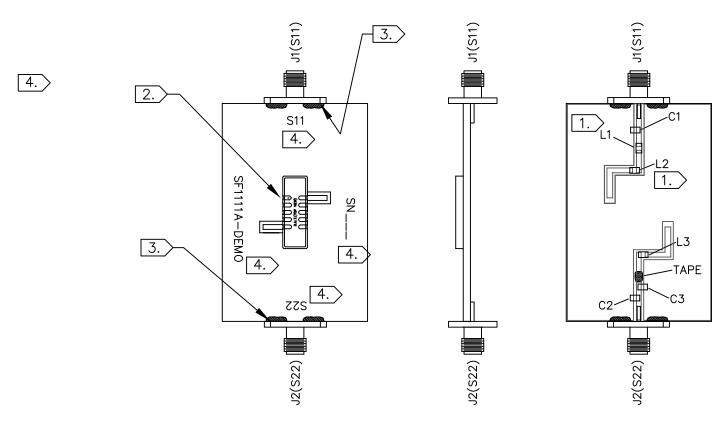
REV	ECN NO.	DESCRIPTION	DATE
Α	8252	NEW DESIGN	05nov99



DRAWN BY/DATE: J.F.Ch	topherson 02nov99	TITLE:	ASSEME	3LY	DIAGRAM, SF1111A	(DEN	10)
RF Monolithics, DALLAS, TEXAS 75244	C. CHECKED/APPROVED	size A	code ident 2U874	DWG. NO.	SF1111A-000	rev A	SHEET 1/4

#### NOTES:

- 1. NOTE PROPER ORIENTATION OF INDUCTOR PAIRS L1 & L2. THEY ARE TO BE POSITIONED 90° TO EACH OTHER.
- 2. SOLDER SURFACE MOUNT PACKAGE TO TEST SIDE OF PCB. SOLDER 10 PLACES AS SHOWN. NOTE PIN 1 INDICATOR.
- 3. SOLDER CONNECTOR FLANGES ON BOTH SIDES OF PCB.
- 4. MARK USING LABEL MAKER.



RF	Monolithics, Inc	٠
	DALLAS, TEXAS 75244	

SIZE	CODE IDEN
А	2U874

