



N-Channel 100-V (D-S) MOSFET

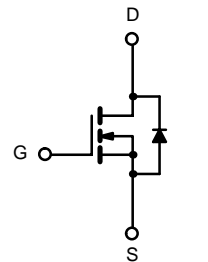
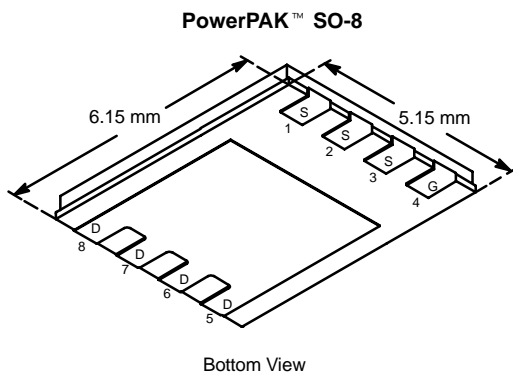
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.034 @ $V_{GS} = 10$ V	7.8
	0.040 @ $V_{GS} = 6.0$ V	7.2

FEATURES

- TrenchFET® Power MOSFETS
- New Low Thermal Resistance PowerPAK™ Package with Low 1.07-mm Profile
- PWM Optimized for Fast Switching

APPLICATIONS

- Primary Side Switch for High Density DC/DC
- Telecom/Server 48-V, Full-/Half-Bridge DC/DC
- Industrial and 42-V Automotive



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	100		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	7.8	5.0	A
		$T_A = 85^\circ\text{C}$	5.7	3.6	
Pulsed Drain Current	I_{DM}	30			
Avalanche Current	I_{AS}	25		mJ	
Single Avalanche Energy (Duty Cycle $\leq 1\%$)		E_{AS}	31		
Continuous Source Current (Diode Conduction) ^a	I_S	4.0	1.6	A	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	4.8	1.9	W
		$T_A = 85^\circ\text{C}$	2.6	1.0	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	21	26	$^\circ\text{C/W}$
		Steady State	55	65	
Maximum Junction-to-Case (Drain)	R_{thJC}	1.6	2		

Notes

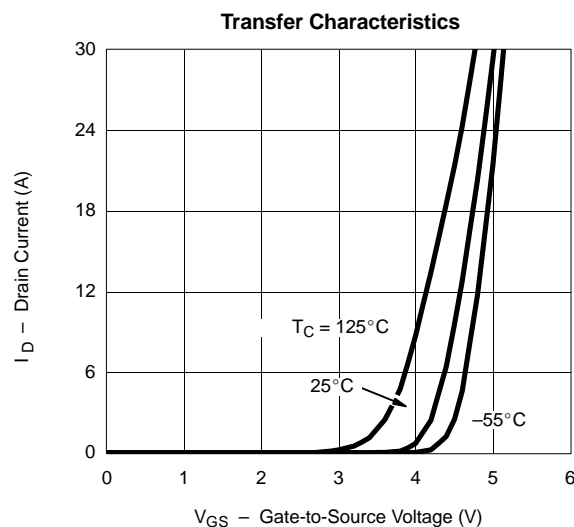
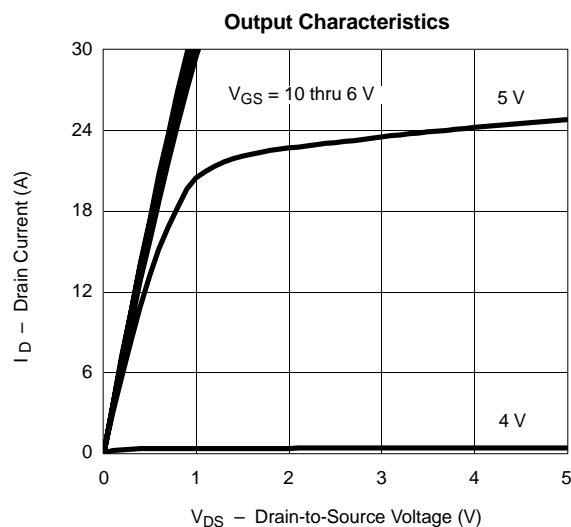
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V			1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 85 °C			20	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 7.8 A		0.028	0.034	Ω
		V _{GS} = 6.0 V, I _D = 7.2 A		0.032	0.040	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 7.8 A		25		S
Diode Forward Voltage ^a	V _{SD}	I _S = 4 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 7.8 A		24	30	nC
Gate-Source Charge	Q _{gs}			7.6		
Gate-Drain Charge	Q _{gd}			5.4		
Gate Resistance	R _G			1.25		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 50 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		16	30	ns
Rise Time	t _r			10	20	
Turn-Off Delay Time	t _{d(off)}			35	70	
Fall Time	t _f			20	40	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 4 A, di/dt = 100 A/μs		50	80	

Notes

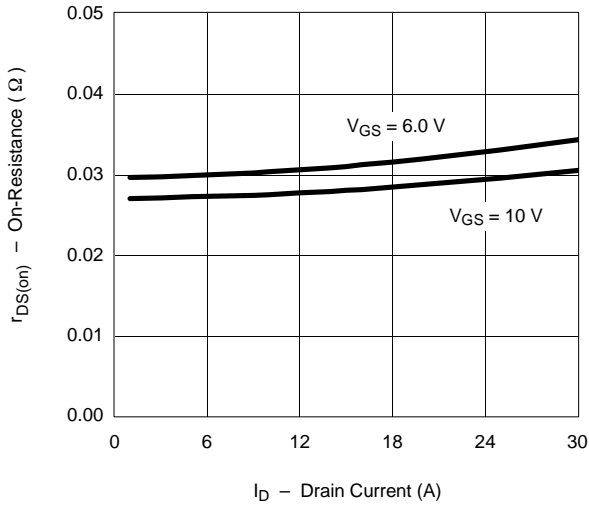
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

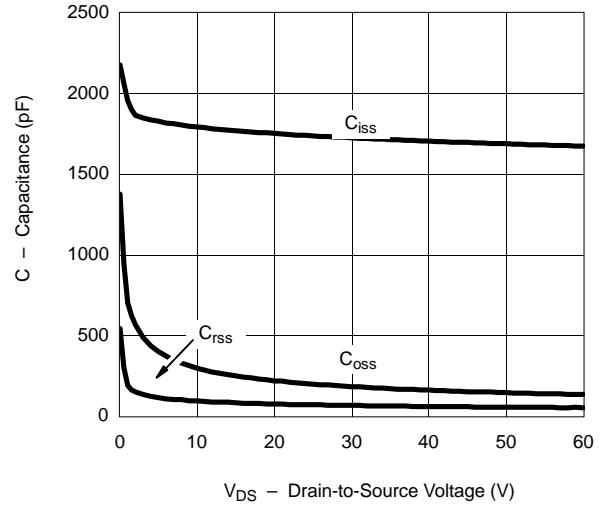


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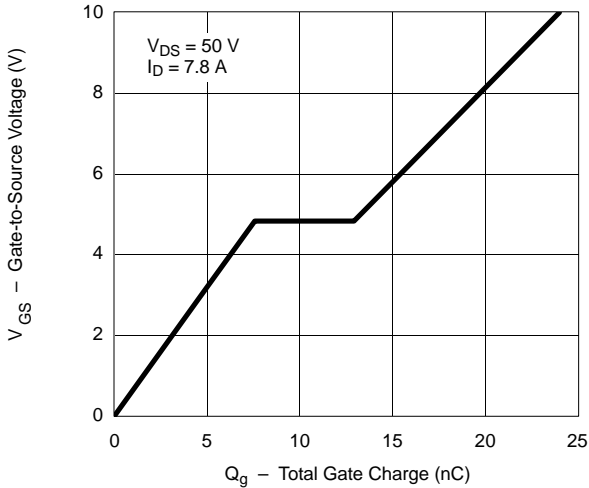
On-Resistance vs. Drain Current



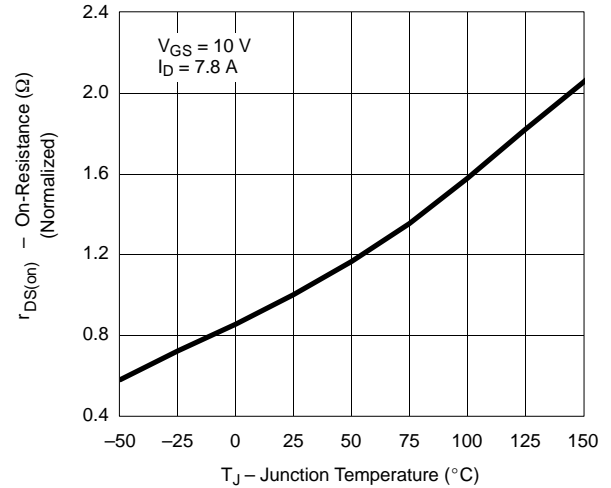
Capacitance



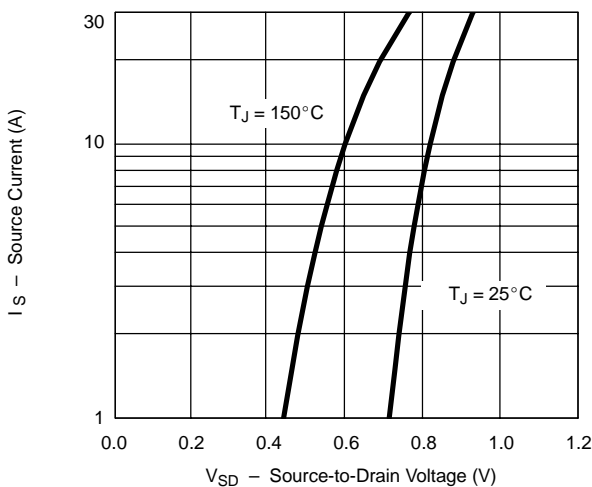
Gate Charge



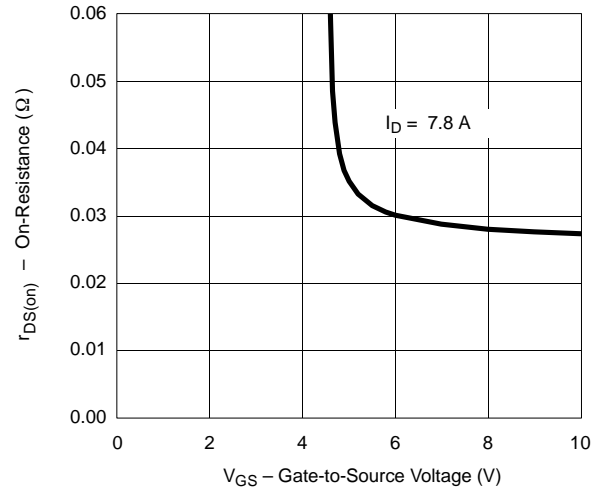
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

