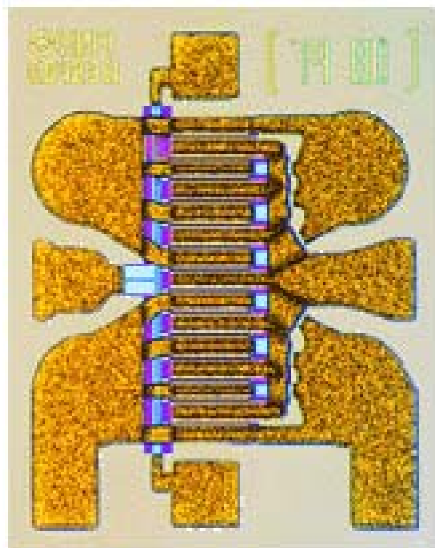
TriQuint SEMICONDUCTOR®

DC - 12 GHz Discrete HFET TGF4230-SCC



Key Features and Performance

- Nominal Pout of 28.5 dBm at 8.5 GHz
- Nominal Gain of 10.0 dB at 8.5 GHz
- Nominal PAE of 55 % at 8.5 GHz
- 1200 µm HFET
- 0.61 x 0.74 x 0.1 mm (0.024 x 0.029 x 0.004 in)
- Bias at 8 Volts, 96 mA

Primary Applications

- Cellular Base Stations
- High dynamic-range LNAs
- Military and Space

Description

The TriQuint TGF4230-SCC is a single gate 1.2 mm Discrete GaAs Heterostructure Field Effect Transistor (HFET) designed for high-efficiency power applications up to 12 GHz in Class A and Class AB operation.

Bond-pad and backside metalization is gold plated for compatibility with eutectic alloy attach methods as well as thermocompression and thermosonic wire-bonding processes. The TGF4230-SCC is readily assembled using automatic equipment.

For an Application Note on the use of HFETs, refer to the TriQuint website for the Millimeter Wave Division.

TABLE I
MAXIMUM RATINGS

SYMBOL	PARAMETER 1/	VALUE	NOTES
V_{DS}	Drain to Source Voltage	12 V	
V_{GS}	Gate to Source Voltage Range	0 to -5.0 Volts	
P_D	Power Dissipation	See Thermal Data	
T_{CH}	Operating Channel Temperature	150°C	2/, 3/
T_{STG}	Storage Temperature	-65 to 150°C	
T_M	Mounting Temperature (30 seconds)	320°C	

1/ These ratings represent the maximum values for this device. Stresses beyond those listed under "Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "DC Probe Characteristics" and "Electrical Characteristics" is not implied. Exposure to maximum rated conditions for extended periods may affect device reliability.

2/ Junction temperature will directly affect the device Mean Time to Failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

3/ These ratings apply to each individual FET

TABLE II
DC PROBE CHARACTERISTICS
(T_A = 25 °C, Nominal)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Note
I_{DSS}	Saturated Drain Current	--	294	--	mA	1/
G_M	Transconductance	--	198	--	mS	1/
V_P	Pinch-off Voltage	1	1.85	3	V	2/
V_{BGS}	Breakdown Voltage Gate-Source	17	22	30	V	2/
V_{BGD}	Breakdown Voltage Gate-Drain	17	22	30	V	2/

1/ Total for two FETS
2/ V_P, V_{BGS}, and V_{BGD} are negative.

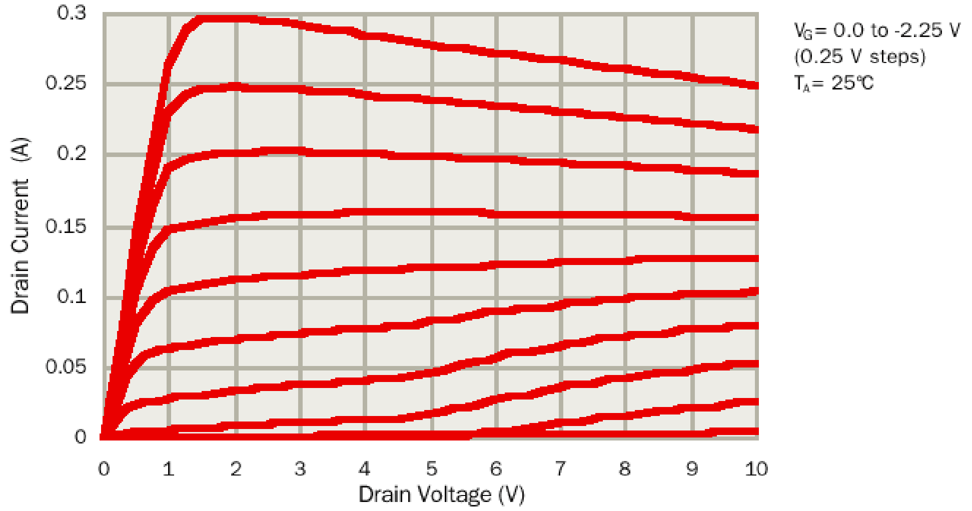
TABLE III
ELECTRICAL CHARACTERISTICS
(T_A = 25 °C, Nominal)
Bias Conditions: Vd = 8 V, Id = 50 mA +/- 10%, @ 8.5 GHz

Symbol	Parameter	Typical	Unit
Pout	Output Power	28.5	dBm
Gp	Power Gain	10	dB
PAE	Power Added Efficiency	55	%

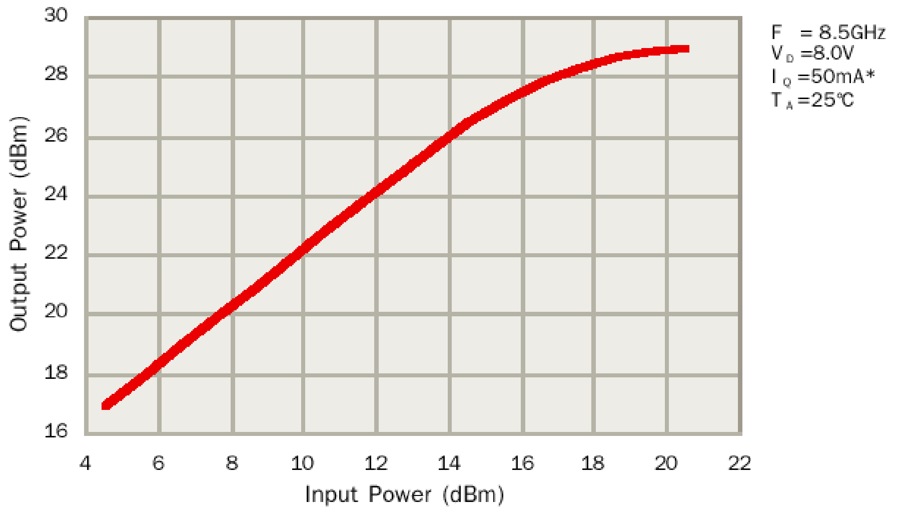
Note: The recommended bias current for HFETs is 80 mA/mm. For this 1.2 mm HFET IQ is 96 mA.

TYPICAL PERFORMANCE

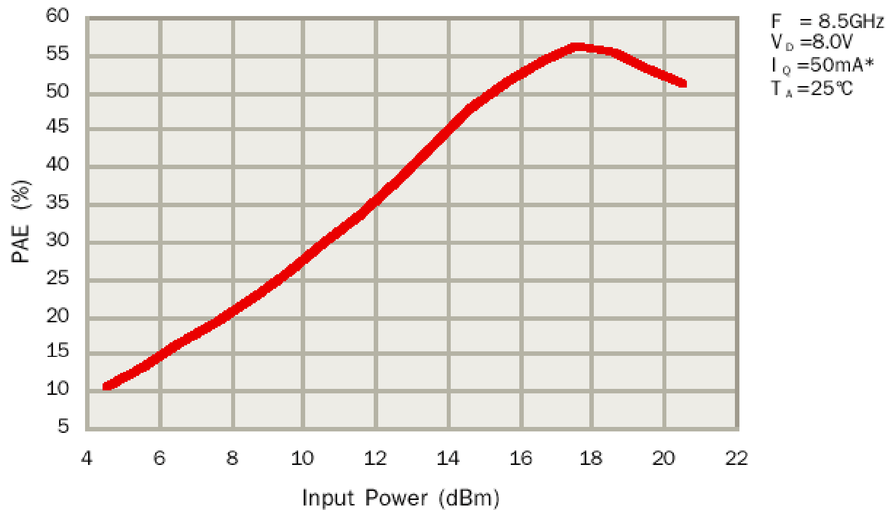
EXAMPLE OF DC I-V CURVES



OUTPUT POWER VS. INPUT POWER

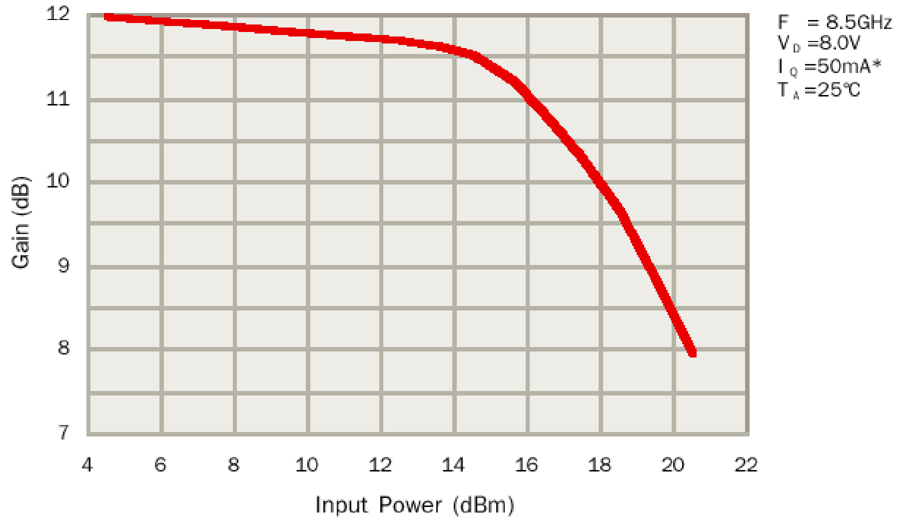


POWER ADDED EFFICIENCY VS. INPUT POWER

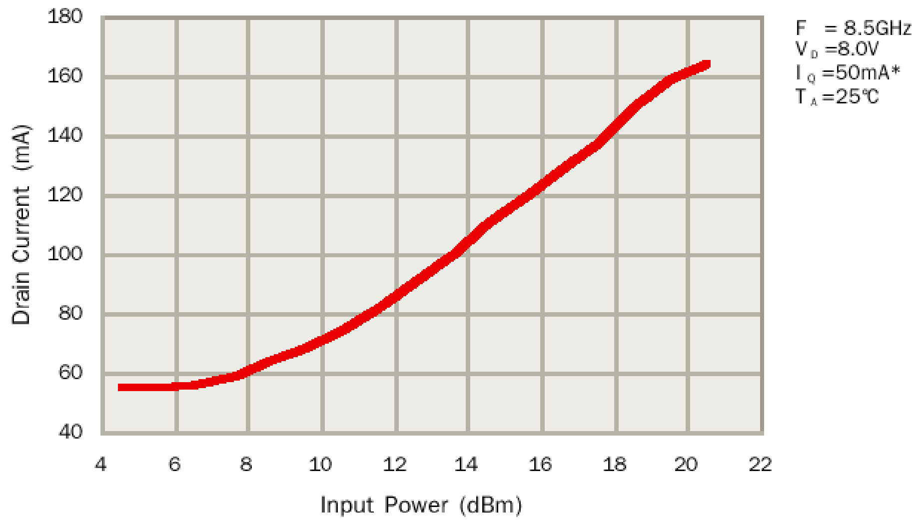


TYPICAL PERFORMANCE

GAIN VS. INPUT POWER



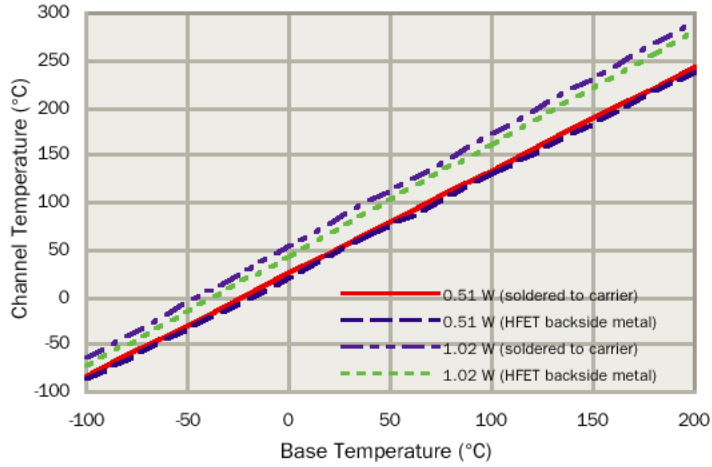
DRAIN CURRENT VS. INPUT POWER



* Note: I_Q is defined as the drain current before application of RF signal at the input.

THERMAL INFORMATION

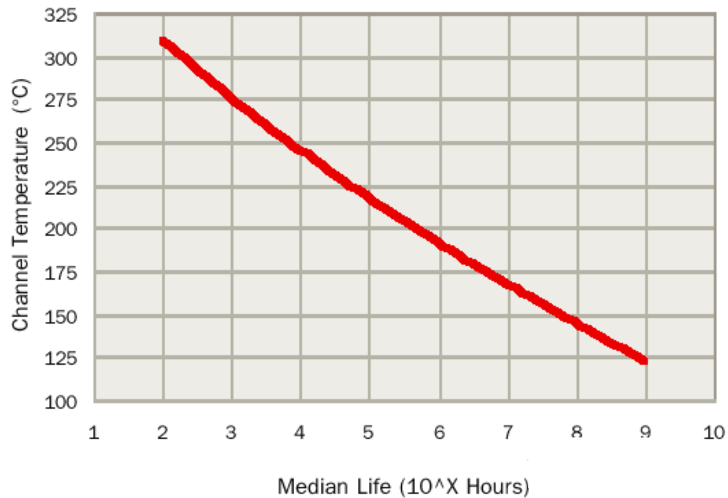
PREDICTED CHANNEL TEMPERATURE VS. BASE TEMPERATURE at 0.51 W and 1.02 W dissipated power



Case 1: Base temperature at backside of carrier (with 38 µm AuSn solder attach to 0.5 mm CuMo Carrier)

Case 2: Base temperature at backside of 1.2 mm HFET.

HFET CHANNEL TEMPERATURE VS. MEDIAN LIFE

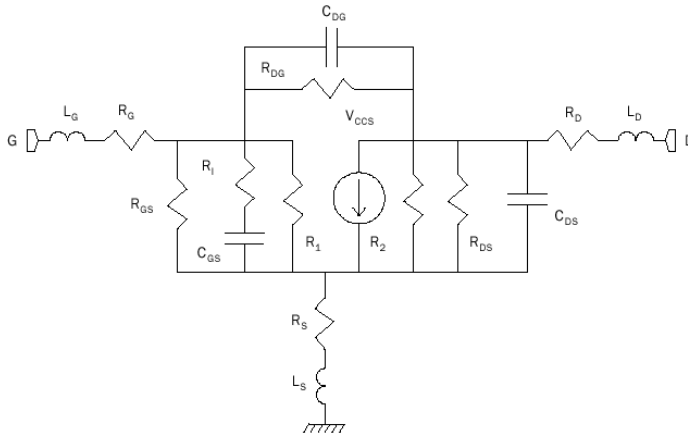


MODELED S-PARAMETERS

Frequency (GHz)	S_{11} MAG	S_{11} ANG(°)	S_{21} MAG	S_{21} ANG(°)	S_{12} MAG	S_{12} ANG(°)	S_{22} MAG	S_{22} ANG(°)
0.5	0.985	-29.88	8.095	161.49	0.021	72.66	0.343	-22.22
1.0	0.959	-56.20	7.297	145.18	0.038	58.80	0.328	-41.75
1.5	0.931	-77.47	6.368	131.86	0.050	47.65	0.312	-57.46
2.0	0.908	-94.02	5.512	121.22	0.057	39.12	0.301	-69.57
2.5	0.891	-106.82	4.791	112.62	0.062	32.60	0.295	-78.80
3.0	0.880	-116.82	4.202	105.49	0.065	27.55	0.294	-85.89
3.5	0.871	-124.76	3.723	99.42	0.067	23.56	0.297	-91.41
4.0	0.865	-131.19	3.330	94.11	0.068	20.34	0.302	-95.80
4.5	0.861	-136.48	3.004	89.37	0.069	17.70	0.309	-99.38
5.0	0.858	-140.92	2.732	85.06	0.069	15.51	0.319	-102.37
5.5	0.856	-144.69	2.501	81.09	0.069	13.67	0.329	-104.94
6.0	0.855	-147.94	2.304	77.39	0.068	12.12	0.340	-107.18
6.5	0.854	-150.78	2.133	73.90	0.068	10.82	0.352	-109.19
7.0	0.854	-153.29	1.984	70.59	0.067	9.72	0.364	-111.03
7.5	0.854	-155.53	1.852	67.43	0.066	8.80	0.377	-112.73
8.0	0.855	-157.54	1.736	64.40	0.065	8.05	0.390	-114.32
8.5	0.855	-159.37	1.632	61.49	0.065	7.45	0.404	-115.84
9.0	0.856	-161.04	1.539	58.67	0.064	7.00	0.417	-117.29
9.5	0.857	-162.58	1.455	55.95	0.063	6.68	0.430	-118.68
10.0	0.858	-164.01	1.378	53.30	0.061	6.49	0.444	-120.03
10.5	0.859	-165.34	1.308	50.73	0.060	6.43	0.457	-121.35
11.0	0.860	-166.58	1.244	48.23	0.059	6.51	0.470	-122.63
11.5	0.862	-167.76	1.186	45.79	0.058	6.71	0.483	-123.89
12.0	0.863	-168.87	1.131	43.41	0.057	7.05	0.496	-125.11
12.5	0.864	-169.93	1.081	41.09	0.056	7.52	0.509	-126.32
13.0	0.866	-170.94	1.034	38.83	0.055	8.12	0.521	-127.51
13.5	0.867	-171.91	0.991	36.62	0.053	8.86	0.534	-128.68
14.0	0.869	-172.84	0.950	34.46	0.052	9.74	0.546	-129.82

V_{DS} = 8.0 V and 30% I_{DSS} at T = 25°C

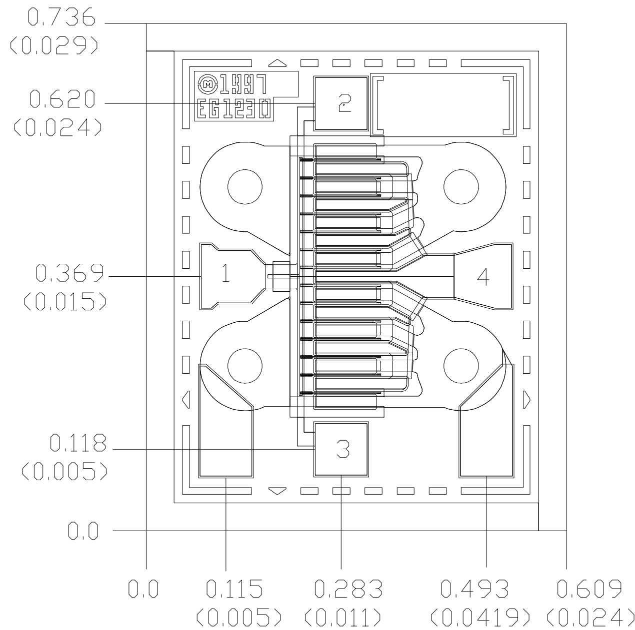
LINEAR MODEL



V_{DS} = 8.0 V and 30% I_{DSS} at T = 25°C

FET Elements	R_{DG} = 204000 Ω	**VCCS Parameters**
L_G = 0.0421nH	R_S = 0.4 Ω	M = 132.9 mS
R_G = 0.43 Ω	L_S = 0.015 nH	A = 0
R_{GS} = 81700 Ω	R_{DS} = 98.01 Ω	R1 = 1E19 Ω
R_I = 1.21Ω	C_{DS} = 0.25325 pF	R2 = 1E19 Ω
C_{GS} = 1.21 pF	R_D = 0.66 Ω	F = 0
C_{DG} = 0.1004 pF	L_D = 0.022 nH	T = 5.49 pS

Mechanical Drawing



Units: millimeters (inches)
Thickness: 0.100 (0.004)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.051 (0.002)

GND IS BACKSIDE OF MMIC

Bond pad #1 (gate) 0.072 x 0.075 (0.003 x 0.003)
Bond pad #2 (gate)* 0.075 x 0.075 (0.003 x 0.003)
Bond pad #3 (gate)* 0.075 x 0.075 (0.003 x 0.003)
Bond pad #4 (drain) 0.083 x 0.077 (0.003 x 0.003)

Minimum connections to Bond pads 1 and 4. Sources are connected to backside metalization.

*Alternate gate pads used for paralleling TGF4230s or for multiple gate wires.

NOTE: Gate bias supplies should be designed to sink or source gate current. The magnitude and direction of the gate current is a function of bias point, load impedence, and drive level.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300 °C for 30 sec
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200 °C.

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Note: Die are shipped in gel pack unless otherwise specified.