

**SWITCHING**  
**N- AND P-CHANNEL POWER MOS FET**

**DESCRIPTION**

The  $\mu$ PA1793 is N- and P-Channel MOS Field Effect Transistors designed for Motor Drive application.

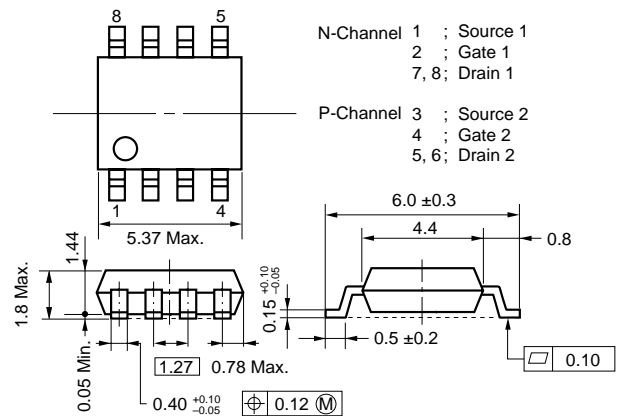
**FEATURES**

- Low on-state resistance  
 N-Channel  $R_{DS(on)1} = 69 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = 4.5 \text{ V}$ ,  $I_D = 1.5 \text{ A}$ )  
 $R_{DS(on)2} = 72 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = 4.0 \text{ V}$ ,  $I_D = 1.5 \text{ A}$ )  
 $R_{DS(on)3} = 107 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = 2.5 \text{ V}$ ,  $I_D = 1.0 \text{ A}$ )  
 P-Channel  $R_{DS(on)1} = 115 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = -4.5 \text{ V}$ ,  $I_D = -1.5 \text{ A}$ )  
 $R_{DS(on)2} = 120 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = -4.0 \text{ V}$ ,  $I_D = -1.5 \text{ A}$ )  
 $R_{DS(on)3} = 190 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = -2.5 \text{ V}$ ,  $I_D = -1.0 \text{ A}$ )
- Low input capacitance  
 N-Channel  $C_{iss} = 160 \text{ pF TYP.}$   
 P-Channel  $C_{iss} = 370 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

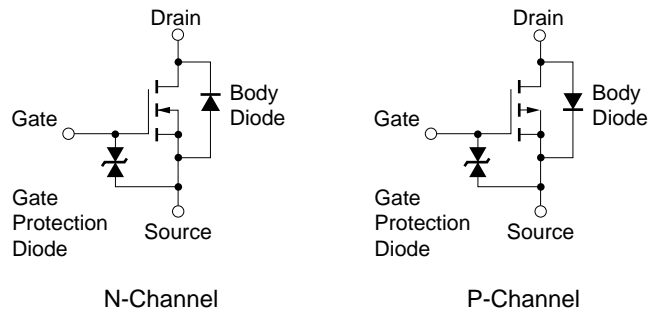
**ORDERING INFORMATION**

PART NUMBER	PACKAGE
$\mu$ PA1793G	Power SOP8

**PACKAGE DRAWING (Unit: mm)**



**EQUIVALENT CIRCUIT**



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version. Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C, All terminals are connected.)**

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	20	-20	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	± 12	∓ 12	V
Drain Current (DC)	I <sub>D(DC)</sub>	± 3	∓ 3	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	± 12	∓ 12	A
Total Power Dissipation (1 unit) <sup>Note2</sup>	P <sub>T</sub>	1.7		W
Total Power Dissipation (2 units) <sup>Note2</sup>	P <sub>T</sub>	2.0		W
Channel Temperature	T <sub>ch</sub>	150		°C
Storage Temperature	T <sub>stg</sub>	-55 to +150		°C

**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%

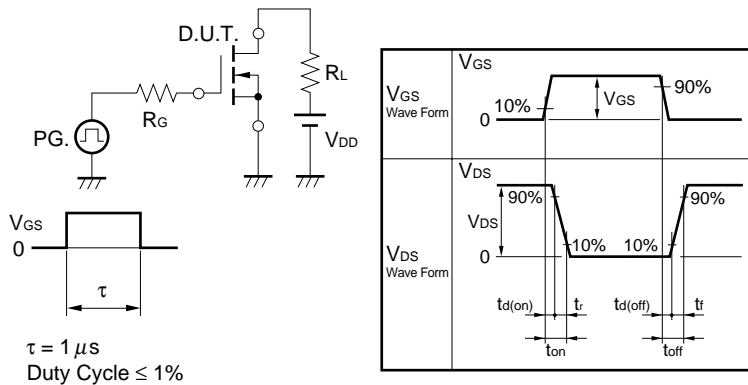
**2.** Mounted on ceramic substrate of 5500 mm<sup>2</sup> × 2.2 mm, T<sub>A</sub> = 25°C

**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, All terminals are connected.)**

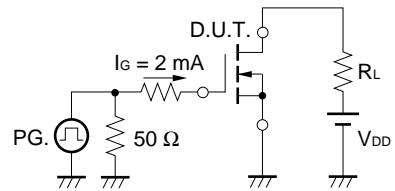
**A) N-Channel**

Characteristic	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±12 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	0.5	1.0	1.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.5 A	1.0			S
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1.5 A		55	69	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 1.5 A		57	72	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 1.0 A		78	107	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		160		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		60		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		40		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, I <sub>D</sub> = 1.5 A		17		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 4.0 V		50		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		86		ns
Fall Time	t <sub>f</sub>			80		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 16 V		3.1		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 4.0 V		0.7		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 3.0 A		1.4		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 3.0 A, V <sub>GS</sub> = 0 V		0.86		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 3 A, V <sub>GS</sub> = 0 V		70		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 50 A/μs		12		nC

**TEST CIRCUIT 1 SWITCHING TIME**



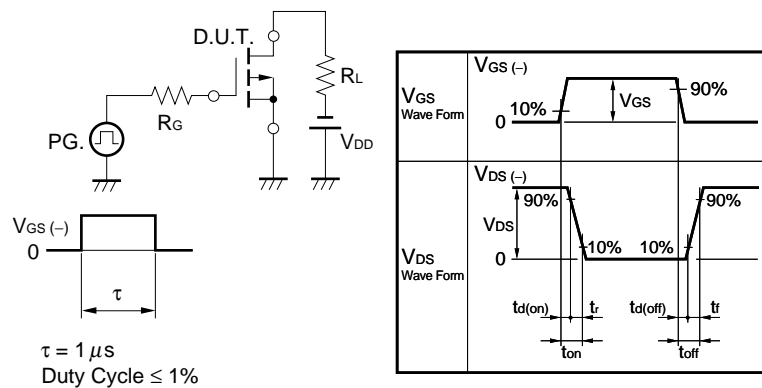
**TEST CIRCUIT 2 GATE CHARGE**



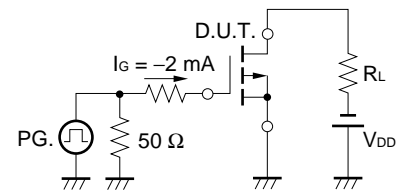
**B) P-Channel**

Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			-10	$\mu\text{A}$
Gate Leakage Current	$I_{GSS}$	$V_{GS} = \mp 12\text{ V}, V_{DS} = 0\text{ V}$			$\mp 10$	$\mu\text{A}$
Gate Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$	-0.5	-1.0	-1.5	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -1.5\text{ A}$	1.0			S
Drain to Source On-state Resistance	$R_{DS(on)1}$	$V_{GS} = -4.5\text{ V}, I_D = -1.5\text{ A}$		75	115	$\text{m}\Omega$
	$R_{DS(on)2}$	$V_{GS} = -4.0\text{ V}, I_D = -1.5\text{ A}$		80	120	$\text{m}\Omega$
	$R_{DS(on)3}$	$V_{GS} = -2.5\text{ V}, I_D = -1.0\text{ A}$		116	190	$\text{m}\Omega$
Input Capacitance	$C_{iss}$	$V_{DS} = -10\text{ V}$		370		pF
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$		110		pF
Reverse Transfer Capacitance	$C_{rss}$	$f = 1\text{ MHz}$		40		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, I_D = -1.5\text{ A}$		120		ns
Rise Time	$t_r$	$V_{GS} = -4.0\text{ V}$		260		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G = 10\ \Omega$		410		ns
Fall Time	$t_f$			360		ns
Total Gate Charge	$Q_G$	$V_{DD} = -10\text{ V}$		3.4		nC
Gate to Source Charge	$Q_{GS}$	$V_{GS} = -4.0\text{ V}$		1.3		nC
Gate to Drain Charge	$Q_{GD}$	$I_D = -3.0\text{ A}$		1.6		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	$I_F = 3.0\text{ A}, V_{GS} = 0\text{ V}$		0.86		V
Reverse Recovery Time	$t_{rr}$	$I_F = 3\text{ A}, V_{GS} = 0\text{ V}$		24		ns
Reverse Recovery Charge	$Q_{rr}$	$di/dt = 10\text{ A}/\mu\text{s}$		1.5		nC

**TEST CIRCUIT 1 SWITCHING TIME**



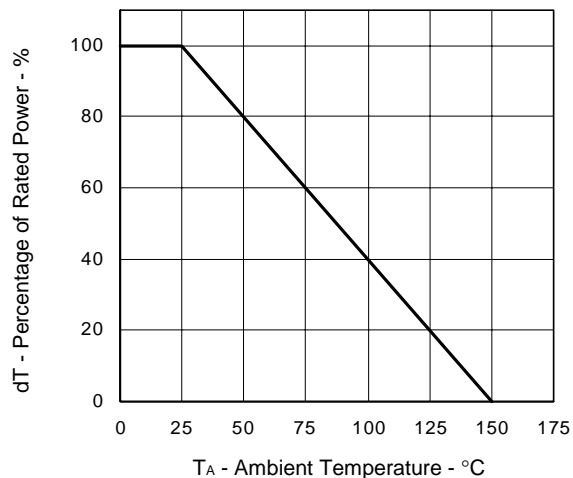
**TEST CIRCUIT 2 GATE CHARGE**



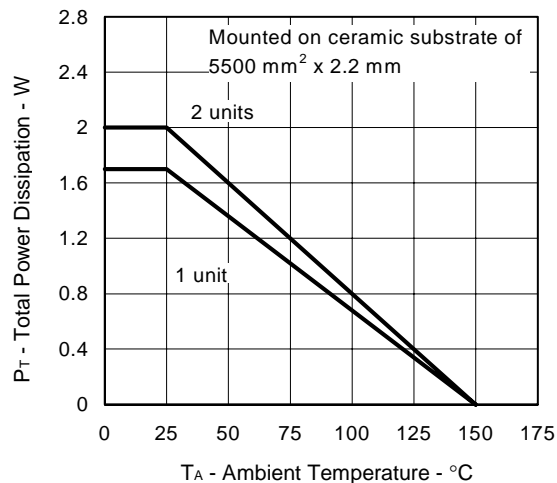
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

A) N-Channel

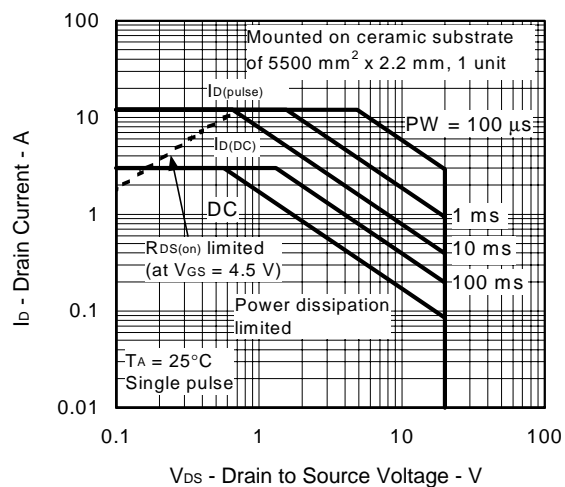
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



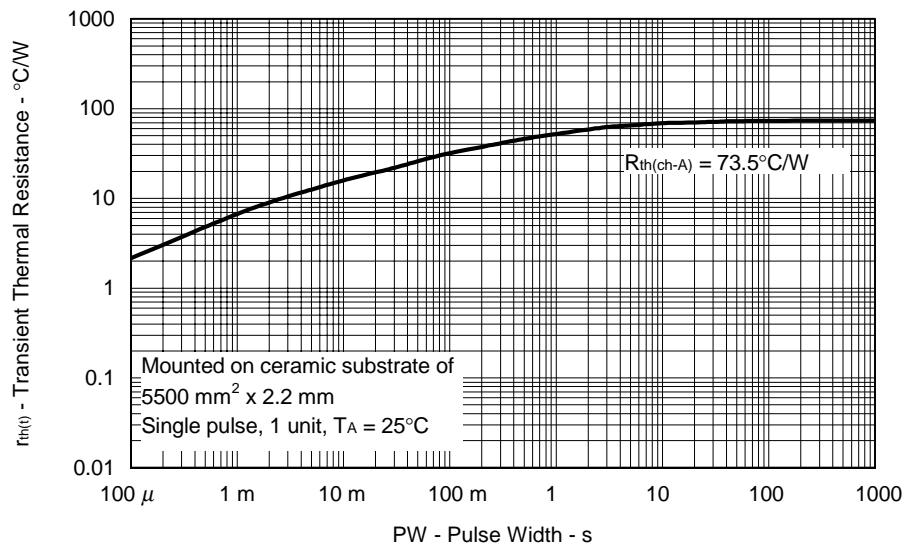
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



FORWARD BIAS SAFE OPERATING AREA

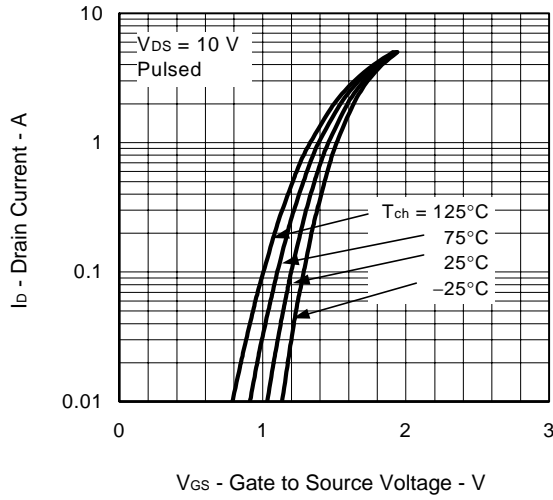


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

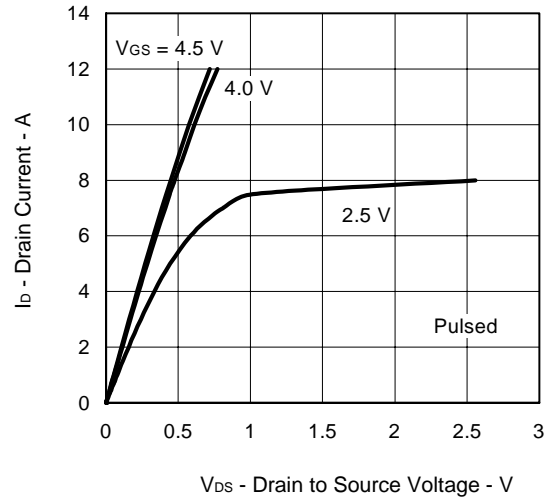


A) N-Channel

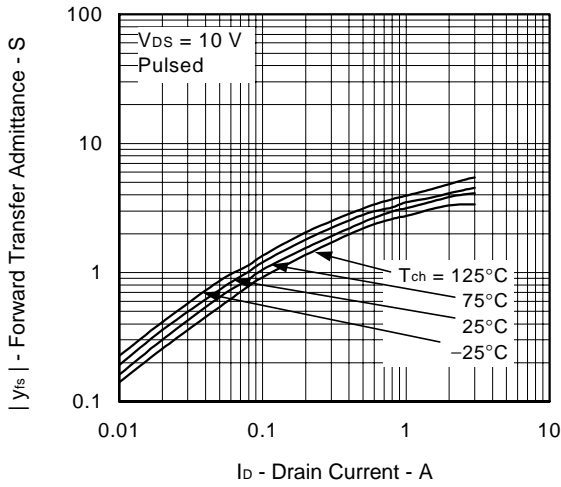
FORWARD TRANSFER CHARACTERISTICS



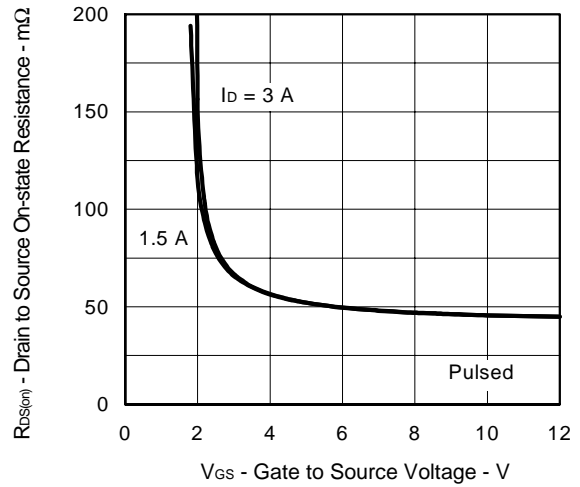
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



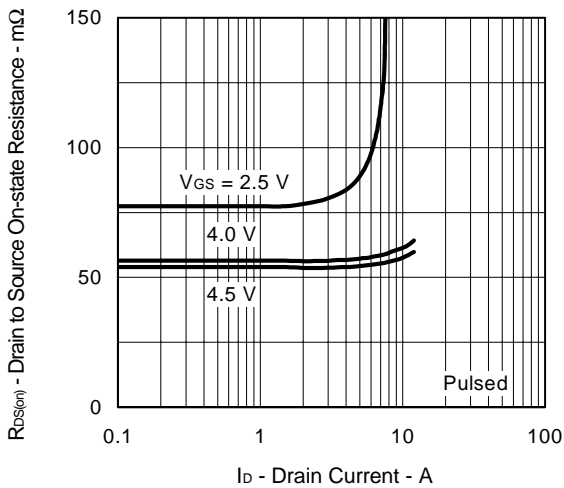
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



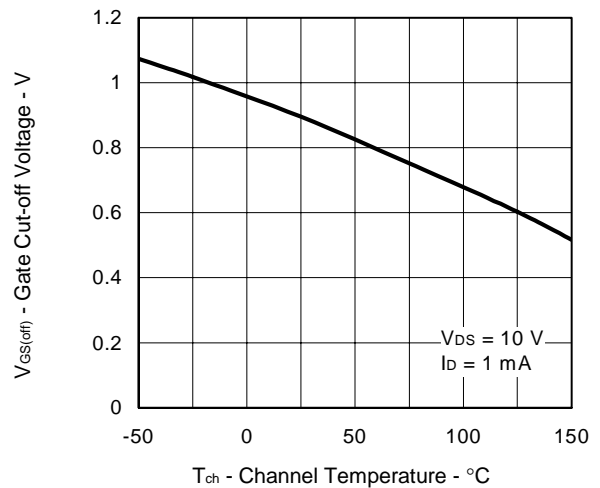
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

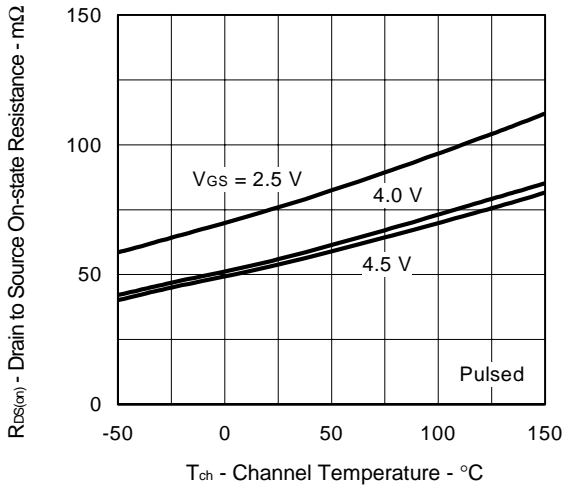


GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

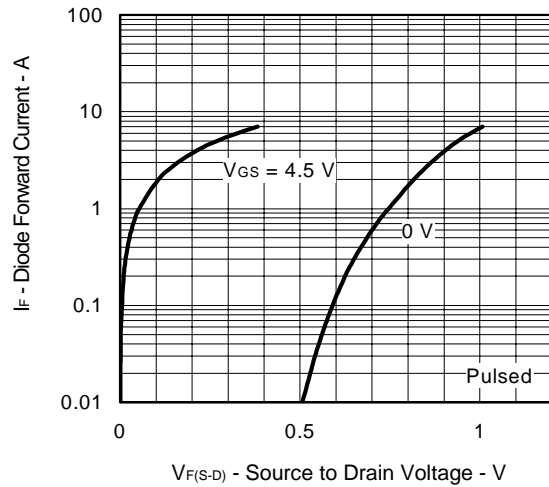


A) N-Channel

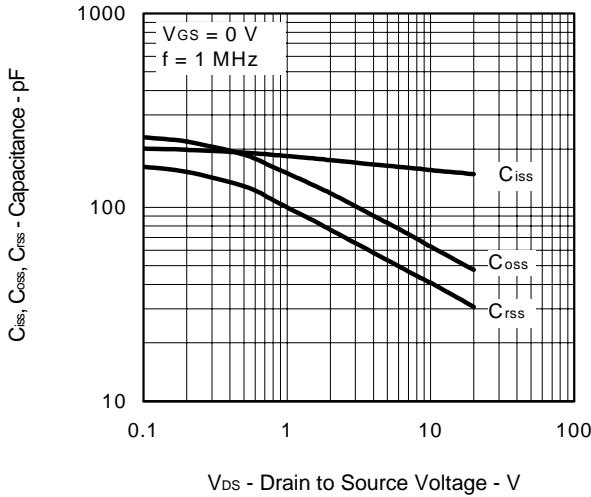
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



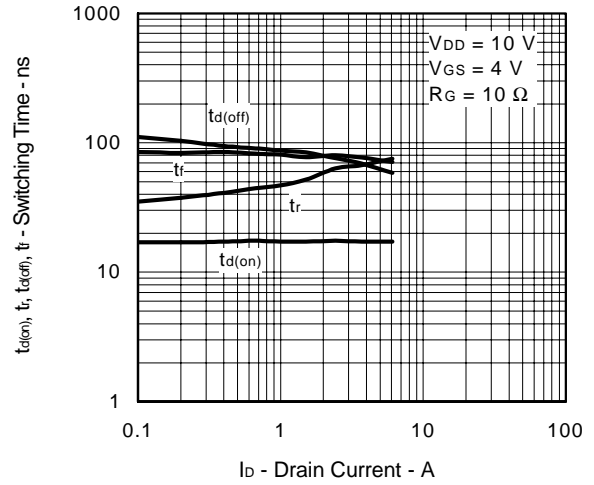
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



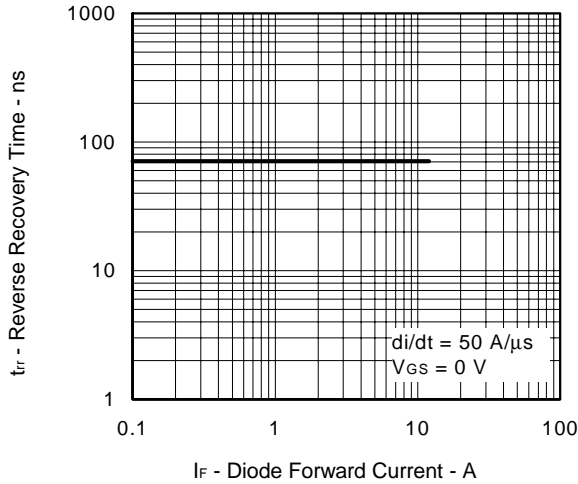
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



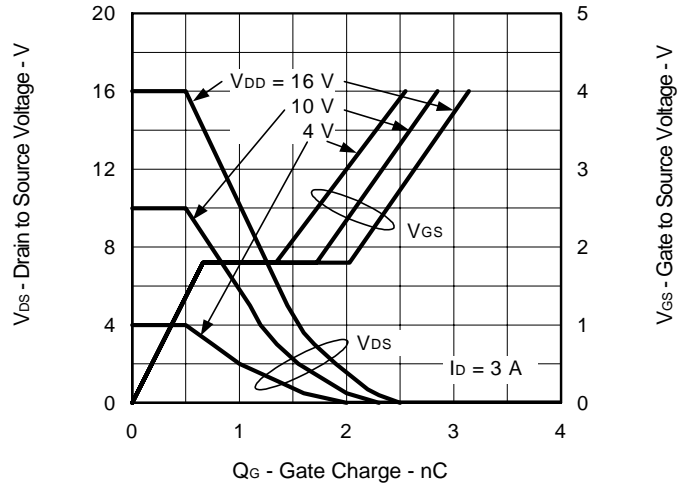
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

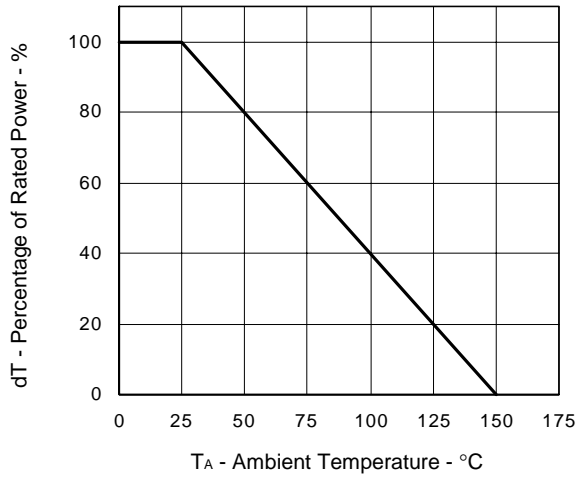


DYNAMIC INPUT/OUTPUT CHARACTERISTICS

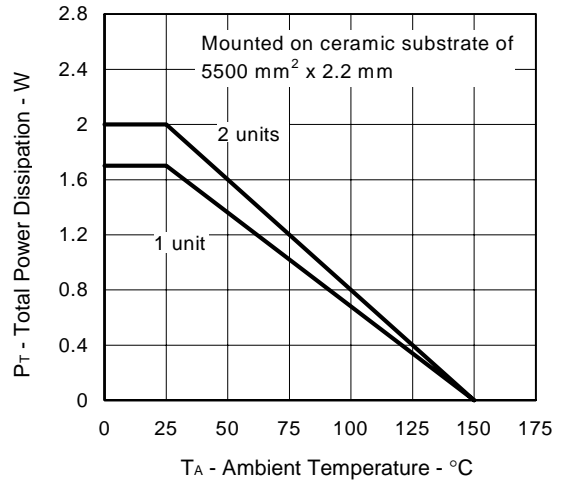


B) P-Channel

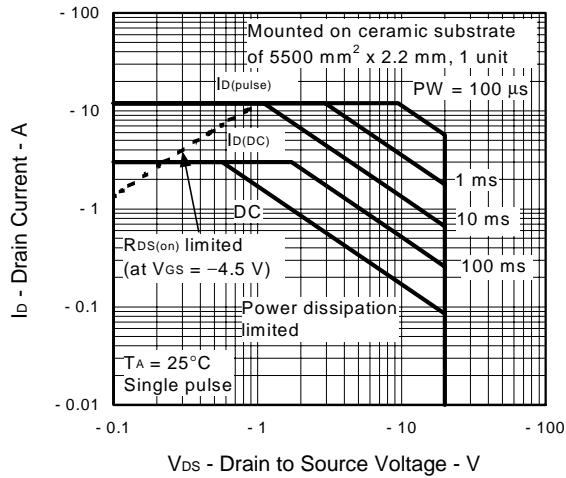
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



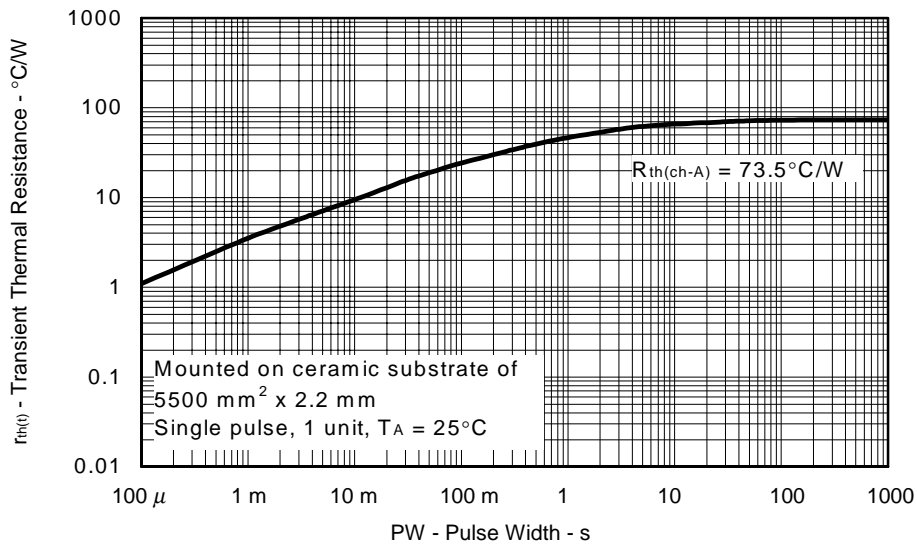
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



FORWARD BIAS SAFE OPERATING AREA



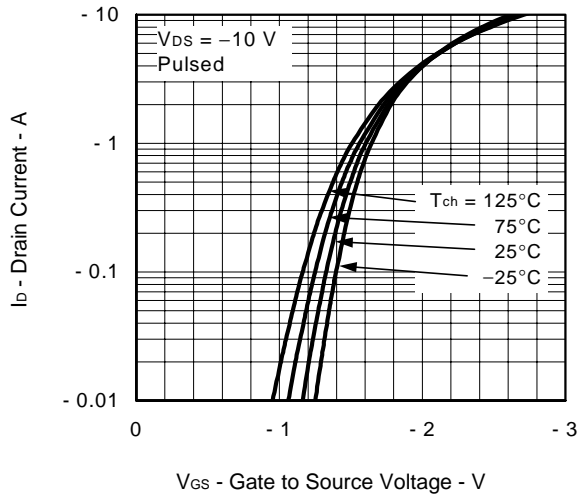
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



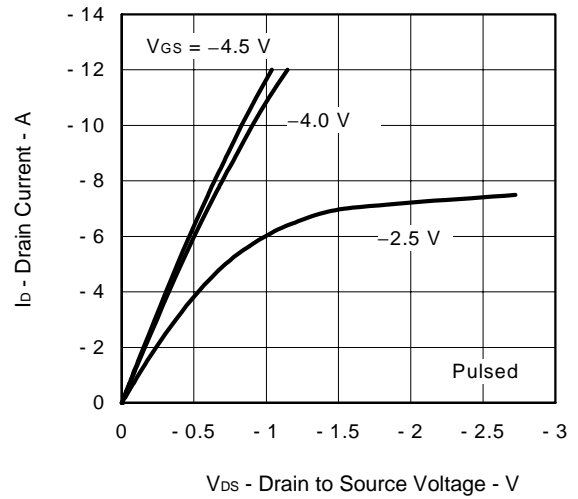


B) P-Channel

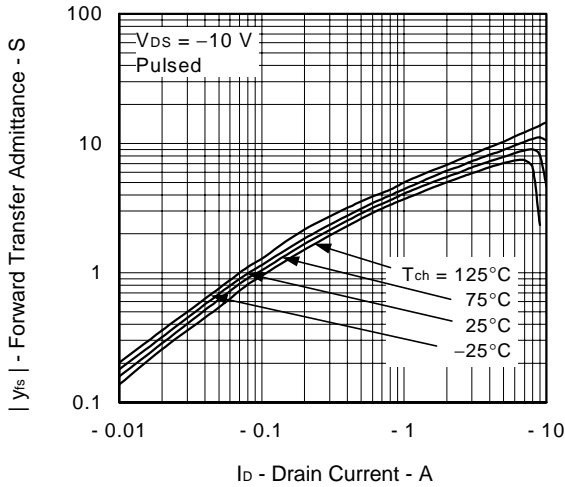
FORWARD TRANSFER CHARACTERISTICS



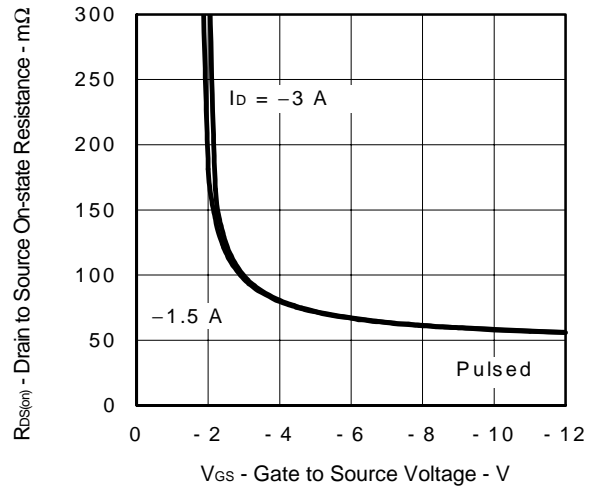
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



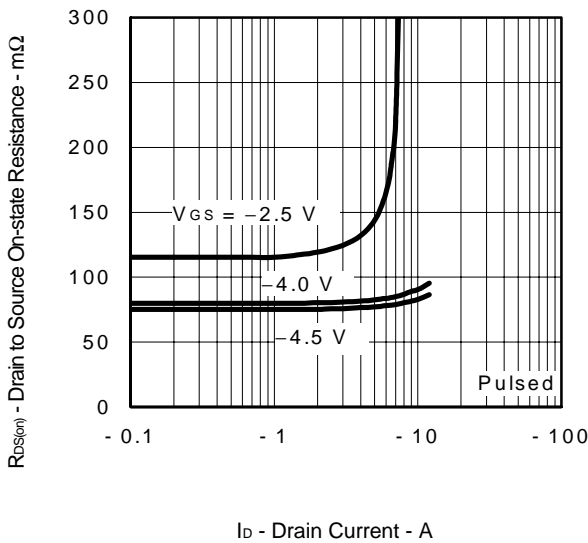
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



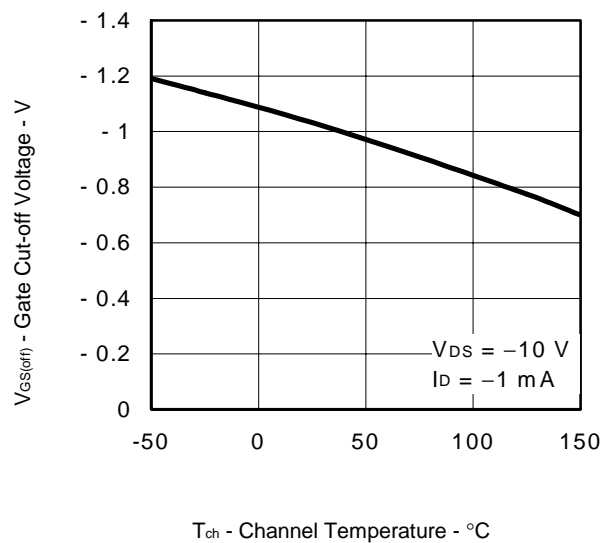
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

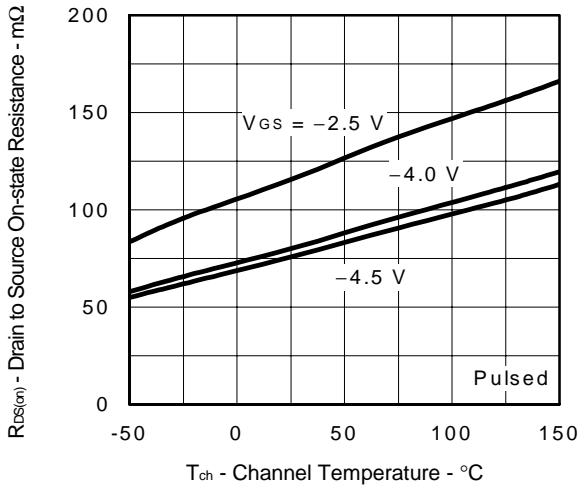


GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

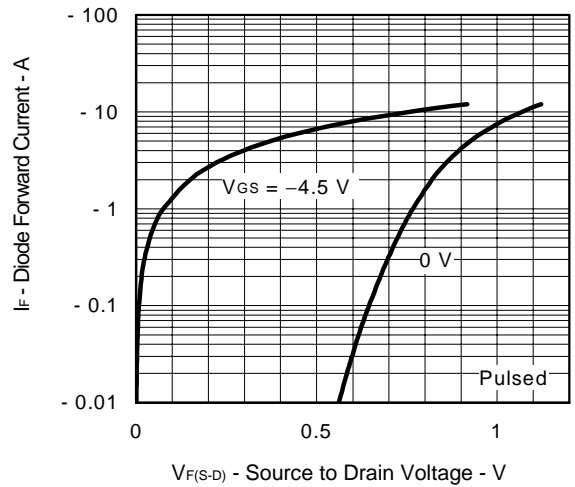


) P-Channel

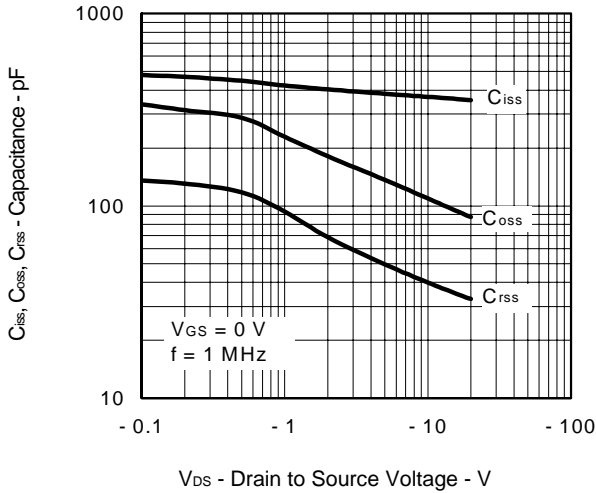
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



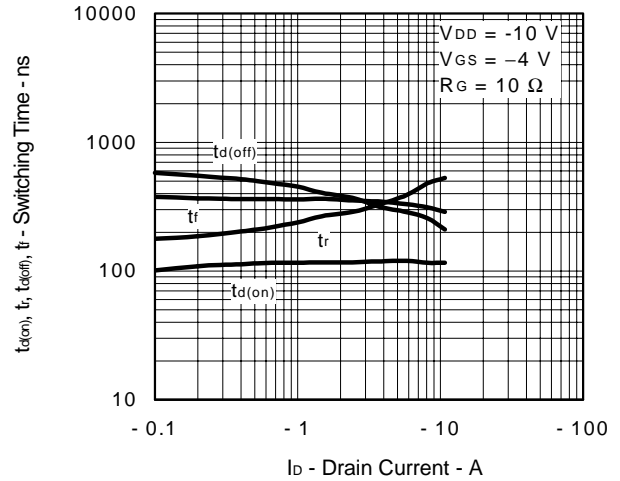
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



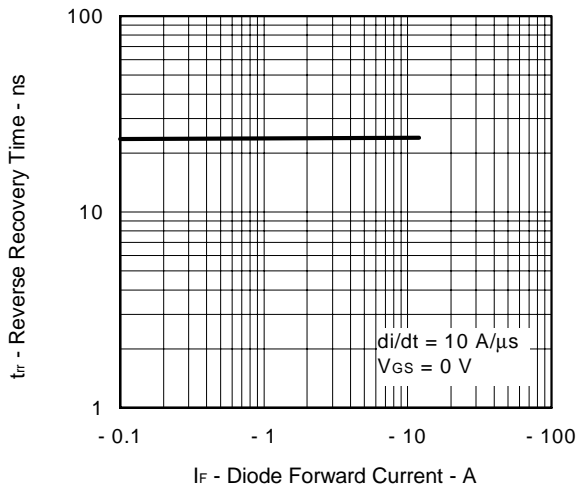
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



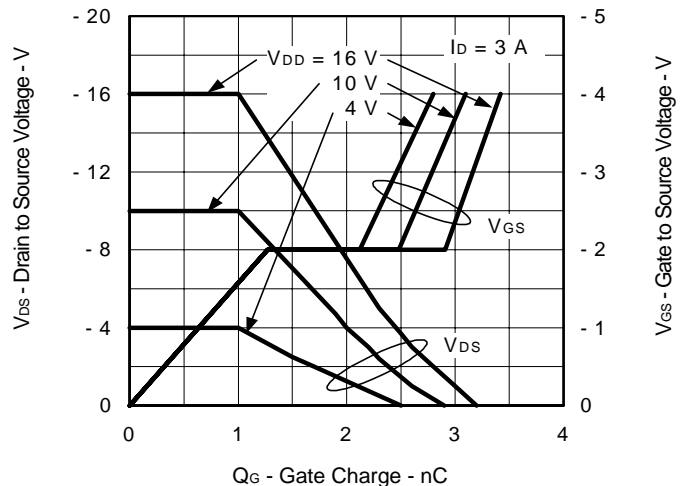
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



[MEMO]

- **The information in this document is current as of September, 2002. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
  - No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
  - NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
  - Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
  - While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
  - NEC semiconductor products are classified into the following three quality grades:  
"Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.
    - "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
    - "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
    - "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.
- The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.
- (Note)
- (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.
  - (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).