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FAIRCHILD SEMICONDUCTOR®

USB1T1105A

Universal Serial Bus Peripheral Transceiver with Voltage Regulator

General Description

The USB1T1105A is an Universal Serial Bus Specification Rev 2.0 compliant transceiver. The device provides an USB interface for Full-Speed (12Mbit/s) USB applications. The USB1T1105A provides excellent flexibility, allowing differential and single ended inputs while an integrated voltage regulator sets the I/O level to 1.65V to 3.6V. Utilizing an integrated 5.0V to 3.3V voltage regulator, the part can be powered directly from the USB host (V_{BUS}) to minimize the power consumed from the local sources while used in devices with low supply voltages.

The USB1T1105A provides 15kV ESD protection on the USB bus pins (D+/D−). This eliminates the need for any external ESD devices while providing excellent protection to larger and more expensive ASICs and USB controllers.

Features

- Complies with Universal Serial Bus Specification 2.0
- Integrated 5V to 3.3V voltage regulator for powering VBus
- Utilizes digital inputs and outputs to transmit and receive USB cable data
- Supports full speed 12Mbits/s speed data rates
- Ideal for portable electronic devices
- 15kV contact HBM ESD protection on bus pins
- 3.3mm leadless package
- Industry standard HBCC footprint is lead-free

Applications

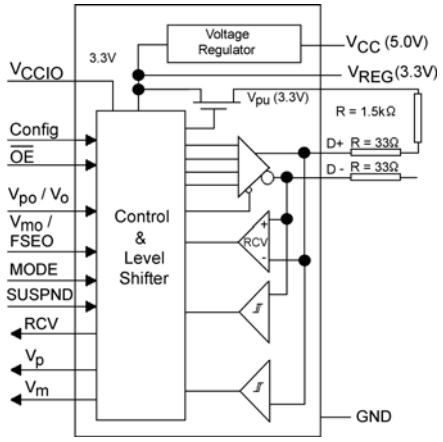
- Cell phone
- PDA
- Digital camera
- MP3

Ordering Code:

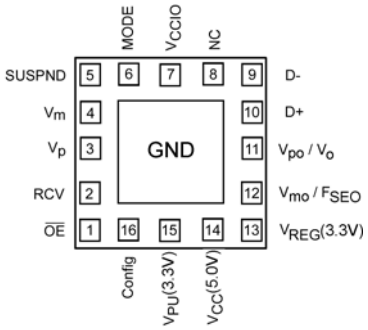
Order Number	Package Number	Package Description
USB1T1105AMHX	MLP16HB	Pb-Free 16-Terminal Molded Leadless Package (MHBCC), JEDEC MO-217, 3mm Square

Pb-Free package per JEDEC J-STD-020B.

Logic Diagram



Connection Diagram



(Bottom View)

Terminal Descriptions

Terminal Number	Terminal Name	I/O	Terminal Description
1	$\overline{OE}$	I	Output Enable: Active LOW enables the transceiver to transmit data on the bus. When not active the transceiver is in the receive mode (CMOS level is relative to V_{CCIO})
2	RCV	O	Receive Data Output: Non-inverted CMOS level output for USB differential Input (CMOS output level is relative to V_{CCIO}). Driven LOW when SUSPN is HIGH; RCV output is stable and preserved during SE0 condition.
3	V_p	O	Single-ended D+ receiver output V_P (CMOS level relative to V_{CCIO}): Used for external detection of SEO, error conditions, speed of connected device; Driven HIGH when no supply connected to V_{CC} and V_{REG}.
4	V_m	O	Single-ended D− receiver output V_m (CMOS level relative to V_{CCIO}): Used for external detection of SEO, error conditions, speed of connected device; Driven HIGH when no supply connected to V_{CC} and V_{REG}.
5	SUSPND	I	Suspend: Enables a low power state (CMOS level is relative to V_{CCIO}). While the SUSPND pin is active (HIGH) it will drive the RCV pin to logic “0” state.
6	MODE	I	MODE input (CMOS level is relative to V_{CCIO}). A HIGH selects the differential input MODE (V_{po}, V_{mo}) whereas a LOW enables the single-ended MODE (V_o, V_{FSEO}) see Table 2 and Table 3
7	V_{CCIO}		Supply Voltage for digital I/O pins (1.65V to 3.6V): When not connected the D+ and D− pins are in 3-STATE. This supply bus is totally independent of V_{CC} (5V) and V_{REG} (3.3V).
8	NC	NC	
10, 9	D+, D−	AI/O	Data +, Data −: Differential data bus conforming to the USB standard.
11	V_{po} / V_o	I	Driver Data Input (CMOS level is relative to V_{CCIO}); Schmitt trigger input; see Table 2 and Table 3
12	V_{mo} / F_{SEO}	I	Driver Data Input (CMOS level is relative to V_{CCIO}); Schmitt trigger input; see Table 2 and Table 3
13	V_{REG} (3.3V)		Internal Regulator Option: Regulated supply output voltage (3.0V to 3.6V) during 5V operation; decoupling capacitor of at least 0.1 μF is required.
14	V_{CC} (5.0V)		Internal Regulator Option: Used as supply voltage input (4.0V to 5.5V); can be connected directly to USB line Vbus.

Terminal Number	Terminal Name	I/O	Terminal Description
15	V_{PU} (3.3V)		Pull-up Supply Voltage (3.3V ± 10%): Connect an external 1.5kΩ resistor on D+ (FS data rate); Pin function is controlled by Config input pin: Config = LOW – V_{PU} (3.3V) is floating (High Impedance) for zero pull-up current. Config = HIGH – V_{PU} (3.3V) = 3.3V; internally connected to V_{REG} (3.3V).
16	Config	I	USB connect or disconnect software control input. Configures 3.3V to external 1.5kΩ resistor on D+ when HIGH.
Exposed Diepad	GND	GND	GND supply down bonded to exposed diepad to be connected to the PCB GND.

Functional Description

The USB1T1105A transceiver is designed to convert CMOS data into USB differential bus signal levels and to convert USB differential bus signal to CMOS data.

To minimize EMI and noise the outputs are edge rate controlled with the rise and fall times controlled and defined for full speed data rates. The rise, fall times are balanced between the differential pins to minimize skew.

Table 1 describes the specific pin functionality selection. Table 2, Table 3, and Table 4 describe the specific Truth Tables for Driver and Receiver operating functions.

The USB1T1105A also has the capability of various power supply configurations to support mixed voltage supply applications (see Table 5) and Power Supply Configurations and Options for detailed descriptions.

Functional Tables

TABLE 1. Function Select

SUSPND	$\overline{OE}$	D+, D–	RCV	V_p/V_m	Function
L	L	Driving & Receiving	Active	Active	Normal Driving (Differential Receiver Active)
L	H	Receiving (Note 1)	Active	Active	Receiving
H	L	Driving	Inactive (Note 2)	Active	Driving during Suspend (Differential Receiver Inactive)
H	H	3-STATE (Note 1)	Inactive (Note 2)	Active	Low Power State

Note 1: Signal levels is function of connection and/or pull-up/pull-down resistors.

Note 2: For SUSPND = HIGH mode the differential receiver is inactive and the output RCV output is forced LOW. The out-of-suspend signaling (K) is detected via the single-ended receiver outputs of the V_p and V_m pins.

TABLE 2. Driver Function ($\overline{OE}$ = L) using Differential Input Interface Mode Pin = H

V_{mo}	V_{po}	Data
L	L	SE0 (Note 3)
L	H	Differential Logic 1
H	L	Differential Logic 0
H	H	Illegal State

Note 3: SE0 = Single Ended Zero

TABLE 3. Driver Function ($\overline{OE}$ = L) using Single-ended Input Interface Mode Pin = L

FSE0	V_o	Data
L	L	Differential Logic 0
L	H	Differential Logic 1
H	L	SE0 (Note 4)
H	H	SE0 (Note 4)

Note 4: SE0 = Single Ended Zero

TABLE 4. Receiver Function ($\overline{OE}$ = H)

D+, D−	RCV	V_p	V_m
Differential Logic 1	H	H	L
Differential Logic 0	L	L	H
SE0	X	L	L
Sharing Mode	L	H	H

X = Don't Care

Power Supply Configurations and Options

The three modes of power supply operation are:

- Normal Mode: Regulated Output and Regulator Bypass
  1. Regulated Output: V_{CCIO} is connected and V_{CC} (5.0) is connected to 5V (4.0V to 5.5V) and the internal voltage regulator then produces 3.3V for the USB connections.
  2. Internal Regulator Bypass Mode: V_{CCIO} is connected and both V_{CC}(5.5) and V_{REG}(3.3) are connected to a 3.3V source (3.0V to 3.6V).

  In both cases for normal mode the V_{CCIO} is an independent voltage source (1.65V to 3.6V) that is a function of the external circuit configuration.
- Sharing Mode: V_{CCIO} is only supply connected. V_{CC} and V_{REG} are not connected. In this mode the D+ and D− pins are 3-STATE and the USB1T1105A allows external signals up to 3.6V to share the D+ and D− bus lines. Internally the circuitry limits leakage from D+ and D− pins (maximum 10 μA) and V_{CCIO} such that device is in low power (suspended) state. Terminals Vbusmon and RCV are forced LOW as an indication of this mode with Vbusmon being ignored during this state.
- Disable Mode: V_{CCIO} is not connected. V_{CC} is connected, or V_{CC} and V_{REG} are connected. 0V to 3.3V in this mode D+ and D− are 3-STATE and V_{PU} is HIGH Impedance (switch is turned off). The USB1T1105A allows external signals up to 3.6V to share the D+ and D− bus lines. Internally the circuitry limits leakage from D+ and D− terminals (maximum 10μA).

A summary of the Supply Configurations is described in Table 5.

TABLE 5. Power Supply Configuration Options

Pins	Power Supply Mode Configuration			
	Sharing	Disable	Normal (Regulated Output)	Normal (Regulator Bypass)
V_{CC} (5V)	< 3.6V	Connected to 5V Source	Connected to 5V Source	Connected to V_{REG} (3.3V) [max drop of 0.3V] (2.7V to 3.6V)
V_{REG} (3.3V)	Pulled LOW Regulator OFF	3.3V, 300 μA Regulated Output	3.3V, 300 μA Regulated Output	Connected to 3.3V Source
V_{CCIO}	1.65V to 3.6V Source	Not Connected	1.65V to 3.6V Source	1.65V to 3.6V Source
V_{PU} (3.3V)	3-STATE (Off)	3-STATE (Off)	3.3V Available if Config = HIGH	3.3V Available if Config = HIGH
D+, D−	3-STATE	3-STATE	Function of Mode Set Up	Function of Mode Set Up
V_p, V_m	H	Invalid	Function of Mode Set Up	Function of Mode Set Up
RCV	L	Invalid	Function of Mode Set Up	Function of Mode Set Up
OE, SUSPND, Config, V_{po}/V_o, V_{mo}/F_{SEO}, MODE	Hi-Z	Hi-Z	Function of Mode Set Up	

Note 5: Hi-Z or forced LOW.

Absolute Maximum Ratings(Note 6)

Supply Voltage (V_{CC})(5V)	−0.5V to +6.0V
I/O Supply Voltage (V_{CCIO})	−0.5V to +4.6V
Latch-up Current (I_{LU})	
V_I = −1.8V to +5.4V	150 mA
DC Input Current (I_{IK})	
$V_I < 0$	−18 mA
DC Input Voltage (V_I)	
(Note 7)	−0.5V to V_{CCIO} +0.5V
DC Output Diode Current (I_{OK})	
$V_O > V_{CC}$ or $V_O < 0$	±18 mA
DC Output Voltage (V_O)	
(Note 7)	−0.5V to V_{CCIO} + 0.5V
Output Source or Sink Current (I_O)	
V_O = 0 to V_{CC}	
Current for D+, D− Pins	±12 mA
Current for RCV, V_m/V_p	±12 mA
DC V_{CC} or GND Current	
(I_{CC}, I_{GND})	±100 mA
ESD Immunity Voltage (V_{ESD});	
Contact HBM	
Pins D+, D−, and GND	15kV
All Other Pins	2.5kV
Storage Temperature (T_{STO})	−40°C to + 125°C
Power Dissipation (P_{TOT})	
I_{CC} (5V)	48 mW
I_{CCIO}	9 mW

Recommended Operating Conditions

DC Supply Voltage V_{CC} (5V)	4.0V to 5.5V
I/O DC Voltage V_{CCIO}	1.65V to 3.6V
DC Input Voltage Range (V_I)	0V to V_{CCIO} + 0.5V
DC Input Range for AI/O ($V_{IA/O}$)	0V to 3.6V
Pins D+ and D−	0V to 3.6V
Operating Ambient Temperature	
(T_{AMB})	−40°C to +85°C

Note 6: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristic tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 7: IO Absolute Maximum Rating must be observed.

DC Electrical Characteristics (Supply Pins)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted).
V_{CC} (5V) = 4.0V to 5.5V or V_{REG} (3.3V) = 3.0V to 3.6V, V_{CCIO} = 1.65V to 3.6V

Symbol	Parameter	Conditions	Limits			Units
			−40°C to +85°C			
			Min	Typ	Max	
V_{REG} (3.3V)	Regulated Supply Output	Internal Regulator Option; $I_{LOAD} \le 300$ µA	3.0 (Note 8)(Note 9)	3.3	3.6	V
I_{CC}	Operating Supply Current (V_{CC}5.0)	Transmitting and Receiving at 12 Mbits/s; C_{LOAD} = 50 pF (D+, D−)		4.0 (Note 10)	8.0	mA
I_{CCIO}	I/O Operating Supply Current	Transmitting and Receiving at 12 Mbits/s		1.0 (Note 10)	2.0	mA
$I_{CC\ (IDLE)}$	Supply Current during FS IDLE and SE0 (V_{CC}5.0)	IDLE: $V_{D+} \ge 2.7V$, $V_{D-} \le 0.3V$; SE0: $V_{D+} \le 0.3V$, $V_{D-} \le 0.3V$			500 (Note 11)	µA
$I_{CCIO\ (STATIC)}$	I/O Static Supply Current	IDLE, SUSPND or SE0			20.0	µA
$I_{CC(SUSPND)}$	Suspend Supply Current USB1T1105A	SUSPND = HIGH $\overline{OE}$ = HIGH $V_m = V_p$ = OPEN			25.0 (Note 11)	µA
$I_{CCIO(SHARING)}$	I/O Sharing Mode Supply Current	V_{CC} (5V) Not Connected			20.0	µA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Limits			Units
			−40°C to +85°C			
			Min	Typ	Max	
$I_{D\pm(SHARING)}$	Sharing Mode Load Current on D+/D− Pins	V_{CC} (5V) Not Connected Config = LOW; $V_{D\pm}$ = 3.6V			10.0	μA
V_{CCTH}	V_{CC} Threshold Detection Voltage	1.65V ≤ V_{CCIO} ≤ 3.6V				V
		Supply Lost			3.6	
		Supply Present	4.1			
V_{CCHYS}	V_{CC} Threshold Detection Hysteresis Voltage	V_{CCIO} = 1.8V		70.0		mV
V_{CCIOTH}	V_{CCIO} Threshold Detection Voltage	2.7V ≤ V_{REG} ≤ 3.6V				V
		Supply Lost			0.5	
		Supply Present	1.4			
$V_{CCIOHYS}$	V_{CCIO} Threshold Detection Hysteresis Voltage	V_{REG} = 3.3V		450		mV

Note 8: I_{LOAD} includes the pull-up resistor current via pin V_{PU}

Note 9: The minimum voltage in Suspend mode is 2.7V.

Note 10: Not tested in production, value based on characterization.

Note 11: Excludes any current from load and V_{PU} current to the 1.5kΩ resistor.

Note 12: Includes current between V_{pu} and the 1.5k internal pull-up resistor.

Note 13: When V_{CCIO} < 2.7V, minimum value for V_{REGTH} = 2.0V for supply present condition.

DC Electrical Characteristics (Digital Pins – excludes D+, D− Pins)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted). V_{CCIO} = 1.6V to 3.6V

Symbol	Parameter	Test Conditions	Limits		Units
			−40°C to +85°C		
			Min	Max	
Input Levels					
V_{IL}	LOW Level Input Voltage			0.3	V
V_{IH}	HIGH Level Input Voltage		0.6*V_{CCIO}		V
V_{HYS}	Hysteresis Voltage P11 + P12	Pins V_{po}/V_{mo}, V_{CCIO} = 3.3V	0.3	0.7	V
Output Levels					
V_{OL}	LOW Level Output Voltage	I_{OL} = 2 mA		0.4	V
		I_{OL} = 100 μA		0.15	
V_{OH}	HIGH Level Output Voltage	I_{OH} = 2 mA	V_{CCIO} - 0.4		V
		I_{OH} = 100 μA	V_{CCIO}- 0.15		
Leakage Current					
I_{LI}	Input Leakage Current	V_{CCIO} = 1.65V to 3.6V		±1.0 (Note 14)	μA
Capacitance					
C_{IN}, $C_{I/O}$	Input Capacitance	Pin to GND		10.0	pF

Note 14: If V_{CCIO} ≥ V_{REG} then leakage current will be higher than specified.

DC Electrical Characteristics (Analog I/O Pins – D+, D– Pins)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted). V_{CC} = 4.0V to 5.5V or V_{REG} = 3.0V to 3.6V

Symbol	Parameter	Test Condition	Limits			Units
			–40°C to +85°C			
			Min	Typ	Max	
Input Levels – Differential Receiver						
V_{DI}	Differential Input Sensitivity	$\lvert V_{I(D+)} - V_{I(D-)} \rvert$	0.2			V
V_{CM}	Differential Common Mode Voltage		0.8		2.5	V
Input Levels – Single-ended Receiver						
V_{IL}	LOW Level Input Voltage				0.8	V
V_{IH}	HIGH Level Input Voltage		2.0			V
V_{HYS}	Hysteresis Voltage		0.4		0.7	V
Output Levels						
V_{OL}	LOW Level Output Voltage	R_L = 1.5kΩ to 3.6V			0.3	V
V_{OH}	HIGH Level Output Voltage	R_L = 15kΩ to GND	2.8 (Note 15)		3.6	V
Leakage Current						
I_{LZ}	Input Leakage Current Off State	$\overline{OE}$ = H			±1.0	µA
Capacitance						
$C_{I/O}$	I/O Capacitance	Pin to GND			20.0	pF
Resistance						
Z_{DRV}	Driver Output Impedance		34.0	41.0 (Note 16)	44.0	Ω
Z_{IN}	Driver Input Impedance		10.0			MΩ
R_{SW}	Switch Resistance				10.0	Ω
V_{TERM}	Termination Voltage	R_{PU} Upstream Port	3.0 (Note 17) (Note 18)		3.6	V

Note 15: V_{OH} min. = V_{REG} - 0.2V.

Note 16: Includes external resistors of 33Ω on both D+ and D– pins.

Note 17: This voltage is available at pin V_{PU} and V_{REG}.

Note 18: Minimum voltage is 2.7V in the suspend mode.

AC Electrical Characteristics (A I/O Pins Full Speed)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted). V_{CC} = 4.0V to 5.5V or V_{REG} = 3.0V to 3.6V, V_{CCIO} = 1.65V to 3.6V, C_L = 50 pF; R_L = 1.5K on D+ to V_{PU}

Symbol	Parameter	Test Conditions	Limits			Unit
			−40°C to +85°C			
			Min	Typ	Max	
Driver Characteristics						
t_{FR}	Output Rise Time	C_L = 50 − 125 pF	4.0		20.0	ns
		10% to 90%				
t_{FF}	Output Fall Time	Figures 1, 5	4.0		20.0	
f_{RFM}	Rise/Fall Time Match	t_F/ t_R Excludes First Transition from Idle State	90.0		111.1	%
V_{CRS} (Note 19)	Output Signal Crossover Voltage	Excludes First Transition from Idle State see Waveform	1.3		2.0	V
Driver Timing						
t_{PLH} t_{PHL}	Propagation Delay (V_p/V_{po}, V_m/V_{mo} to D+/D−)	Figures 2, 5			18.0	ns
t_{PHZ} t_{PLZ}	Driver Disable Delay ($\overline{OE}$ to D+/D−)	Figures 4, 6			15.0	ns
t_{PZH} t_{PZL}	Driver Enable Delay ($\overline{OE}$ to D+/D−)	Figures 4, 6			15.0	ns
Receiver Timing						
t_{PLH} t_{PHL}	Propagation Delay (Diff) (D+/D− to Rev)	Figures 3, 7			15.0	ns
t_{PLH} t_{PHL}	Single Ended Receiver Propagation Delay (D+/D− to V_p/ V_{po}, V_m/V_{mo})	Figures 3Figure 7			18.0	ns

Note 19: Not production tested, guaranteed by characterization.

AC Waveforms

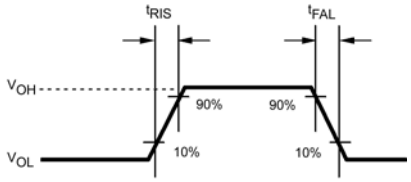


FIGURE 1. Rise and Fall Times

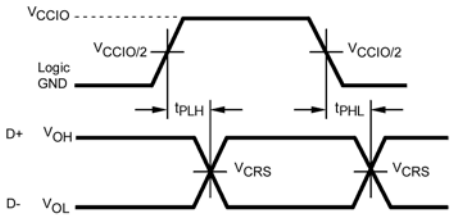


FIGURE 2. V_{po}/V_o, V_{mo}/V_{SEO} to D+/D–

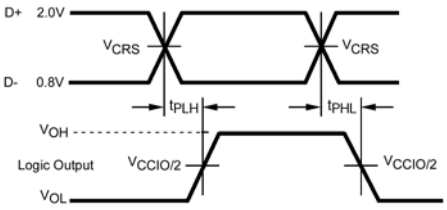


FIGURE 3. D+/D– to R_{CV}, V_p and V_m

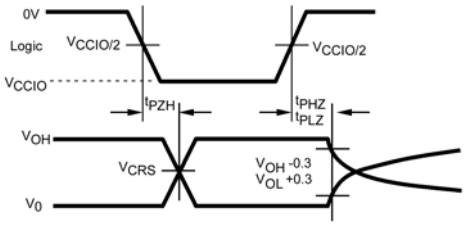
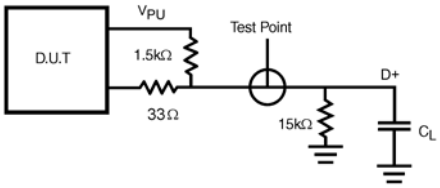


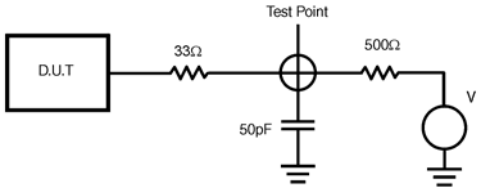
FIGURE 4. $\overline{OE}$ to D+/D–

Test Circuits and Waveforms



C_L = 50 pF Full Speed Propagation Delays
C_L = –125 pF Edge Rates only

FIGURE 5. Load for D+/D–



V = 0 for t_{PZH}, t_{PHZ}
V = V_{REG} for t_{PZL}

FIGURE 6. Load for Enable and Disable Times

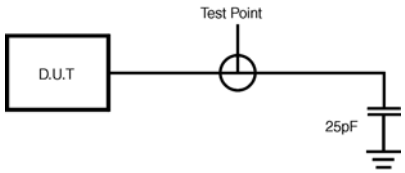


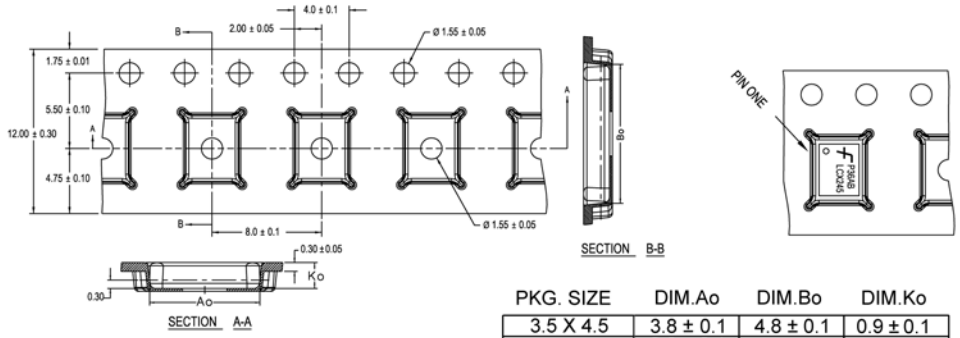
FIGURE 7. Load for V_m/V_{mo}, V_p/V_{po} and RCV

Tape and Reel Specification

Tape Format for MHBCC

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
MHX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



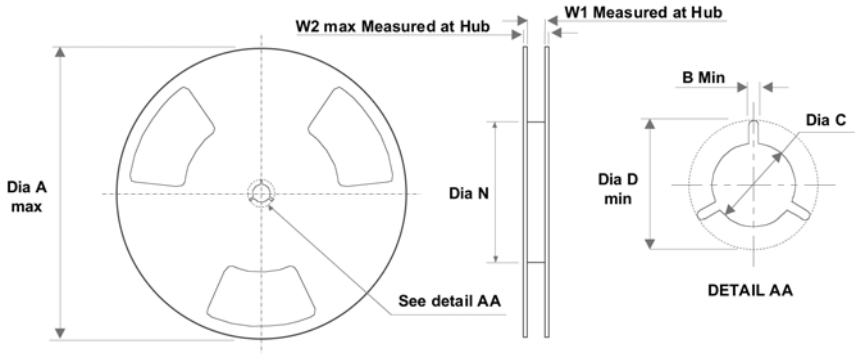
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

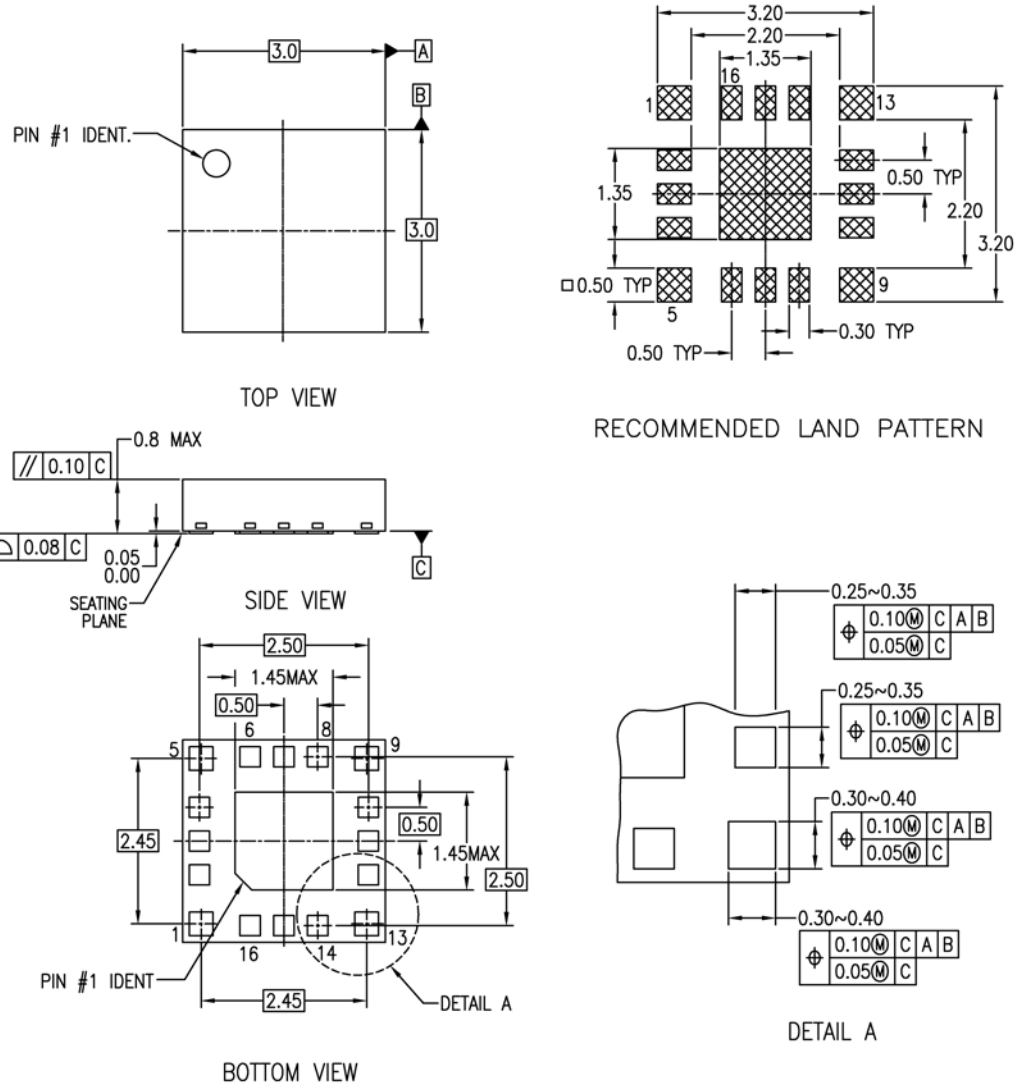
1. Cummulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Diemension in inches rounded.

REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0	0.059	0.512	0.795	7.008	0.488	0.724
	330	(1.50)	(13.00)	(20.20)	(178)	(12.4)	(18.4)

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. SIMILAR TO JEDEC REGISTRATION MO-217, DATED 11/2001
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP16HBrevA

Pb-Free 16-Terminal Molded Leadless Package (MHBCC), JEDEC MO-217, 3mm Square
Package Number MLP16HB

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of terms

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