



FEATURES

- Four 8-bit voltage output DACs
- Dual 2.7V to 5.5V supply (separate digital and analogue supplies)
- DNL ± 0.03 LSB, INL ± 0.3 LSB typical
- Low power consumption:
 - 3mW, slow mode - 3V supply
 - 9mW, fast mode - 3V supply
- DSP and microprocessor compatible serial interface
- Programmable settling time of 2.5 μ s or 8.5 μ s typical

APPLICATIONS

- Battery powered test instruments
- Digital offset and gain adjustment
- Battery operated/remote industrial controls
- Machine and motion control devices
- Wireless telephone and communication systems
- Arbitrary waveform generation
- Robotics

ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM2627CDT	0° to 70°C	16-pin TSSOP
WM2627IDT	-40° to 85°C	16-pin TSSOP

DESCRIPTION

The WM2627 is a quadruple 8-bit voltage output, resistor string, digital-to-analogue converter. Each DAC can be individually powered down under software control. A hardware controlled mode is provided that powers down all DACs. Power down reduces current consumption to 1 μ A.

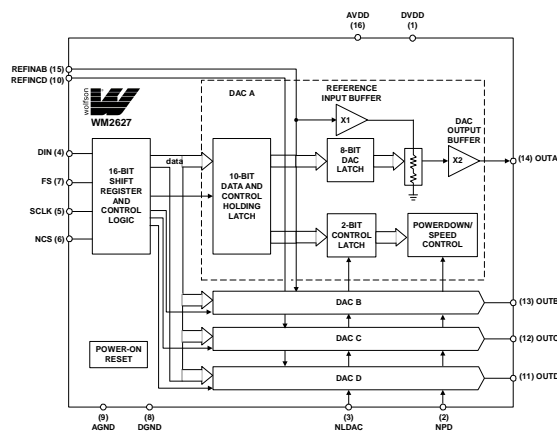
The device has been designed to interface efficiently to industry standard microprocessors and DSPs. It is programmed with a 16-bit serial word comprising of a DAC address, individual DAC control bits and an 8-bit value.

The WM2627 has provision for two supplies: one supply for the serial interface (DVDD, DGND), and one for the DACs, reference buffers and output buffers (AVDD, AGND). This enables a typical application where the device can be controlled via a microprocessor operating on a 3V supply, with the DACs operating on a 5V supply. Alternatively, the supplies can be tied together in a single supply application.

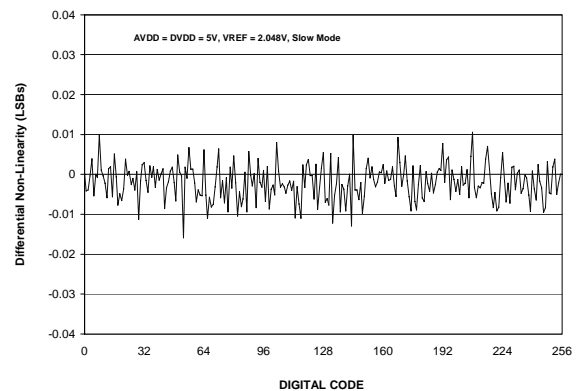
Excellent performance is delivered with a typical DNL of ± 0.03 LSB. The settling time of the DAC is programmable to allow the designer to optimize speed versus power dissipation. The output stage is buffered by a x2 gain near rail-to-rail amplifier, which features a Class AB output stage. DACs A and B can have a different reference voltage to DACs C and D.

The device is available in a 16-pin TSSOP package. Commercial temperature (0° to 70°C) and Industrial temperature (-40° to 85°C) variants are supported.

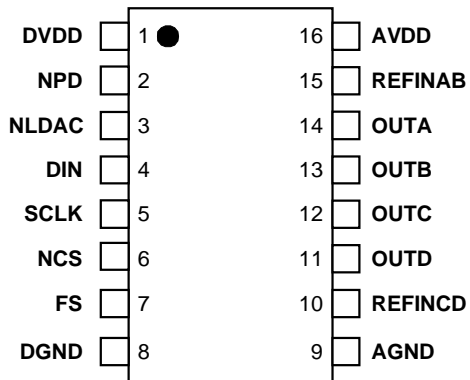
BLOCK DIAGRAM



TYPICAL PERFORMANCE



PIN CONFIGURATION



PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	DVDD	Supply	Digital supply.
2	NPD	Digital input	Power down. Powers down all DACs overriding their individual power down settings and all output stages. This pin is active low.
3	NLDAC	Digital input	Load DAC. Digital input active low. NLDAC must be taken low to update the DAC latch from the holding latches.
4	DIN	Digital input	Serial data input.
5	SCLK	Digital input	Serial clock input.
6	NCS	Digital input	Chip select. This pin is active low.
7	FS	Digital input	Frame synchronisation for serial input data.
8	DGND	Ground	Digital ground.
9	AGND	Ground	Analogue ground.
10	REFINCD	Analogue input	Voltage reference input for DACs C and D.
11	OUTD	Analogue output	DAC D output.
12	OUTC	Analogue output	DAC C output.
13	OUTB	Analogue output	DAC B output.
14	OUTA	Analogue output	DAC A output.
15	REFINAB	Analogue input	Voltage reference input for DACs A and B.
16	AVDD	Supply	Analogue supply.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION		MIN	MAX
Supply voltages, AVDD to AGND, DVDD to DGND			7V
Supply voltage differences, AVDD to DVDD		-2.8V	2.8V
Digital input voltage		-0.3V	DVDD + 0.3V
Reference input voltage		-0.3V	AVDD + 0.3V
Operating temperature range, T _A	WM2627C	0°C	70°C
	WM2627I	-40°C	85°C
Storage temperature		-65°C	150°C
Soldering lead temperature, 1.6mm (1/16 inch) from package body for 10 seconds			260°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage	AVDD, DVDD		2.7		5.5	V
High-level digital input voltage	V _{IH}	DVDD = 2.7V to 5.5V	2			V
Low-level digital input voltage	V _{IL}	DVDD = 2.7V to 5.5V			0.8	V
Reference voltage to REFINAB, REFINCD	V _{REF}	See Note	0		AVDD - 1.5	V
Load resistance	R _L		2	10		kΩ
Load capacitance	C _L				100	pF
Serial clock rate	f _{SCLK}				20	MHz
Operating free-air temperature	T _A	WM2627CDT	0		70	°C
		WM2627IDT	-40		85	°C

Note: Reference voltages greater than AVDD/2 will cause output saturation for large DAC codes.

ELECTRICAL CHARACTERISTICS**Test Conditions:**

$R_L = 10k\Omega$, $C_L = 100pF$. $AVDD = DVDD = 5V \pm 10\%$, $V_{REF} = 2.048V$ and $AVDD = DVDD = 3V \pm 10\%$, $V_{REF} = 1.024V$ over recommended operating free-air temperature range (unless noted otherwise).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static DAC Specifications						
Resolution			8			bits
Integral non-linearity	INL	See Note 1		± 0.3	± 0.5	LSB
Differential non-linearity	DNL	See Note 2		± 0.03	± 0.5	LSB
Zero code error	ZCE	See Note 3			± 10	mV
Gain error	GE	See Note 4			± 0.6	% FSR
Power supply rejection ratio	PSRR	See Note 5		-68		dB
Zero code error temperature coefficient		See Note 6		10		ppm/°C
Gain error temperature coefficient		See Note 6		10		ppm/°C
DAC Output Specifications						
Output voltage range		$R_L = 10k\Omega$	0		$AVDD - 0.1$	V
Output load regulation		2k Ω to 10k Ω load See Note 7		0.1	0.25	% of FS voltage
Power Supplies						
Active supply current	I_{DD}	No load, $V_{IH} = DVDD$, $V_{IL} = 0V$ AVDD = 5V, $V_{REF} = 2.048V$ Slow AVDD = 5V, $V_{REF} = 2.048V$ Fast AVDD = 3V, $V_{REF} = 1.024V$ Slow AVDD = 3V, $V_{REF} = 1.024V$ Fast See Note 8		1.4 3.5 1.0 3.0	2.2 5.5 1.5 4.5	mA
Power down supply current		No load, all digital inputs 0V or DVDD		1		μA
Dynamic DAC Specifications						
Slew rate		Fast Slow See Note 9		1.0 5.0		V/ μs V/ μs
Settling time		To $\pm 0.1LSB$ Slow Fast See Note 10		8.5 2.5		μs μs
Glitch energy		Code 127 to 128		10		nV-s
Signal to noise ratio	SNR	$f_s = 400ksps$, $f_{OUT} = 1kHz$, BW = 20kHz See Note 11		57		dB
Signal to noise and distortion ratio	SINAD	$f_s = 400ksps$, $f_{OUT} = 1kHz$, BW = 20kHz See Note 11		49		dB
Total harmonic distortion	THD	$f_s = 400ksps$, $f_{OUT} = 1kHz$, BW = 20kHz See Note 11		-50		dB
Spurious free dynamic range	SFDR	$f_s = 400ksps$, $f_{OUT} = 1kHz$, BW = 20kHz See Note 11		60		dB

Test Conditions:

$R_L = 10k\Omega$, $C_L = 100pF$. $AVDD = DVDD = 5V \pm 10\%$, $V_{REF} = 2.048V$ and $AVDD = DVDD = 3V \pm 10\%$, $V_{REF} = 1.024V$ over recommended operating free-air temperature range (unless noted otherwise).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference						
Reference input resistance	R_{REFIN}			10		$M\Omega$
Reference input capacitance	C_{REFIN}			5		pF
Reference feedthrough		$V_{REF} = 1V_{PP}$ at 1kHz + 1.024V dc, DAC code 0		-75		dB
Reference input bandwidth		$V_{REF} = 0.2V_{PP} + 1.024V$ dc DAC code 128 Slow Fast		0.5 1		MHz MHz
Digital Inputs						
High level input current	I_{IH}	Input voltage = DVDD			± 1	μA
Low level input current	I_{IL}	Input voltage = 0V			± 1	μA
Input capacitance	C_I			3		pF

Notes:

- Integral non-linearity (INL)** is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full scale errors).
- Differential non-linearity (DNL)** is the difference between the measured and ideal 1LSB amplitude change of any adjacent two codes. A guarantee of monotonicity means the output voltage changes in the same direction (or remains constant) as a change in digital input code.
- Zero code error** is the voltage output when the DAC input code is zero.
- Gain error** is the deviation from the ideal full scale output excluding the effects of zero code error.
- Power supply rejection ratio** is measured by varying AVDD from 4.5V to 5.5V and measuring the proportion of this signal imposed on the zero code error and the gain error.
- Zero code error** and **Gain error** temperature coefficients are normalised to full scale voltage.
- Output load regulation** is the difference between the output voltage at full scale with a 10k Ω load and 2k Ω load. It is expressed as a percentage of the full scale output voltage with a 10k Ω load.
- I_{DD}** is measured while continuously writing code 512 to the DAC. For $V_{IH} < DVDD - 0.7V$ and $V_{IL} > 0.7V$ supply current will increase.
- Slew rate** results are for the lower value of the rising and falling edge slew rates.
- Settling time** is the time taken for the signal to settle to within 0.1LSB of the final measured value for both rising and falling edges. Limits are ensured by design and characterisation, but are not production tested.
- SNR, SNRD, THD** and **SPFDR** are measured on a synthesised sinewave at frequency f_{OUT} generated with a sampling frequency f_s .

SERIAL INTERFACE

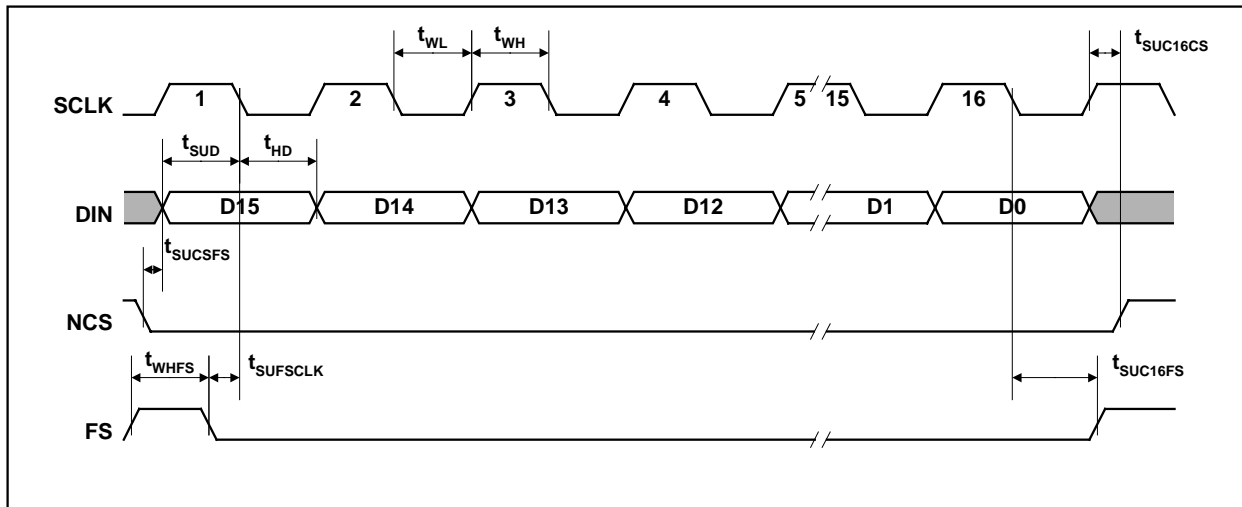


Figure 1 Timing Diagram

Test Conditions:

$R_L = 10k\Omega$, $C_L = 100pF$. $AVDD = DVDD = 5V \pm 10\%$, $V_{REF} = 2.048V$ and $AVDD = DVDD = 3V \pm 10\%$, $V_{REF} = 1.024V$ over recommended operating free-air temperature range (unless noted otherwise)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SUCSFS}	Setup time NCS low before negative FS edge.	10			ns
$t_{SUFSCLK}$	Setup time FS low before first negative SCLK edge.	8			ns
$t_{SUC16FS}$	Setup time, sixteenth negative SCLK edge after FS low on which D0 is sampled before rising edge of FS.	10			ns
$t_{SUC16CS}$	Setup time, sixteenth positive SCLK edge (first positive after D0 sampled) before NCS rising edge. If FS is used instead of the sixteenth positive edge to update the DAC, then the setup time is between the FS rising edge and the NCS rising edge.	10			ns
t_{WHCLK}	Pulse duration, SCLK high.	25			ns
t_{WLCLK}	Pulse duration, SCLK low.	25			ns
t_{SUDCLK}	Setup time, data ready before SCLK falling edge.	8			ns
t_{HDCLK}	Hold time, data held valid after SCLK falling edge.	5			ns
t_{WHFS}	Pulse duration, FS high.	20			ns

TYPICAL PERFORMANCE GRAPHS

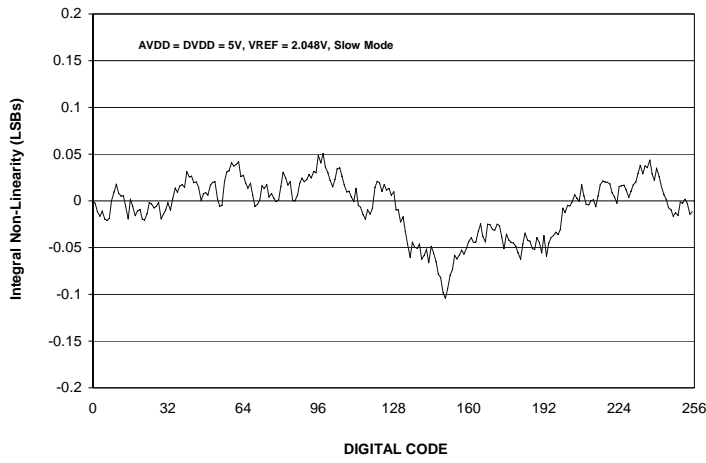


Figure 2 Integral Non-Linearity

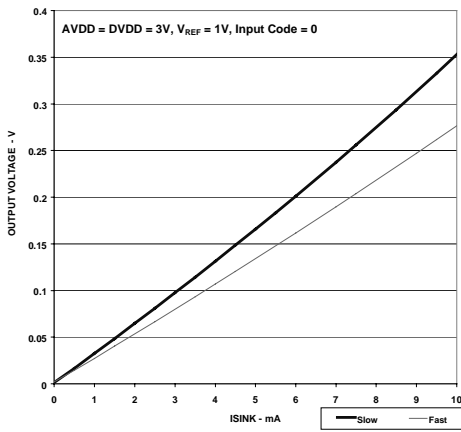


Figure 3 Sink Current AVDD = DVDD = 3V

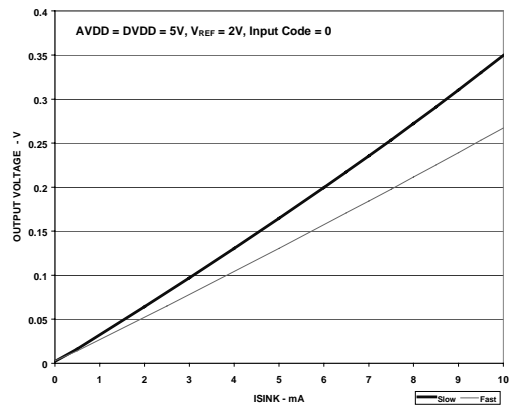


Figure 4 Sink Current AVDD = DVDD = 5V

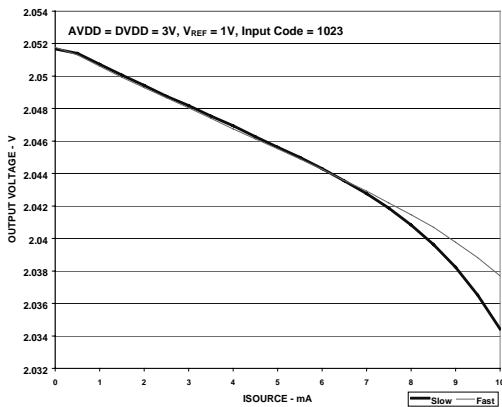


Figure 5 Source Current AVDD = DVDD = 3V

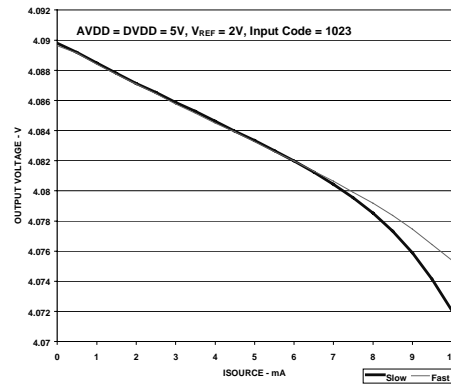


Figure 6 Sink Current AVDD = DVDD = 5V

DEVICE DESCRIPTION

GENERAL FUNCTION

The device uses a resistor string network buffered with an op amp to convert 8-bit digital data to analogue voltage levels (see Block Diagram). The output voltage is determined by the reference input voltage and the input code according to the following relationship:

$$V_{out} = 2(V_{REFIN}) \frac{CODE}{256}$$

INPUT		OUTPUT
1111	1111	$2(V_{REF}) \frac{255}{256}$
:	:	:
1000	0001	$2(V_{REF}) \frac{129}{256}$
1000	0000	$2(V_{REF}) \frac{128}{256} = V_{REF}$
0111	1111	$2(V_{REF}) \frac{127}{256}$
:	:	:
0000	0001	$2(V_{REF}) \frac{1}{256}$
0000	0000	0V

Table 1 Binary Code Table (0V to 2V_{REF} Output), Gain = 2

POWER ON RESET

An internal power-on-reset circuit resets the DAC registers to all 0s on power-up.

BUFFER AMPLIFIER

The output buffer has a near rail-to-rail output with short circuit protection and can reliably drive a 2kΩ load with a 100pF load capacitance.

EXTERNAL REFERENCE

The reference voltage input is buffered which makes the DAC input resistance independent of code. REFINAB and REFINCD pins have an input resistance of 10MΩ and an input capacitance of typically 5pF. The reference voltage determines the DAC full-scale output.

HARDWARE CONFIGURATION OPTIONS

DEVICE POWER DOWN

The device can be powered-down by pulling pin NPD (Pin 2) high. This powers down all DACs overriding their individual power down settings. This will reduce power consumption to typically 10nA. When the power down function is released the device reverts to the DAC code set prior to power down.

SIMULTANEOUS DAC UPDATE

The NLDAC pin (Pin 3) can be held high to prevent serial word writes from updating the DAC latches. By writing new values to multiple DACs then pulling NLDAC low, all new DAC codes are loaded into the DAC latches simultaneously.

SERIAL INTERFACE

To start transferring data, the device first has to be enabled with NCS set to low. Then, a falling edge of FS starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred, the next rising edge on SCLK or FS causes the content of the shift register to be moved to the DAC holding latch. If NLDAC is low, the DAC latch will also be updated immediately.

The serial interface of the device can be used in two basic modes:

- four wire (with chip select)
- three wire (without chip select)

Using chip select (four wire mode), it is possible to have more than one device connected to the serial port of the data source (DSP or microcontroller). If there is no need to have more than one device on the serial bus, then NCS can be tied low.

SERIAL CLOCK AND UPDATE RATE

Figure 1 shows the device timing. The maximum serial rate is:

$$f_{SCLKmax} = \frac{1}{t_{WCHmin} + t_{WCLmin}} = 20MHz$$

The digital update rate is limited to an 800ns period, or 1.25MHz frequency. However, the DAC settling time to 8 bits limits the update rate for large input step transitions.

SOFTWARE CONFIGURATION OPTIONS

The 16 bits of data can be transferred with the sequence shown in Table 2. D11-D2 contains the 8-bit data word. D15-D12 hold the programmable options.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A1	A0	PWR	SPD	New DAC value (8 bits)								0	0	0	0

Table 2 Register Map

DAC ADDRESSING

A particular DAC (A, B, C, D) within the device is selected by A1 and A0 within the input word.

A1	A0	DAC ADDRESS
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

PROGRAMMABLE SETTling TIME (SPD – BIT D12)

Settling time is a software selectable 2.5µs or 8.5µs, typical to within ±0.1LSB of final value. This is controlled by the value of SPD – Bit D12 and an associated DAC address. A ONE defines a settling time of 2.5µs, a ZERO defines a settling time of 8.5µs for that DAC.

PROGRAMMABLE POWER DOWN

The power down function is controlled by PWR - Bit D13 and an associated DAC address. A ZERO configures that DAC as active, a ONE configures that DAC into power down mode.

APPLICATIONS INFORMATION

LINEARITY, OFFSET, AND GAIN ERROR

Amplifiers operating from a single supply can have positive or negative voltage offsets. With a positive offset, the output voltage changes on the first code transition. However, if the offset is negative, the output voltage may not change with the first code, depending on the magnitude of the offset voltage. This is because with the most negative supply rail being ground, any attempt to drive the output amplifier below ground will clamp the output at 0 V. The output voltage then remains at zero until the input code is sufficiently high to overcome the negative offset voltage, resulting in the transfer function shown in Figure 7.

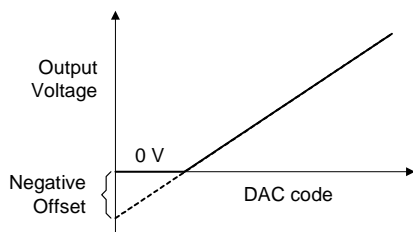


Figure 7 Effect of Negative Offset

This offset error, not the linearity error, produces the breakpoint. The transfer function would follow the dotted line if the output buffer could drive below the ground rail.

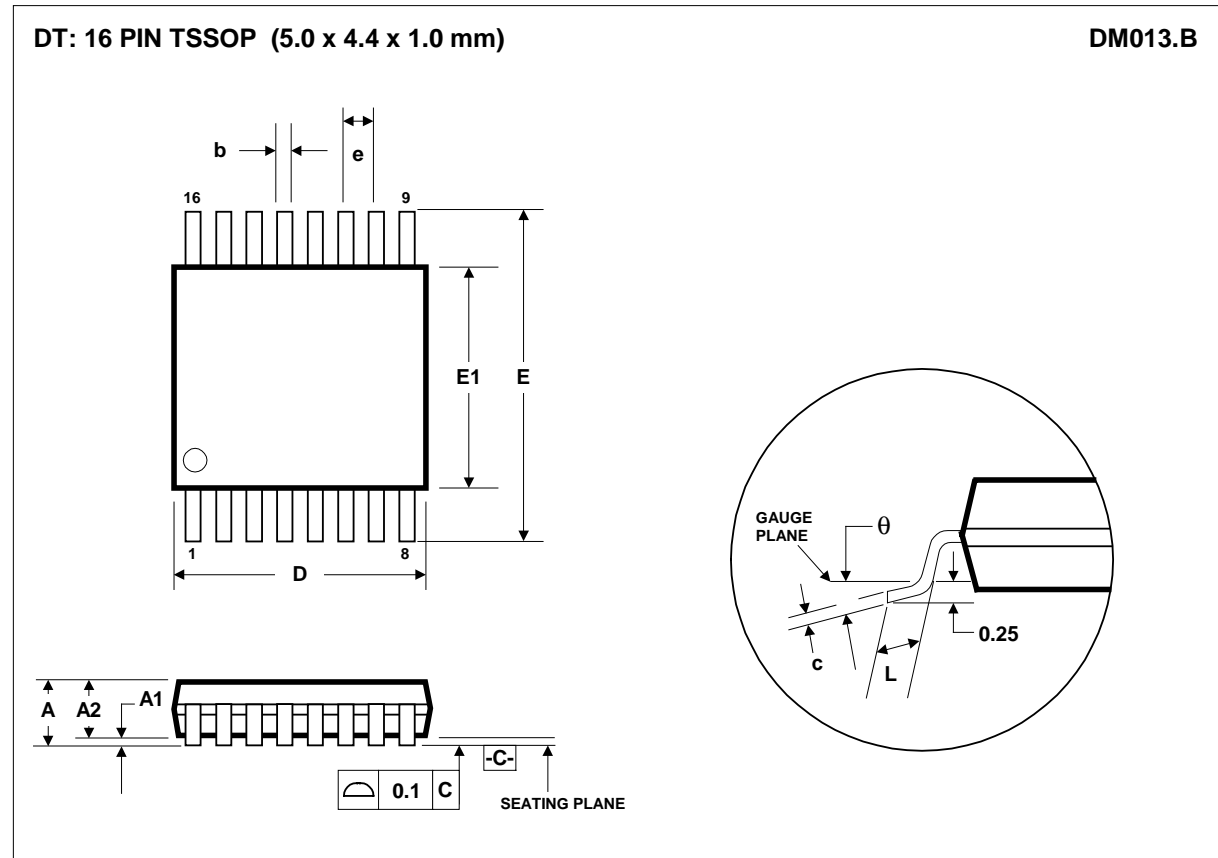
DAC linearity is measured between zero-input code (all input bits at 0) and full-scale code (all inputs at 1), disregarding offset and full-scale errors. However, due to the breakpoint in the transfer function, single supply operation does not allow for adjustment when the offset is negative. In such cases, the linearity is therefore measured between full-scale and the lowest code that produces a positive (non-zero) output voltage.

POWER SUPPLY DECOUPLING AND GROUNDING

Printed circuit boards with separate analogue and digital ground planes deliver the best system performance. The two ground planes should be connected together at the low impedance power supply source. Ground currents should be managed so as to minimise voltage drops across the ground planes.

A 0.1 μ F decoupling capacitor should be connected between the positive supply and ground pins of the DAC, with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analogue supply from the digital supply.

PACKAGE DIMENSIONS



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	1.20
A₁	0.05	-----	0.15
A₂	0.80	1.00	1.05
b	0.19	-----	0.30
c	0.09	-----	0.20
D	4.90	5.00	5.10
e	0.65 BSC		
E	6.4 BSC		
E₁	4.30	4.40	4.50
L	0.45	0.60	0.75
theta	0°	-----	8°
REF:	JEDEC.95, MO-153		

- NOTES:
 A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
 B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
 C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
 D. MEETS JEDEC.95 MO-153, VARIATION = AB. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.