XC2164 Series

ICs for use with Crystal Oscillators

TOREX

◆CMOS Low Power Consumption
◆Oscillation Frequency : 4MHz~ 125MHz
: 4MHz ~ 30MHz
(Fundamental Oscillation)
: 20MHz ~ 125MHz
(3rd Overtone Oscillation)
◆3-State Output
◆Built-in Capacitors Cg, Cd
◆Built-in Feedback Resistor
◆Chip form
◆Mini Mold SOT-26 Package

■APPLICATIONS

●Crystal oscillation modules
●Micro computer, DSP clocks
●Communication equipment
●Various system clocks

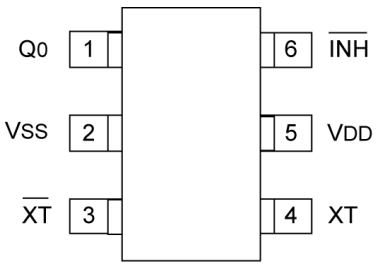
■GENERAL DESCRIPTION

The XC2164 series are high frequency, low current consumption CMOS ICs with built-in crystal oscillator and divider circuits.
For fundamental oscillation, output is selectable from any one of the following values for f0: f0/1, f0/2, f0/4, f0/8.
With oscillation capacitors and a feedback resistor built-in, it is possible to configure a stable fundamental oscillator or 3rd overtone oscillator using only an external crystal. Also the series has stand-by function built-in and the type, which suspends the oscillation completely (C/E type) or the type suspends only an output (O/E type) are available. The XC2164 series are integrated into SOT-26 packages. The series is also available in chip form.

■FEATURES

Oscillation Frequency : 4MHz ~ 30MHz (Fundamental)
20MHz ~ 125MHz(3rd Overtone)
Divider Ratio : Selectable from f0/1, f0/2, f0/4, f0/8
(f0/2, f0/4, f0/8 are fundamental only)
Output :3-State
Operating Voltage Range :3.3V±10%, 5.0V±10%
Low Power Consumption :Stand -by function included
Selectable from C/E type and
O/E type
Chip Form :Chip Size 1.3×0.8 mm
Ultra Small Package :SOT-26 mini mold

■PIN CONFIGURATION



SOT-26
(TOP VIEW)

■PIN ASSIGNMENT

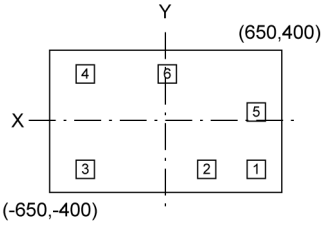
PIN NUMBER	PIN NAME	FUNCTION
1	Q0	Clock Output
2	VSS	Ground
3	/XT	Crystal Oscillator Connection (Output)
4	XT	Crystal Oscillator Connection (Input)
5	VDD	Power Supply
6	/INH	Stand-by Control*

*Stand-by control pin has a pull-up resistor built-in. unit [μm]

■/INH, Q0 PIN FUNCTION

/INH	Q0
“H” or OPEN	Clock Output
“L”	High impedance

■PAD LAYOUT FOR CHIP FORM



Size (Chip) : 1.3 × 0.8 mm
Thickness (Chip) : XC2164x51xxT : 280±20μ
: XC2164x51xxF : 200±20μ
Backside (Chip) : VDD Level
Aperture (Pad) : 100 × 100μ

■PAD DIMENSIONS

PIN NUMBER	PIN NANE	PAD DIMENSIONS	
		X	Y
1	Q0	514	- 264
2	VSS	222	- 264
3	/ XT	- 450	- 264
4	XT	- 450	264
5	VDD	514	27
6	/ INH	47	264

■ PRODUCT CLASSIFICATION

●Ordering Information

XC2164 ①②③④⑤⑥

DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
①	Divider Ratio & Stand-by Mode	A	: Chip Enable: f0/1
		B	: Chip Enable: f0/2 (Fundamental only)
		C	: Chip Enable: f0/4 (Fundamental only)
		D	: Chip Enable: f0/8 (Fundamental only)
		K	: Output Enable: f0/1
		L	: Output Enable: f0/2 (Fundamental only)
		M	: Output Enable: f0/4 (Fundamental only)
		N	: Output Enable: f0/8 (Fundamental only)
②	Fixed Number	5	: -
③	Duty Level	1	: CMOS (VDD/2) *TTL: Fundamental 4MHz to 30MHz
④	Frequency Range & Rf, Cg, Cd Values	(Table 1)	: 3rd Overtone, built-in type
		(Table 2)	: Fundamental, built-in type
⑤	Package	C	: Chip form
		M	: SOT-26
⑥	Device Orientation	R	: Embossed tape, standard feed
		L	: Embossed tape, reverse feed
		T	: Chip tray (Wafer thickness : 280±20μm)
		F	: Chip tray (Wafer thickness : 200±20μm)
		W	: Wafer

Table 1: 3rd Overtone, Built-In Type

SYMBOL	FREQUENCY RANGE		Rf (kΩ)	Cg (pF)	Cd (pF)
	3.3V ±10%	5.0V ±10%			
A	—	20MHz to 30MHz	9.0	21.5	21.5
B	20MHz to 30MHz	30MHz to 40MHz	6.5	20.0	20.0
C	30MHz to 40MHz	40MHz to 50MHz	5.0	16.0	16.0
D	40MHz to 50MHz	50MHz to 65MHz	3.5	14.0	14.0
E	50MHz to 65MHz	65MHz to 80MHz	2.8	12.5	12.5
F	65MHz to 80MHz	80MHz to 95MHz	2.5	10.0	10.0
H	80MHz to 95MHz	95MHz to 110MHz	2.2	8.0	8.0
K	95MHz to 110MHz	110MHz to 125MHz	2.0	7.0	7.0
L	110MHz to 125MHz	—	2.3	5.5	5.5

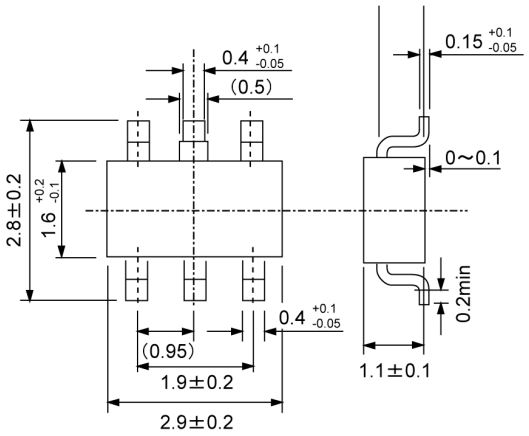
Table 2: Fundamental, Built-In Type

SYMBOL	FREQUENCY RANGE		Rf (kΩ)	Cg (pF)	Cd (pF)
	3.3V ±10%	5.0V ±10%			
M, V	4MHz to 30MHz	4MHz to 30MHz	3.5/7.0	20.0	20.0
T	4MHz to 30MHz	4MHz to 30MHz	3.5/7.0	35.0	35.0

(＊)Rf = 3.5MΩ@VDD = 5.0V Operation
Rf = 7.0 MΩ@VDD =3.3V Operation

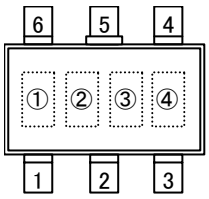
■ PACKAGING INFORMATION

●SOT-26



■ MARKING RULE

●SOT-26



SOT-26
(TOP VIEW)

①Represents product series

MARK
4

②Represents divider ratio

<Chip Enable>

MARK	RATIO	MARK	RATIO
A	f0/1	C	f0/4
B	f0/2	D	f0/8

*B, C, D: fundamental only

<Output Enable>

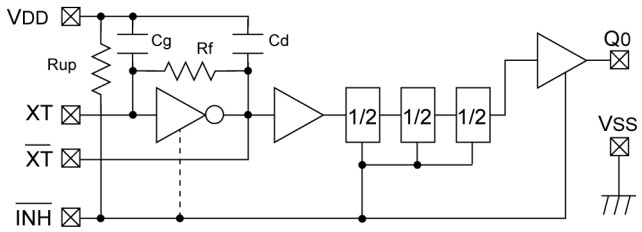
MARK	RATIO	MARK	RATIO
K	f0/1	M	f0/4
L	f0/2	N	f0/8

*L, M, N: fundamental only

③Represents recommended frequency & Rf, Cg &Cd values
*) Please refer to the ordering information, SYMBOL ① to ④

④Represents assembly lot number
(Based on internal standards)

■BLOCK DIAGRAM



Built-in oscillation capacitors, oscillation feedback resistor

■ABSOLUTE MAXIMUM RATINGS

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	UNITS
Supply Voltage	V_{DD}	V_{SS} - 0.3 ~ V_{SS} + 7.0	V
Input Voltage	V_{IN}	V_{SS} - 0.3 ~ V_{DD} + 0.3	V
Power Dissipation	Pd	250*	mW
Operating Temperature Range	Topr	- 40 ~ + 85	℃
Storage Temperature Range	Tstg	- 65 ~ + 150 (Chip Form)	℃
		- 55 ~ + 125 (SOT-26)	℃

** When implemented on a glass epoxy PCB. (SOT-26 package)

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

XC2164A51M, T, V / XC2164K51M, T, V (Fundamental)

5.0V operation (unless otherwise stated, V_{DD}=5.0V, No Load, Ta=-30~+80℃)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Operating Voltage	V_{DD}			4.5	5.0	5.5	V
"H" Level Input Voltage	V_{IH}			2.4	-	-	V
"L" Level Input Voltage	V_{IL}			-	-	0.4	V
"H" Level Output Voltage	V_{OH}	CMOS: V_{DD}=4.5V, I_{OH}=-16mA		3.9	4.2	-	V
"L" Level Output Voltage	V_{OL}	CMOS: V_{DD}=4.5V, I_{OH}=16mA		-	0.3	0.4	V
Supply Current 1	I_{DD1}	/I_{NH}=Open, Q0=Open f=30MHz	XC2164A51M, V	-	11	(15)	mA
			XC2164A51T	-	11	(15)	
			XC2164K51M, V	-	11	(15)	
			XC2164K51T	-	11	(15)	
Supply Current 2	I_{DD2}	/I_{NH}="L", Q0=Open f=30MHz	XC2164A51M, V	-	5	(8)	μA
			XC2164A51T	-	5	(8)	
			XC2164K51M, V	-	(T.B.D.*)	(T.B.D.*)	mA
			XC2164K51T	-	9	(14)	
Input Pull-Up Resistance 1	Rup1	/I_{NH}="L"		0.5	1.0	2.0	MΩ
Input Pull-Up Resistance 2	Rup2	/I_{NH}=0.7 V_{DD}		25	50	100	kΩ
Internal Oscillation Feedback Resistance	Rf			-	3.5	-	MΩ
Output Disable Leak Current	I_{OZ}	/I_{NH}="L"		-	-	10	μA

* T.B.D.: To be determined

XC2164A51M, XC2164K51M (Fundamental)

3.3V operation (unless otherwise stated, V_{DD}=3.3V, No Load, Ta=-30~+80℃)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Operating Voltage	V_{DD}			2.97	3.30	3.63	V
"H" Level Input Voltage	V_{IH}			2.4	-	-	V
"L" Level Input Voltage	V_{IL}			-	-	0.4	V
"H" Level Output Voltage	V_{OH}	CMOS: V_{DD}=2.97V, I_{OH}=-8mA		2.5	-	-	V
"L" Level Output Voltage	V_{OL}	CMOS: V_{DD}=2.97V, I_{OH}=8mA		-	-	0.4	V
Supply Current 1	I_{DD1}	/I_{NH}=Open, Q0=Open, f=30MHz	XC2164A51M	-	5	(8)	mA
			XC2164K51M	-	(T.B.D.*)	(T.B.D.*)	
Supply Current 2	I_{DD2}	/I_{NH}="L", Q0=Open, f=30MHz	XC2164A51M	-	2	(4)	μA
			XC2164K51M	-	(T.B.D.*)	(T.B.D.*)	mA
Input Pull-Up Resistance 1	Rup1	/I_{NH}="L"		1.0	2.0	4.0	MΩ
Input Pull-Up Resistance 2	Rup2	/I_{NH}=0.7 V_{DD}		35	70	140	kΩ
Internal Oscillation Feedback Resistance	Rf			-	7.0	-	MΩ
Output Disable Leak Current	Id	/I_{NH}="L"		-	-	10	μA

* T.B.D.: To be determined

■ELECTRICAL CHARACTERISTICS (Continued)

XC2164A51T, V / XC2164K51T, V (Fundamental)

3.3V operation (unless otherwise stated, V_{DD}=3.3V, No Load, Ta=-30~+80℃)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Operating Voltage	V_{DD}			2.50	3.30	3.63	V
"H" Level Input Voltage	V_{IH}			2.4	-	-	V
"L" Level Input Voltage	V_{IL}			-	-	0.4	V
"H" Level Output Voltage	V_{OH}	CMOS: 2.97V, I_{OH}=-8mA		2.5	-	-	V
"L" Level Output Voltage	V_{OL}	CMOS: 2.97V, I_{OH}=8mA		-	-	0.4	V
Supply Current 1	I_{DD1}	/INH=Open, Q0=Open, f=30MHz	XC2164A51T	-	4	(6.5)	mA
			XC2164A51V	-	5	(8)	
			XC2164K51T	-	4	(6.5)	
			XC2164K51V	-	5	(8)	
Supply Current 2	I_{DD2}	/INH="L", Q0=Open, f=30MHz	XC2164A51T	-	2	(4)	μA
			XC2164A51V	-	2	(4)	
			XC2164K51T	-	(T.B.D.*)	(T.B.D.*)	mA
			XC2164K51V	-	(T.B.D.*)	(T.B.D.*)	
Input Pull-Up Resistance 1	Rup1	/INH="L"		1.0	2.0	4.0	MΩ
Input Pull-Up Resistance 2	Rup2	/INH=0.7 V_{DD}		35	70	140	kΩ
Internal Oscillation Feedback Resistance	Rf			-	7.0	-	MΩ
Output Disable Leakage Current	I_{OZ}	/INH="L"		-	-	10	μA

* T.B.D.: To be determined

Comparative Chart of Oscillation Frequency vs. Supply Voltage, and Negative Resistance Value

SYMBOL	OSCILLATION FREQUENCY vs. SUPPLY VOLTAGE		NEGATIVE RESISTANCE VALUE	
	V_{DD}=3.3V±10%	V_{DD}=5.0V±10%	V_{DD}=3.3V	V_{DD}=5.0V
M	±4.3ppm	±4.5ppm	-130Ω	-220Ω
V	±1.2ppm	±2.1ppm	-150Ω	-250Ω
T	±9.4ppm	±7.0ppm	-660Ω	-760Ω

(The designed value when 30MHz crystal is used.)

■ELECTRICAL CHARACTERISTICS (Continued)

XC2164A51A ~ XC2164A51K (3rd Overtone)

5.0V Operation (Unless otherwise stated, V_{DD}=5.0V, No Load, Ta=-30~+80℃)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Operating Voltage	V_{DD}			4.5	5.0	5.5	V
"H" Level Input Voltage	V_{IH}			2.4	-	-	V
"L" Level Input Voltage	V_{IL}			-	-	0.4	V
"H" Level Output Voltage	V_{OH}	CMOS: 4.5V, I_{OH}=-16mA		3.9	4.2	-	V
"L" Level Output Voltage	V_{OL}	CMOS: 4.5V, I_{OH}=16mA		-	0.3	0.4	V
Supply Current 1	I_{DD1}	/I_{NH}=Open, Q_0=Open	XC2164A51A, f0=30MHz	-	17.0	(23)	mA
			XC2164A51B, f0=40MHz	-	17.0	(23)	
			XC2164A51C, f0=55MHz	-	19.0	(26)	
			XC2164A51D, f0=70MHz	-	23.0	(32)	
			XC2164A51E, f0=85MHz	-	24.0	(32)	
			XC2164A51F, f0=100MHz	-	30.0	(40)	
			XC2164A51H, f0=110MHz	-	30.0	(40)	
			XC2164A51K, f0=125MHz	-	30.0	(40)	
Supply Current 2	I_{DD2}	/I_{NH}="L", Q0=Open		-	5.0	(8)	μA
Input Pull-Up Resistance 1	Rup1	/I_{NH}="L"		0.5	1.0	2.0	MΩ
Input Pull-Up Resistance 2	Rup2	/I_{NH}=0.7 V_{DD}		25	50	100	kΩ
Internal Oscillation Feedback Resistance	Rf	XC2164A51A		-	9.0	-	kΩ
		XC2164A51B		-	6.5	-	
		XC2164A51C		-	5.0	-	
		XC2164A51D		-	3.5	-	
		XC2164A51E		-	2.8	-	
		XC2164A51F		-	2.5	-	
		XC2164A51H		-	2.2	-	
		XC2164A51K		-	2.0	-	
Output Disable Leak Current	I_{OZ}	/I_{NH}="L"		-	-	10	μA

■ELECTRICAL CHARACTERISTICS (Continued)

XC2164A51B, C, E, F, H, K, L (3rd Overtone)

3.3V Operation (unless otherwise stated, V_{DD}=3.3V, No Load, Ta=-30~+80℃)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Operating Voltage	V_{DD}			2.97	3.30	3.63	V
"H" Level Input Voltage	V_{IH}			2.4	-	-	V
"L" Level Input Voltage	V_{IL}			-	-	0.4	V
"H" Level Output Voltage	V_{OH}	CMOS: 2.97V, I_{OH}=-8mA		2.5	-	-	V
"L" Level Output Voltage	V_{OL}	CMOS: 2.97V, I_{OH}=8mA		-	-	0.4	V
Supply Current 1	I_{DD1}	/I_{NH}=Open, Q0=Open	XC2164A51B, f0=30MHz	-	4.5	(7)	mA
			XC2164A51C, f0=40MHz	-	5.0	(8)	
			XC2164A51E, f0=70MHz	-	8.0	(13)	
			XC2164A51F, f0=85MHz	-	8.5	(13)	
			XC2164A51H, f0=100MHz	-	9.5	(15)	
			XC2164A51K, f0=110MHz	-	10.0	(15)	
			XC2164A51L, f0=125MHz	-	10.5	(15)	
Supply Current 2	I_{DD2}	/I_{NH}="L", Q_0=Open		-	2.0	-	μA
Input Pull-Up Resistance 1	Rup1	/I_{NH}="L"		1.0	2.0	4.0	MΩ
Input Pull-Up Resistance 2	Rup2	/I_{NH}=0.7 V_{DD}		35	70	140	kΩ
Internal Oscillation Feedback Resistance	Rf	XC2164A51B		-	6.5	-	kΩ
		XC2164A51C		-	5.0	-	
		XC2164A51E		-	2.8	-	
		XC2164A51F		-	2.5	-	
		XC2164A51H		-	2.2	-	
		XC2164A51K		-	2.0	-	
		XC2164A51L		-	2.3	-	
Output Disable Leak Current	I_{OZ}	/I_{NH}="L"		-	-	10	μA

XC2164A51D (3rd Overtone)

3.3V Operation (Unless otherwise stated, V_{DD}=3.3V, Oscillation Frequency f0=48MHz, Ta=30~+80℃)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Operating Voltage	V_{DD}			2.70	3.30	3.63	V
'H' Level Input Voltage	V_{IH}			2.4	-	-	V
'L' Level Input Voltage	V_{IL}			-	-	0.4	V
'H' Level Output Voltage	V_{OH}	CMOS: 2.97V, I_{OH}=-8mA		2.5	-	-	V
'L' Level Output Voltage	V_{OL}	CMOS: 2.97V, I_{OH}=8mA		-	-	0.4	V
Supply Current 1	I_{DD1}	/I_{NH}=Open, Q0=Open	XC2164A51D, F0=55MHz	-	6.5	(10)	mA
Supply Current 2	I_{DD2}	/I_{NH} = 'L', Q0=Open		-	2.0	-	μA
Input Pull-Up Resistance 1	Rup1	/I_{NH} = 'L'		1.0	2.0	4.0	MΩ
Input Pull-Up Resistance 2	Rup2	/I_{NH} = 0.7V_{DD}		35	70	140	kΩ
Internal Oscillation Feedback Resistance	Rf	XC2164A51D		-	3.5	-	kΩ
Output Disable Leak Current	I_{OZ}	/I_{NH} = 'L'		-	-	10	μA

■SWITCHING CHARACTERISTICS

XC2164A51M, T, V (Fundamental) <Chip Enable> (unless otherwise stated, V_{DD}=3.3V or 5.0V, Ta=-30~+80℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise Time (*1)	tr	CMOS: C_L=15pF, 0.1V_{DD}→0.9V_{DD}	-	1.5	-	ns
		TTL: Load=10TTL, 0.4V →2.4V	-	1.5	-	ns
Output Fall Time (*1)	tf	CMOS: C_L=15pF, 0.9V_{DD}→0.1V_{DD}	-	1.5	-	ns
		TTL: Load=10TTL, 2.4V →0.4V	-	1.5	-	ns
Output Duty Cycle	DUTY	CMOS: C_L=15pF @ 0.5V_{DD}	45	-	55	%
		TTL: Load=10TTL, 1.4V	45	-	55	%
Output Disable Delay Time (*1)	tplz	f0=4MHz, C_L=15pF	-	-	100	ns
Output Enable Delay Time (*1)	tplz	f0=4MHz, C_L=15pF	-	-	6	ms
Oscillation Start Time (*1)	tosc_on	f0=4MHz, C_L=15pF	-	-	6	ms

*1: the values are the designed values.

XC2164A51A～L (3rd Overtone) <Chip Enable> (unless otherwise stated, V_{DD}=3.3V or 5.0V, Ta=-30~+80℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise Time (*1)	tr	CMOS: C_L=15pF, 0.1V_{DD}→0.9V_{DD}	-	1.5	-	ns
		TTL: Load=10TTL, 0.4V →2.4V	-	1.5	-	ns
Output Fall Time (*1)	tf	CMOS: C_L=15pF, 0.9V_{DD}→0.1V_{DD}	-	1.5	-	ns
		TTL: Load=10TTL, 2.4V →0.4V	-	1.5	-	ns
Output Duty Cycle	DUTY	CMOS: C_L=15pF @ 0.5V_{DD}	45	-	55	%
		TTL: Load=10TTL, 1.4V	45	-	55	%
Output Disable Delay Time (*1)	tplz	f0=20MHz, C_L=15pF	-	-	100	ns
Output Enable Delay Time (*1)	tplz	f0=20MHz, C_L=15pF	-	-	6	ms
Oscillation Start Time (*1)	tosc_on	f0=20MHz, C_L=15pF	-	-	6	ms

*1: the values are the designed values.

XC2164K51M, T, V (Fundamental) <Output Enable>

(unless otherwise stated, V_{DD}=3.3V or 5.0V, Ta=-30~+80℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise Time (*1)	tr	CMOS: C_L=15pF, 0.1V_{DD}→0.9V_{DD}	-	1.5	-	ns
		TTL: Load=10TTL, 0.4V →2.4V	-	1.5	-	ns
Output Fall Time (*1)	tf	CMOS: C_L=15pF, 0.9V_{DD}→0.1V_{DD}	-	1.5	-	ns
		TTL: Load=10TTL, 2.4V →0.4V	-	1.5	-	ns
Output Duty Cycle	DUTY	CMOS: C_L=15pF @ 0.5V_{DD}	45	-	55	%
		TTL: Load=10TTL, 1.4V	45	-	55	%
Output Disable Delay Time (*1)	tplz	f0=4MHz, C_L=15pF	-	-	100	ns
Output Enable Delay Time (*1)	tplz	f0=4MHz, C_L=15pF	-	-	10	μs
Oscillation Start Time (*1)	tosc_on	f0=4MHz, C_L=15pF	-	-	6	ms

*1: the values are the designed values.

* The values shown are preliminary so that the values may be changed without a prior announcement.

■SWITCHING WAVEFORMS

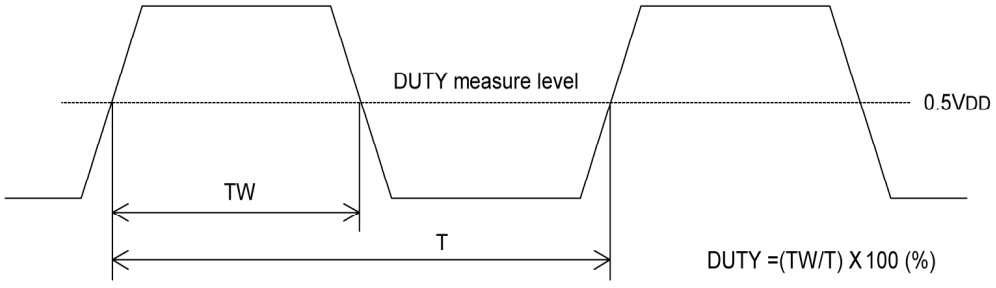
● Switching Time

(1) CMOS Output

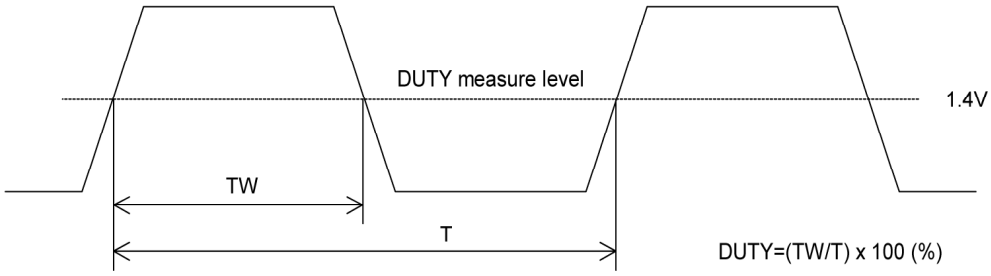
(2) TTL Output

● Duty Cycle

(1) CMOS Output

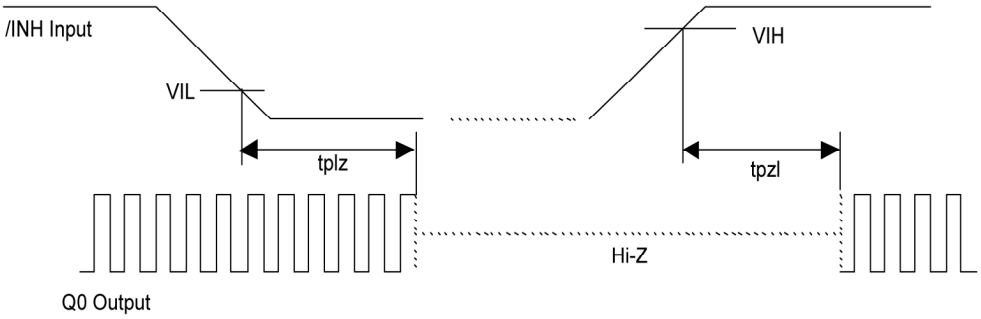


(2) TTL Output



■SWITCHING WAVEFORMS(Continued)

(3) Output Disable Delay Time, Output Enable Delay Time *) / INH pin input waveform: less than tr=tf=10ns, VDD Input



(4) Oscillation Start Time: tosc_on *) VDD pin input waveform : less than tr=tf=10ns, /INH=Open