DESIGN GUIDE FOR THE Si3210/15/16 DC-DC CONVERTER

Introduction

The ProSLIC® from Silicon Laboratories integrates a complete analog telephone interface into one low-voltage CMOS device and offers extensive software programmability to meet many global telephony requirements and customer specifications. In addition to performing all BORSCHT functions, the Si321x also dynamically generates and controls its own battery voltage, eliminating the need for external battery supplies. Two different battery generation architectures are supported: a BJT/inductor design offering a low-cost battery supply solution, and a MOSFET/transformer design offering increased power efficiency and a wider range of input voltages. This application note gives specific guidance in determining dc-dc converter power

requirements and selecting component values for each of the dc-dc converter architectures.

Si321x DC-DC Converter Description

The dc-dc converter dynamically generates the large negative voltages required to operate the linefeed interface. The Si321x acts as the controller for a buck-boost dc-dc converter that converts a positive dc voltage into the desired negative battery voltage. In addition to eliminating external power supplies, this allows the Si321x to minimize power dissipation by dynamically controlling the battery voltage to the minimum required for any given mode of operation.
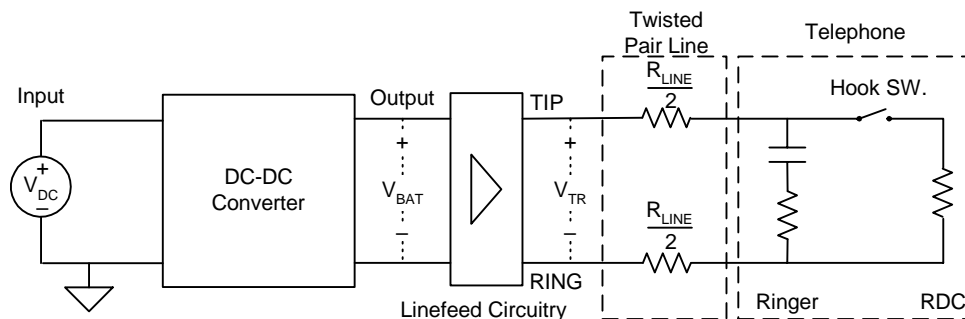
Figure 1. Linefeed Power Diagram

Power Output Requirement

Understanding the maximum power required by the ProSLIC linefeed circuitry to operate a worst-case specified load is the first step in determining the dc-dc converter design solution. Figure 1 defines the linefeed circuit and load circuit in basic blocks of circuitry.

Typically, the ringing state is the highest power consumption state for the SLIC, but in special cases the off-hook state can have the highest. Guidance in calculating each of these states is offered in this section.

The ringer impedance of one telephone is defined as an 8 μF cap in series with a 6930 Ω resistor. This is approximately the same impedance as 7000 Ω at 20 Hz and is defined as 1 REN (ringing equivalence number). Since there can be N number of telephones connected

in parallel to the TIP and RING lines, the equivalent impedance of the parallel ringers can be computed as the following (NREN is limited to 1 to 5):

$$R_{NREN} = \frac{7000}{NREN}$$

During ringing, the TIP-to-RING peak voltage, V_{TR_PK}, is the sum of the rms voltage drop across the ringer circuit, $V_{RINGrms}$, the line resistance, and the internal source resistance of 160 Ω.

$$V_{TR\_PK} = \frac{V_{RINGrms} \times \sqrt{2}}{7000 / NREN} \times \left(\frac{7000}{NREN} + R_{LINE} + R_s \right)$$

Considering the resistance of 26 gauge telephone wire, which is 0.45 Ω per feet, this equation becomes the following:

$$V_{TR\_PK} = \frac{V_{RINGrms} \times \sqrt{2}}{7000/NREN} \times \left(\frac{7000}{NREN} + 2 \times Dist \times 0.045 + 160 \right)$$
Equation 1

The required V_{BAT} is equal to V_{TR_PK} plus VCMR, which is the voltage drop across the linefeed circuit. The VCMR voltage is set by the indirect Register 40 and recommended to be 1.5 V for most applications.

$$V_{BAT} = V_{TR\_PK} + VCMR$$
Equation 2

The worst-case peak current for NREN load is when the load is connected with a short loop of negligible line resistance.

$$I_{PK} = \frac{V_{TR\_PK}}{(7000/NREN)}$$

This yields an average current equation:

$$I_{AVG} = I_{PK} \times \frac{2}{\pi} = \frac{2 \times NREN \times V_{TR\_PK}}{7000\pi}$$

Equation 3

The total output power required during ringing is equal to the power consumed in the load plus the power consumed in the sensing resistors and the external transistors of the linefeed circuitry. This leakage current has a magnitude of 2.5 mA.

$$P_{OUT} = V_{BAT} \times (I_{AVG} + 0.0025)$$

Equation 4

In the Off-Hook State

In a few special cases, the power consumed during off-hook is higher than the power consumed during ringing. It is important to check for this and design the power supply to handle the larger power requirement. Most designers can skip this section unless their designs support long line and/or the brief on-hook voltage measurement (for caller ID 2 and 2.5) with TRACK = 0 (bit 0 of the direct Register 66).

The output current equations in the off-hook active state are as follows:

$$I_{BAT} = I_{LIM} + I_{BJTBIAS} + \left(\frac{0.6 \ V + 80(I_{LIM} + I_{BJTBIAS})}{5100} \right)$$
Equation 5

where I_{LIM} is the current limit set by Register 71, and $I_{BJTBIAS}$ is the bipolar biasing current set by the direct Register 65.

There are two power equations for different track settings. For TRACK = 1, V_{BAT} is allowed to track the line resistance to minimize power consumption. The power equation for this mode is as follows:

$$P_{OFFHOOK} = I_{BAT}(V_{CM} + V_{OV} + I_{LIM} \times R_{LOOPMAX})$$
Equation 6

where V_{CM} is set by the direct Register 73, and V_{OV} is set by Register 66. $R_{LOOPMAX}$ is the maximum total loop resistance (R_{LINE} + Phone's R_{DC} + R_S) where R_S is the internal series resistance.

For TRACK = 0, V_{BAT} can ramp up quickly to support the brief on-hook voltage measurement feature, the power equation is as follows:

$$P_{OFFHOOK} = I_{BAT} \times V_{BATL}$$
Equation 7

where V_{BATL} is set by the direct Register 75.

If the off-hook power consumption is greater than the power during ringing, the dc-dc converter should be designed based on the off-hook current and off-hook V_{BAT}. However, the requirement for the switching components (Q7 and Q8 or M1) should still be based on the V_{BAT} value during ringing.

Power Input Requirement

The input power is equal to the output power plus the wasted power during the power conversion process. The efficiency of the Si321x dc-dc converter is mainly dependent on the inductor loss (copper and magnetic loss) and the switching loss. For worst-case estimation, the efficiency is assumed to be 60% for the BJT/inductor solution (the actual efficiency is between 63% and 73%) and 75% for the MOSFET/transformer solution (the actual efficiency is between 75% and 83%.)

$$P_O = P_{IN} \times Power \ Efficiency = I_{IN} \times V_{IN} \times Power \ Efficiency$$

Solving for I_{IN}:

$$I_{IN} = \frac{P_O}{(V_{IN} \times Power \ Efficiency)}$$
Equation 8

The input voltage to the dc-dc converter could drop quickly (depending on the source impedance) as the

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input current rises. The V_{IN} minimum is defined as the input voltage level at the maximum input current defined in Equation 8. It is important that the V_{IN} minimum is used as the V_{DC} in the design calculation to prevent the dc-dc converter from receding below the low-voltage lock-out threshold, which could cause the dc-dc converter to shut down prematurely.

Component Selection for BJT/Inductor

Solution

The typical circuit application for the BJT/inductor version of the Si321x dc-dc converter is shown in Figure 2. Components in this circuit are discussed, and detailed descriptions for each functional block are provided to guide the designer through the component value selection process.
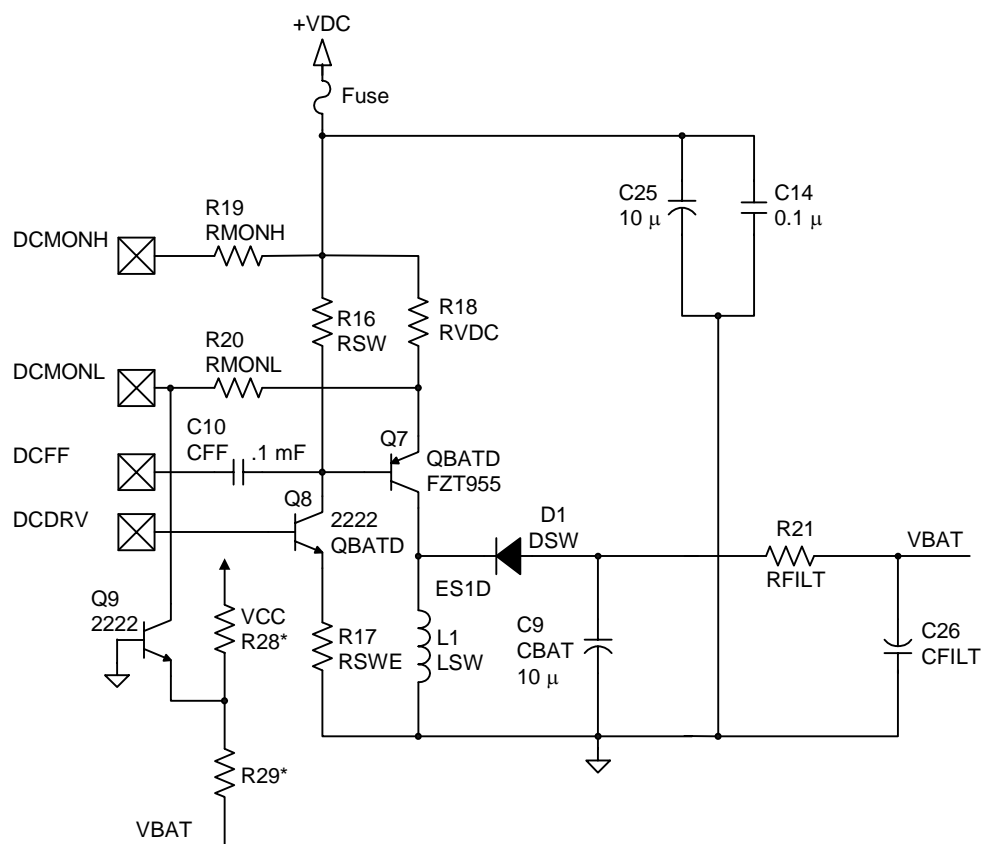

Figure 2. Typical Application Circuit

Power Inductor Design Equation

The L1 inductor is the main power component in the Si321x dc-dc converter. Energy from the input is stored into the L1 during Q7 switch transistor on-time and released to the output during Q7 off-time. The amount of this energy is directly proportional to the inductance of the inductor and to the square of the maximum current that flows through the inductor during on-time.

$$E = \frac{L \times I_{MAX}^{2}}{2}$$

The inductor power equation is derived as the energy over time:

$$P_{IND} = \frac{E}{T} = \frac{L \times I_{MAX}^{2}}{2T} = \frac{L \times I_{MAX}^{2} \times Fs}{2}$$

where Fs is the switching frequency of the Q7 transistor.

This frequency represents the number of times that the energy transfers from the input to the output via the inductor per second.

The output power can be related to inductor power with the efficiency factor, which is defined as the ratio of the output power over the input power.

$$P_{OUT} = E_{FF} \times P_{IND} = E_{FF}\left(\frac{L \times I_{MAX}^{2} \times Fs}{2}\right)$$

Equation 9

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In the Discontinuous Switching mode, the current flowing in the inductor always starts at 0 A at the beginning of on-time of Q7, peaks at the end of the on-time, and goes back to zero at the end of off-time.

During on-time, V_{DC} is presented across the L1 inductor and the current flow increases linearly (see Figure 3) with respect to the on-time duration of Q7. The rate of the current increase depends on V_{DC} and the inductance of L1.

$$i(t) = \frac{V_{DC}}{L} \times t$$

As the output demands more energy, the Si321x lengthens Q7 on-time to increase the L1 inductor

current. This increase in the inductor current raises storage energy in L1; Therefore, more energy is available to the output when Q7 is off. The inductor current reaches its peak I_{PK} at t_{ONMAX}.

$$I_{PK} = \frac{V_{DC}}{L} \times t_{ONMAX}$$

So, the maximum on-time is as follows:

$$t_{ONMAX} = \frac{I_{PK} \times L}{V_{DC}}$$

The off-time equivalent circuit is shown in Figure 4. Q7 is off and the inductor current follows the diode, D1, to the C9 output capacitor and the R_{LOAD}.
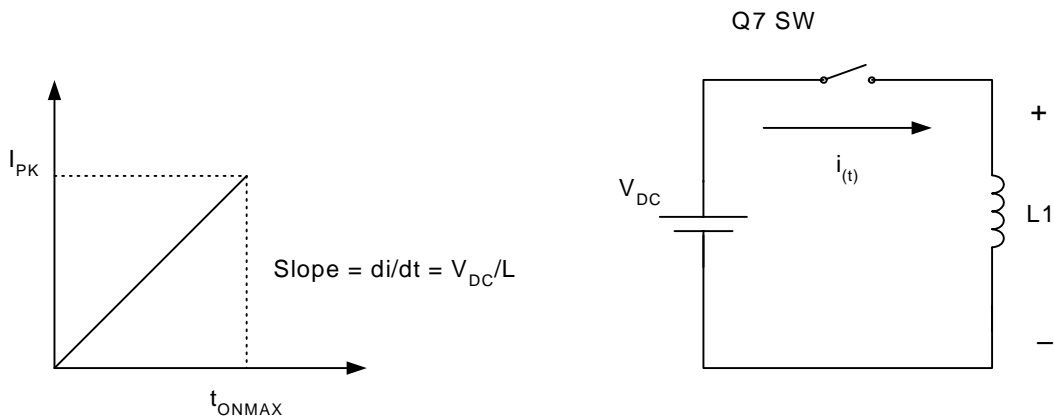

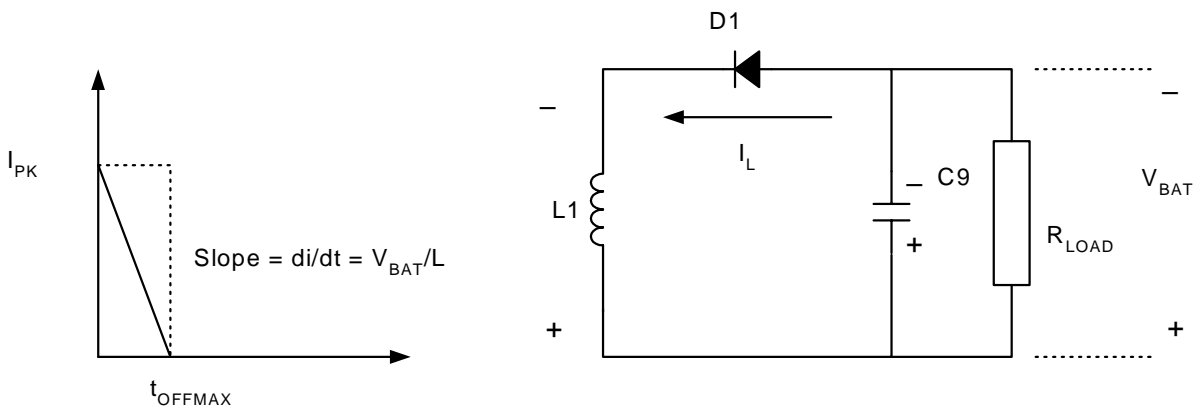**Figure 3. L1 Current Flow during Q7 On-Time**

Figure 4. L1 Current Flow during Q7 Off-Time

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The voltage across the inductor during this time is equal to V_{BAT} less the D1 diode voltage drop or approximately V_{BAT}. Since V_{BAT} is greater than V_{DC}, the rate of current change is faster compared to the current slope during on-time. The inductor current starts from I_{PK} and descends to 0 A at t_{OFFMAX}.

$$\frac{I_{PK}}{t_{OFFMAX}} = \frac{V_{BAT}}{L}$$

So the maximum off-time is as follows:

$$t_{OFFMAX} = \frac{I_{PK} \times L}{V_{BAT}}$$
Equation 10

The period of the switching frequency, Fs, is equal to the reciprocal of the maximum on-time plus maximum off-time:

$$Fs = \frac{1}{t_{ONMAX} + t_{OFFMAX}} = \frac{1}{I_{PK} \times L/V_{DC} + I_{PK} \times L/V_{BAT}}$$

Substituting the above expression for the power Equation 8:

$$P_{OUT} = E_{FF} \times P_{IND} = E_{FF}\left(\frac{L \times I_{PK}^2 \times Fs}{2}\right)$$
Equation 11

And solving for I_{PK}:

$$I_{PK} = \frac{2P_{OUT}(V_{BAT} + V_{DC})}{E_{FF} \times V_{BAT} \times V_{DC}}$$
Equation 12

Solving for L from Equation 11, the required inductance is expressed as:

$$L = \frac{2P_{OUT}}{E_{FF} \times I_{PK}^2 \times Fs}$$
Equation 13

The optimum switching frequency of the Si321x dc-dc converter is between 64 kHz and 85 kHz. Faster switching frequency is generally less efficient. This is a common characteristic of the PNP switching element and low-cost inductor magnetic material.

Power Inductor Selection

Once output power (P_{OUT}), V_{DC}, and V_{BAT} are clearly defined, the inductor can be selected as follows:

1. Calculate I_{PK} based on Equation 12 (assumed 60% efficiency). This is the maximum current requirement for the inductor.

2. Calculate the inductance, L, based on Equation 13 assuming worst case 60% efficiency. Since inductors tend to have tolerances in the range of ±5% to ±30%, the minimum value of inductance must be equal to the calculated value of the inductor. Vary Fs from 64 kHz to 128 kHz to obtain the desired inductance value.

3. Calculate the period, T, for Fs and the corresponding value for direct Register 92 in hexadecimal.

$$\text{PWM Period Register 92} = \frac{T}{61 \text{ ns}}$$
Equation 14

4. Calculate the maximum off-time and the corresponding value for direct Register 93 in hexadecimal.

$$\text{Direct Register 93} = \frac{t_{OFFMAX}}{61 \text{ ns}} = \frac{(I_{PK} \times L)/V_{BAT}}{61 \text{ ns}}$$
Equation 15

Selecting a DC-DC Converter Switching Transistor

The switching transistor (Q7) on the typical application circuit is shown in Figure 2 on page 3. This transistor is turned on by the base drive current through Q8 while R16 provides the discharge current path for Q7's base-emitter capacitor during turn-off. The capacitor, C10, provides additional charge pump boost current from the DCFF pin of the Si321x to turn Q7 off faster. C10 with a value of 22 nF is sufficient for most applications. R16 plays an important role in turning off the Q7 transistor, but R16 also robs the Q7 base drive current during the on-time. With a value of 200 Ω, R16 does an adequate job of turning Q7 off and only takes 3 mA from the base current during on-time.

$$R16 = \frac{0.6}{I_{R16}}$$
Equation 16

Table 1 lists the requirements for the switching transistor, Q7.

Table 1. Switching Transistor Q7

$V_{CEO} > |V_{BAT}| + V_{DC}$
$V_{EBO} > V_{CC}$
$V_{CBO} > |V_{BAT}| + V_{CC} + V_{DC}$
$I_{CMAX} > I_{PK}$ (maximum Inductor current)
$f_T > 100$ MHz

Another critical specification is the transistor gain at I_{CMAX}. The higher the transistor gain (h_{FE}), the less base current is required to keep it in saturation during

on-time and the more efficient the converter will be since the base current is not delivered to the load. Also, as more base current is required, it becomes more difficult for the DCDRV and DCFF pins to switch the transistor off quickly, which further decreases efficiency. Practically, Q7 gain should be around 100 at peak inductor current.

Si321x Bipolar Switch Driver

In Figure 2, the Q8 collector current provides the base current drive that turns the switch transistor Q7 on. The base current drive should be sufficient to keep Q7 in saturation at I_{PK}. The overdrive factor of 1.3 is sufficient.

$$\frac{I_{CMAX}}{I_{BQ7}} < h_{FEmin@ICmax}$$

$$I_{BQ7} = 1.3 \times \frac{I_{CMAX}}{h_{FEmin@ICmax}}$$

Equation 17

The Si321x sets the DCDRV pin high to create the base current drive through Q8. The values of R17 and V_{CC} control the base drive current.

$$I_{BQ7} = \frac{V_{CC} - 0.6\ V}{R_{17}} - \frac{0.6\ V}{R_{16}}$$

$$R_{17} = \frac{V_{CC} - 0.7\ V}{I_{BQ7} + 0.6\ V / R_{16}}$$

Equation 18

Transistor requirements for Q8:

$V_{CEO} > V_{CC} + V_{DC}$
$V_{EBO} > V_{CC}$
$V_{CBO} > V_{CC} + V_{DC}$
$f_T > 200\ MHz$

Selecting Output Capacitor and Filter

The output capacitor, C9, is subject to large ac currents from the inductor and should have low equivalent series resistance (ESR) to minimize ripple voltage on V_{BAT}.

$$V_{RIPPLE} = ERS_{MAX} \times I_{PK}$$

Equation 19

A 10 μF, 100 V electrolytic capacitor provides adequate filtering in most applications.

An RC filter between C9 and the load reduces ripple voltage on the V_{BAT} output. This filter should have a

time constant of less than 100 μs to maintain loop stability. See CFILT and RFILT in Figure 2. (Recommended values for these two components are .1 μF and 15 Ω, respectively.)

Undervoltage and Overcurrent Protection

The Si321x dc-dc converter is designed to operate under a specific input voltage and output loading condition. When the input voltage goes too low, there is not enough power from the input to deliver to the output; so, the dc-dc converter may try to draw excessive current in an attempt to deliver power to the output. A similar condition exists when the output ramps up too fast (during power up, transient loading), short loads, or unintentionally overloads the output. To prevent damage to the switching transistor during these abnormal conditions, the Si321x implements an undervoltage and overcurrent mechanism.
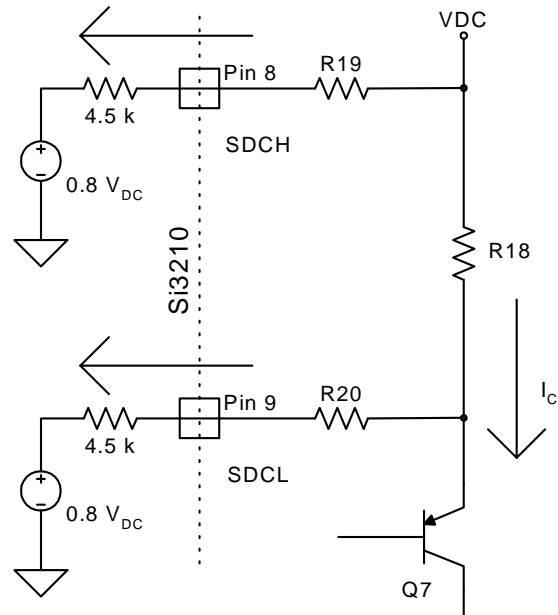
Figure 5. Protection Sense Circuitry

Undervoltage Lock-Out

The undervoltage lock-out is implemented via the SDCH pin as shown in Figure 5. When the V_{DC} goes under a specified value, the current flow through R19 into the SDCH pin goes under 120 μA, and it triggers the Si321x to shut off the dc-dc converter. The equation for R19 with a specific V_{DC} is given by the following:

$$R_{19} = \frac{\frac{VDC}{1.5} - 0.8}{120\ \mu A} - 4.5\ k\Omega$$

Equation 20

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R19 should be calculated with a 20% lower value in V_{DC} to prevent premature low-voltage lock-out. If the voltage lock-out is activated too often or if the Si321x goes in and out of low-voltage lock-out and creates an oscillation-like condition at the input voltage, it indicates that the input power source has high impedance and should be replaced with a better power source. However, the values of R18, R19, and R20 should be checked against the intended low-voltage lock-out before any conclusion is made about the input power source.

Overcurrent Protection

Overcurrent protection is implemented via the SDCL pin. (See Figure 5.) The circuit is designed to produce equal current flow from V_{DC} to both the SDCL and SDCH pins with zero current flow through Q7. (R20 is set to be equal to R19 and the value of R18 is small.) When current flows through Q7, it generates a voltage drop across R18 and reduces the current flow into the SDCL pin. When the current flow into the SDCL pin is 10.5 μA lower compared to the current flow into the SDCH pin, it triggers the overcurrent protection, and the Si321x ends the current PWM cycle to prevent excessive current flow through Q7. The overload current should be set 20% above the maximum inductor current to prevent current shut down prematurely.

$$R_{18} = 10.5 \ \mu A \times \frac{4.5 \ k\Omega + R_{19,20}}{1.2 \times I_{OVERLOAD}}$$

Equation 21

A fuse or other power overload circuit should be placed between the V_{DC} power supply and each input of the ProSLIC dc-dc converter circuit (one per ProSLIC solution) to protect the switching components (Q7 or M1) from potential electrical overstress in the event of a hardware fault condition. For more information concerning fuse selection, please contact Silicon Labs.

Output Overvoltage Protection

It is possible for the dc-dc converter to generate excessively high voltage beyond the voltage rating of external components. To prevent damage to these components, a transistor (Q9) is added to limit the VBAT to a desired level.

Resistors R28 and R29 are connected between VCC and VBAT as a biasing circuit for the transistor, Q9. When VBAT approaches the predetermined voltage level set by R28 and R29, Q9 is turned on and takes current from R20 away from pin SDCL and, consequentially, triggers the Si321x to end its current PWM cycle.

Q9 can be any NPN low voltage (12 V or higher) general-purpose transistor (2N2222 is recommended). The equations for R28 and R29 are as follows:

$$R28 = \frac{(VCC + VBE)}{148 \ \mu A}$$

where VBE = .55 V.

$$R29 = \frac{V_{CLAMP}}{148 \ \mu A}$$

where V_{CLAMP} is the clamping voltage for VBAT.

V_{CLAMP} should be set to a voltage less than the voltage rating of the external components and higher than the maximum VBAT to be generated for a given application.

Design Example

Suppose that the system requires 5REN of loading on 1680 ft. of line length with a ringing signal 45 V RMS at the phone. The fast voltage measurement feature is not supported, and the system prefers optimization for power saving. The system has regulated 5 V as the main supply voltage for the Si321x and an unregulated 12 V dc with a .75 A current rating.

Step 1: Define the Output Requirement

Calculate V_{TR_PK} from Equation 1:

$$V_{TR\_PK} = \frac{V_{RINGrms} \times \sqrt{2}}{7000 / NREN} \times \left(\frac{7000}{NREN} + 2 \times Dist \times 0.045 + 160 \right)$$

$$V_{TR\_PK} = \frac{45 \times \sqrt{2}}{7000 / 5} \times \left(\frac{7000}{5} + 2 \times 1680 \times 045 + 160 \right) = 76.5$$

From Equation 2:

$$V_{BAT} = V_{TR\_PK} + VCMR = 76.5 + 1.5 = 78 \ V$$

From Equation 3:

$$I_{AVG} = I_{PK} \times \frac{2}{\pi} = \frac{2 \times NREN \times V_{TR\_PK}}{7000\pi}$$

$$I_{AVG} = \frac{2 \times 5 \times 76.5}{7000\pi} = 34.79 \ mA$$

The output power equation becomes

$$P_{OUT} = V_{BAT} \times (I_{AVG} + 0.0025) = 78 \times (0.03479 + 0.0025)$$
$$= 2.9 \ W$$

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Step 2: Selecting Output Power Requirement

Set up for power optimization in the active off-hook mode:

$$I_{LIM} = 20 \text{ mA (Register 65)}$$
$$I_{BJTBIAS} = 4 \text{ mA (Register 66)}$$
$$Track = 1 \text{ (Register 71)}$$
$$V_{CM} = 3 \text{ V (Register 73)}$$
$$V_{OV} = 9 \text{ V (Register 66)}$$

From Equation 5:

$$I_{BAT} = I_{LIM} + I_{BJTBIAS} + (0.6 + 80(I_{LIM} + I_{BJTBIAS}))/5100$$
$$= 24.5 \text{ mA}$$

From track 1 Equation 6:

$$P_{OFFHOOK} = I_{BAT}(V_{CM} + V_{OV} + I_{LIM} \times R_{LINE})$$
$$= 24.5 \text{ mA}(3 + 9 + 20 \text{ mA}(2 \times 2000 \times 0.045 + 160)) = .46 \text{ W}$$

Conclusion:

The 2.9 W ringing power is the worst-case power requirement because the active off-hook power requirement is much lower (.46 W). The ringing power is used for the design of the dc-dc converter.

Step 3: Define Input Requirement for the 12 V DC

From Equation 8:

$$I_{IN} = \frac{P_{OUT}}{V_{IN} \times 60\%} = \frac{2.9}{12 \times 0.6} = 0.4 \text{ A}$$

Experiments with the unregulated 12 V source showed that the actual V_{DC} voltage drops down to 10 V at input current equal to .36 A. The adjusted V_{DC} and I_{IN} is as follows:

$$V_{DC} = 10 \text{ V}$$
$$I_{IN} = \frac{P_{OUT}}{V_{IN} \times 60\%} = \frac{2.9}{10 \times 0.6} = 0.48 \text{ A}$$

The total current drew on the 12 V unregulated supply is .48 A, which is well within the 12 V unregulated maximum specification of .75 A.

Step 4: Selecting the Power Inductor

Calculate the I_{PK} using Equation 12:

$$I_{PK} = \frac{2P_{OUT}(V_{BAT} + V_{DC})}{E_{FF} \times V_{BAT} \times V_{DC}} = 1.14 \text{ A}$$

Calculate the L1 Inductance from Equation 13:

$$L = \frac{2P_{OUT}}{E_{FF} \times I_{PK}^2 \times Fs} = 100 \ \mu H$$

$$Fs = 89.5 \text{ kHz}$$

(This frequency was selected to round up the inductor value to 100 μH.)

$$T = \frac{1}{89500} = 11.2 \ \mu S$$

From Equation 14:

$$\text{Period Register } 92 = \frac{11.2 \ \mu S}{61 \text{ nS}} = 183 = b7 \text{ H}$$

From Equation 15:

$$\text{Delay Register } 93 = \frac{t_{OFFMAX}}{61 \text{ nS}} = \frac{0.98 \times (100 \ \mu H)/75}{61 \text{ nS}}$$
$$= 21 = 15 \text{ H}$$

Step 5: Selecting the Q7 Switching Transistor

Transistor requirement:

$$V_{CEO} > V_{BAT} + V_{DC} = 78 + 10 = 88 \text{ V}$$
$$V_{EBO} > V_{CC} = 8 \text{ V}$$
$$V_{CBO} > V_{BAT} + V_{CC} + V_{DC} = 78 + 5 + 10 = 93 \text{ V}$$
$$I_{CMAX} > I_{PK} = 1.14 \text{ A}$$
$$\text{Speed: } f_T > 100 \text{ MHz}$$

The Zetex FZT955 bipolar transistor meets all of the above requirements and its HFE gain at $I_{PK} = 1.14$ A is 100.

Let $I_{R16} = 3$ mA for adequate Q7 base capacitor discharge.

From Equation 16:

$$R16 = \frac{0.6}{0.003} = 200 \ \Omega$$

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Step 6: Select the Base Drive Circuit

Q8 transistor requirement:

$$V_{CEO} = V_{CC} + V_{DC} = 5 + 10 = 15 \text{ V}$$
$$V_{EBO} = V_{CC} = 5 \text{ V}$$
$$V_{CBO} = V_{CC} + V_{DC} = 5 + 10 = 15 \text{ V}$$
$$\text{Speed}: f_T > 200 \text{ MHz}$$

The general purpose 2222 transistor meets all of the above requirements.

Calculate the value for R17:

Base current drive requirement for Q7

From Equation 17:

$$I_{BQ7} = \frac{1.3 \times I_{MAX}}{H_{FE}} = \frac{1.3 \times 0.98}{100} = 12.74 \text{ mA}$$

From Equation 18:

$$R17 = \frac{V_{CC} - 0.6}{I_{BQ7} + 0.6/R16} = 275 \ \Omega$$

Step 7: Under Voltage Circuit Design

Set under voltage lock-out to be 20% lower than the minimum V_{DC}.

$$V_{UNDER} = (1 - 20\%)VDC = 8 \text{ V}$$

From Equation 20:

$$R19 = \left(\frac{V_{UNDER} - 0.8}{120 \ \mu A}\right) - 4500 = 56K$$
$$R19 = R20 = 56K$$

Step 8: Overcurrent Protection

$$I_{OVERLOAD} = 1.2 \times I_{MAX} = 1.176 \text{ A}$$

From Equation 21:

$$R18 = \frac{10.5 \ \mu A \times (4500 + R19)}{I_{OVERLOAD}} = 0.5 \ \Omega$$

Step 9: Output Overvoltage Protection

VBAT max = 78 V (during ringing). See Table 2 for voltage ratings.

Table 2. Component Voltage Rating

Components	Voltage Parameter	Voltage Rating
C9, C26, C3, C4, C5, C6	$V_C - 1.5$	98.5
Q1–Q4 (2N5401)	V_{CEO}	150
Q5, Q6	V_{CEO}	150
Q7	$V_{CEO} - VDC$	$100 - 12 = 88$

Therefore, V_{CLAMP} must be greater than 78 V but less than 88 V: V_{CLAMP} = 85 V.

If VCC = 5 V, then

$$R28 = \frac{(5 + .55) \text{ V}}{148 \ \mu A} = 37.4k$$

$$R29 = \frac{85 \text{ V}}{148 \ \mu A} = 574k$$

MOSFET/Transformer Design DC-DC Converter

The MOSFET/transformer dc-dc converter solution offers higher power efficiency than the BJT/inductor solutions and is the preferred solution for applications using low V_{DC} input voltages.

The transformer dc-dc converter circuit is shown in Figure 6. R16, R17, Q7, and Q8 are eliminated. The M1 MOSFET is the main power-switching component in this design. The Si321xM version of the ProSLIC is used to directly drive the M1 MOSFET using the DCFF pinout.

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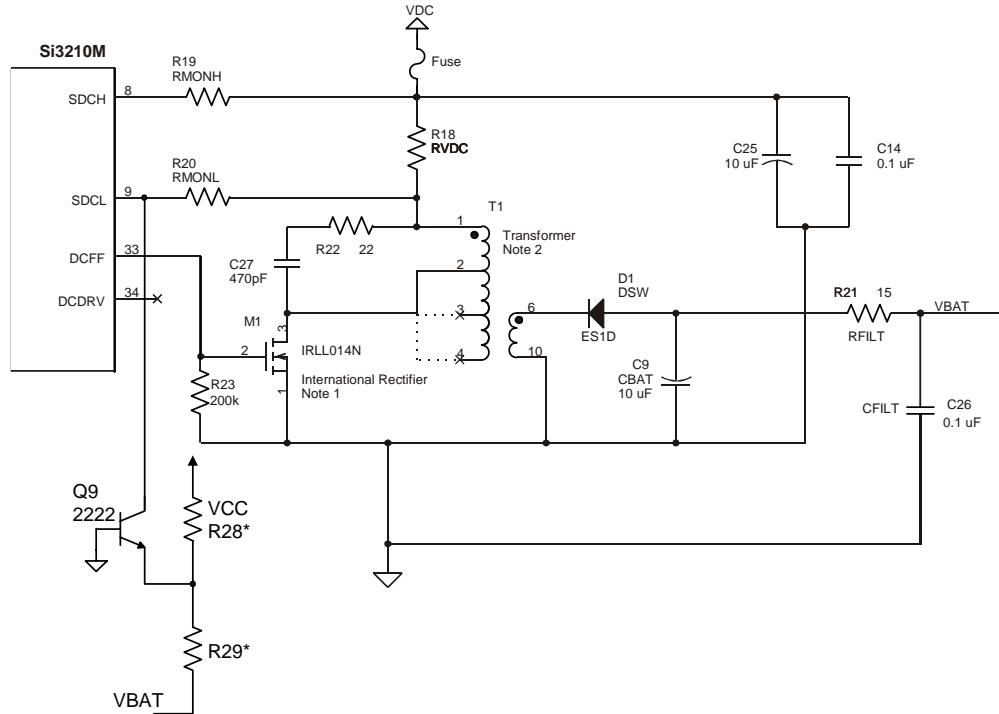
Figure 6. Transformer DC-DC Converter

All relevant design equations for the inductor dc-dc converter are applied in the same manner for the transformer dc-dc converter except for the following equations.

Equation 10A

During the off interval, the switch current goes to 0 and the primary voltage is the reflection of the V_{BAT}: $V_P = N \cdot V_{BAT}$. The transformer mutual primary current equation becomes

$$i(t) = I_{PK} - \frac{N \times V_{BAT}}{L_M}(t)$$

In the discontinuous mode, the current goes to 0 at the end of the off time interval:

$$0 = I_{PK} - \frac{N \times V_{BAT}}{L_M}t_{OFF-MAX}$$

Solving for $t_{OFF-MAX}$:

$$t_{OFF-MAX} = \frac{I_{PK} \times L}{N \times V_{BAT}}$$

Equation 10A

Where N is the transformer turn ratio:

N_P is the number of turn of the primary winding.

$$N = \frac{N_P}{N_S}$$

N_S is the number of turn of the secondary winding.

Equation 12A:

Deriving the peak current equation based on the new $t_{OFF-MAX}$ 10A equation:

$$I_{PK} = \frac{2P_{OUT} \times (N \times V_{BAT} \times V_{DC})}{E_{FF} \times N \times V_{BAT} \times V_{DC}}$$

Equation 12A

Equation 13A

Use the former Equation 13 and solve for F_S.

$$F_S = \frac{2P_{OUT}}{E_{FF} \times L \times I_{PK}^2}$$

Equation 13A

Switching MOSFET Requirements

Due to the low voltage and low current drive capacity of the DCFF pin, logic level MOSFET must be used. Table 3 lists the requirement for the switch MOSFET.

Table 3. Switch MOSFET M1

| |
|---|
| $V_{DSS} > N \times V_{BAT} + V_{DC}$ |
| $I_{D\,MAX} > 3 \times I_{PK}$ at $V_{GS} = 3$ V |
| R_{DS} 0n < .2 Ω at $I_{D\,MAX}$ |
| V_{GS} (th) < 2 V |
| C_{ISS} (input cap) < 300 pF |
| C_{OSS} (output cap) < 60 pF |
| C_{RSS} (reverse t. cap) < 30 pF |
| Total gate charge: 14 nC |
| t_{ON} ($V_{DD} = 50$ V, $I_D = 4$ A) < 10 ns |
| t_{OFF} ($V_{DD} = 50$ V, $I_D = 4$ A) < 20 ns |

Power Transformer

A transformer was designed for the Si321x dc-dc converter based on the TDK PC40EF12.6 E core. This transformer has three primary windings connected in series (see Figure 7) to handle all V_{DC} voltage ranging from 3 V to 35 V (consult the factory for higher V_{DC}). The secondary winding can generates up to 94.5 V V_{BAT} at any in range V_{DC} input. Table 4 shows the voltage and the transformer ratio N value for each of the winding connection.

Table 4. Transformer Winding Connection

V_{DC} Voltage	Winding Connection	Ratio N	Primary Inductance
3 V to 9 V	Winding 1–2	.2	11.3 μH
10 V to 15 V	Winding 1–3	.4	45.2 μH
16 V to 35 V	Winding 1–4	.6	107 μH
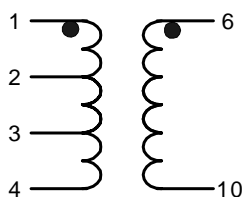
Figure 7. Winding Connections
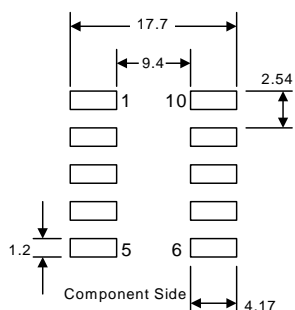
Figure 8. Recommended PCB Layout

Core Material: E core, TDK PC40EF12.6-Z, or equivalent

Air Gap: Center leg .088 mm

Bobbin: 10 pin (ready for pick and place)

Winding:

W1–2 = W2–3 = W3–4 =20T, #28 wire

W6–10 = 40T, #33 wire

Inductance:

W1–2 = 11.3 μH ±10% (only one winding needs to be tested)

W1–3 = 45.2 μH ±10%

W1–4 = 107 μH ±10%

MOSFET/Transformer DC-DC Converter Design Procedure

The transformer dc-dc converter design procedure is similar to the design of the inductor dc-dc converter. Below are design steps based on the BJT/inductor design example.

1. Step 1 to step 2 are identical to the BJT/inductor dc-dc converter

2. In step 3, use 75% efficiency for input power calculation.

3. In step 4, the peak current is calculated using Equation 12A; the maximum delay time for Register 93 is calculated using Equation 10A; the switching frequency F_S and the period for the Register 92 is calculated using Equation 13A. The inductance of inductor L in equations 10A and 13A is selected from Table 4 based on the V_{DC} voltage level.

4. Step 5 now handles the selection of the M1 MOSFET based on the requirements on Table 3.

5. Step 6 is no longer needed since the drive transistor Q8 is eliminated.

6. Steps 7 and 8 are the same.

7. In step 9, use the voltage rating for M1 instead of Q1. The voltage parameter for M1 is as follows:

$$V = \frac{V_{DSS}}{N} - VDC$$

8. Other components in the circuit that are not discussed above should use the component values recommended in Figure 6.

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Document Change List

Revision 0.4 to Revision 0.5

- Equation 6
  - Changed RLINE to RLOOPMAX.
- "In the Off-Hook State"
  - Updated text.
- "Step 1: Define the Output Requirement"
  - Added +160 to first equation.
- "Step 2: Selecting Output Power Requirement"
  - Added +160 to last equation.
  - Changed =.3822 to .46 W.
  - Changed .312 to .46 in last paragraph.
- Added SLIC series resistance.
- VCMR adjustment.
- Changed Si3210 to Si321x throughout.

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