SONY

CXB1828ER

2.5Gbps Laser Diode Driver

Description

The CXB1828ER is a high-speed monolithic laser diode driver. This IC can drive the data rate of 2.5Gbps and the modulation current of up to 50mA. The bias current of up to 50mA can be supplied and it is controlled by the built-in APC (automatic power control). The modulation current and bias current are designed to be linearly controlled by the voltage input to the control pin.

This IC has a built-in DFF, and through mode or DFF mode can be selected. In through mode the signal goes as it is, and in DFF mode the input signal is retimed by the external clock. The data input pin and the clock input pin can accept the differential input of PECL and CML, and the 50Ω termination resistors are provided in the IC.

The shutdown function which shuts down the modulation current and bias current, the activity error detect circuit which detects that the signal has no input, and the alarm output power-on reset circuit. Furthermore, the duty cycle control circuit which corrects the modulation output signal duty is included in this IC.

The CXB1828ER employs the 4.8mm × 4.8mm of 32-pin plastic package, contributing to the miniaturization of the optical mode.

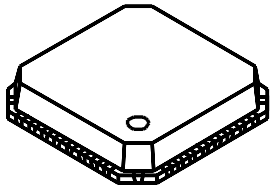
Features

- Direct laser diode drive
- Maximum data rate of 2.5Gbps
- Power-on reset function
- Automatic power control (APC) for bias current
- Alarm function and shutdown function
- Differential PECL and CML inputs or AC coupled input
- Internal duty cycle correction circuit
- Activity error detector function for laser safety
- Typical rise time is 80ps.
- Built-in 50Ω input termination resistor
- Compact package size: 4.8mm × 4.8mm
- Single +3.3V supply voltage

Applications

- Gigabit ethernet: 1.25Gbps
- SONET/SDH: 622Mbps, 2.5Gbps

32 pin VQFN (Plastic)



Absolute Maximum Ratings

• Supply voltage	$V_{CC} - V_{EE}$	–0.3 to +6.0	V
• Data and clock input voltage difference	$\lvert V_D - V_{DN} \rvert$	2.5	V
• Bias output current		100	mA
• Modulation output current		100	mA
• Storage temperature	Tstg	–65 to +150	°C

Recommended Operating Conditions

• Supply voltage	$V_{CC} - V_{EE}$	3.14 to 3.46	V
• Operating ambient temperature	Ta	–40 to +85	°C

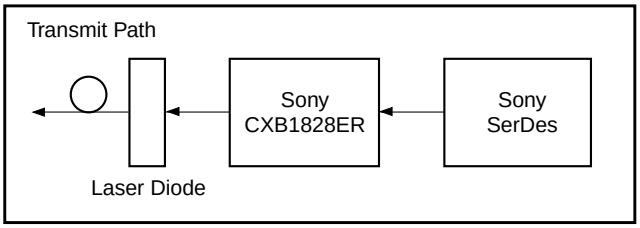
Important Notes

The IC requires SLOW turning power on and off. See Vcc rise and fall time in AC characteristics.

Electrostatic Strength

This IC has a very sensitive electrostatic strength, so care should be taken for handling.

Typical Transmit Block Diagram



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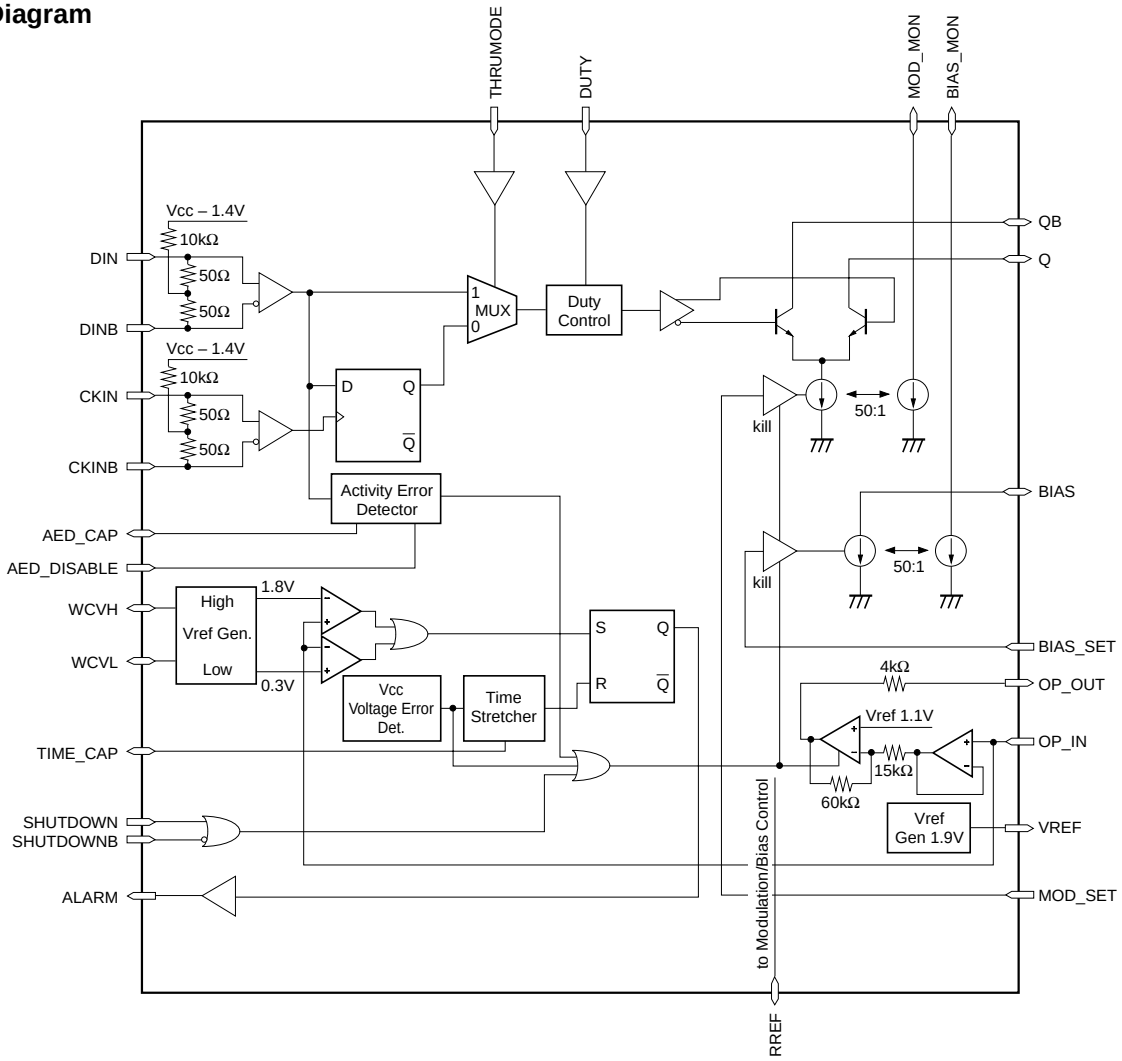
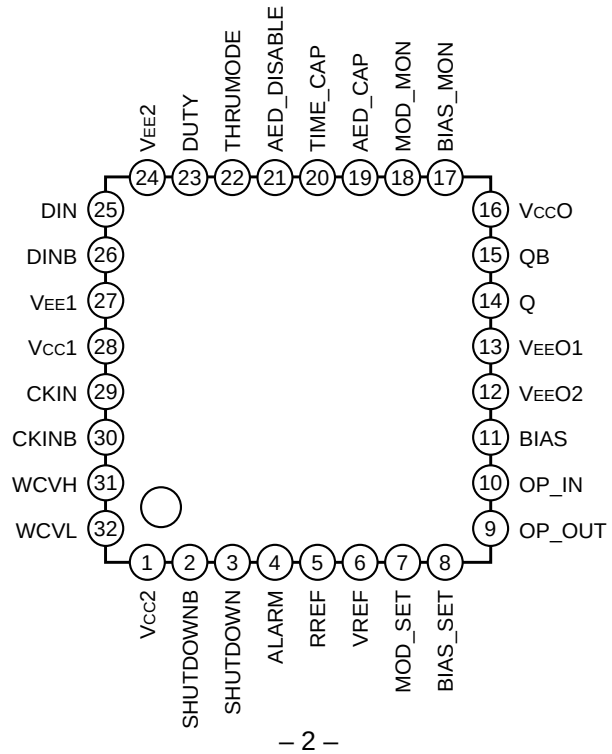
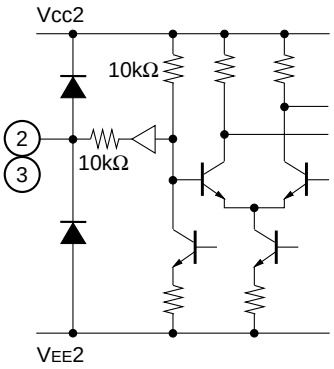
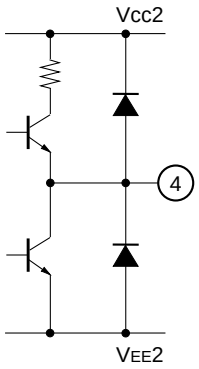
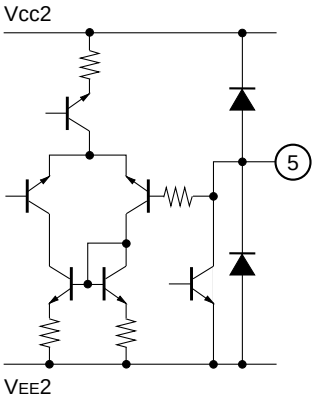
Block Diagram

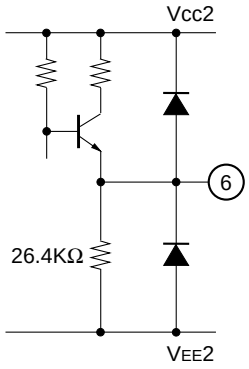
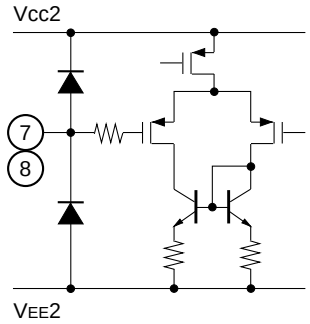
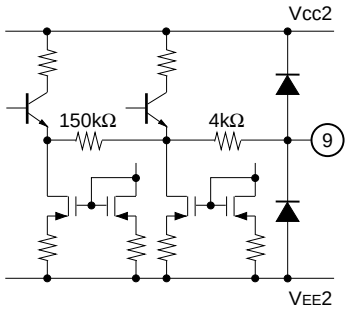
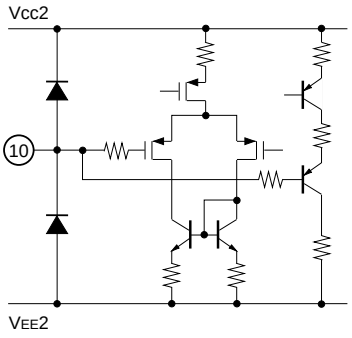


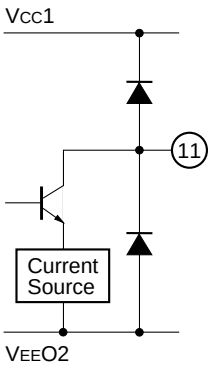
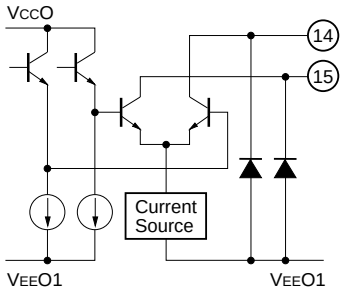
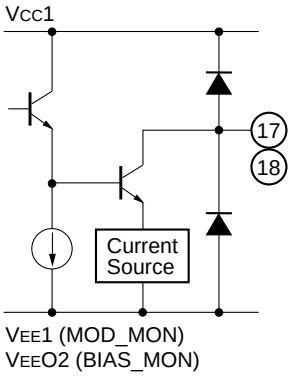
Pin Assignment

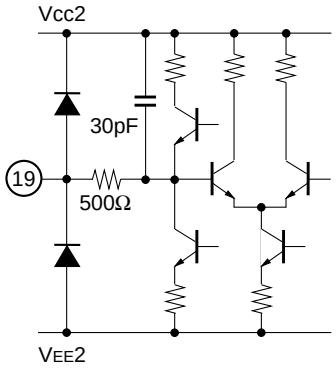
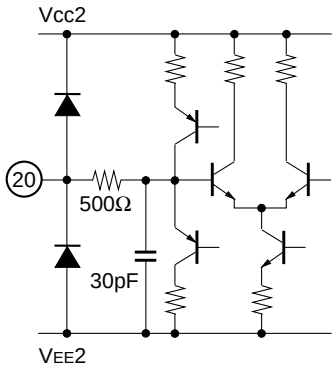
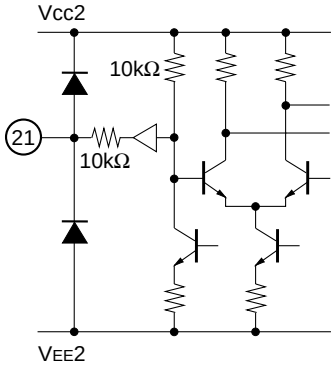
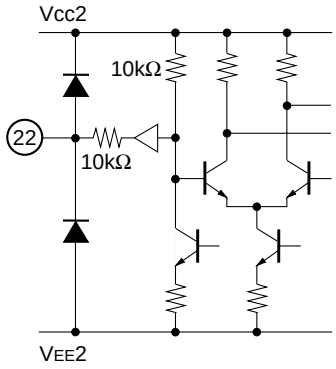


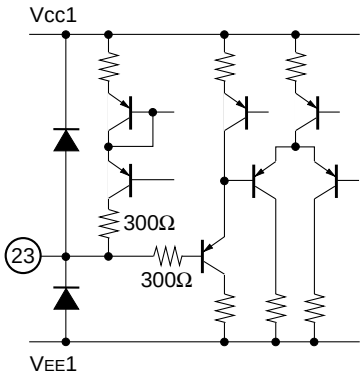
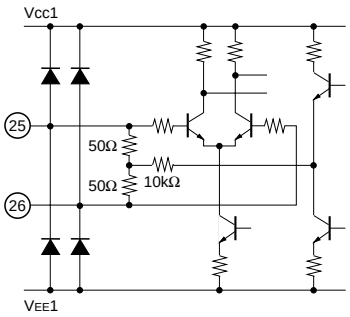
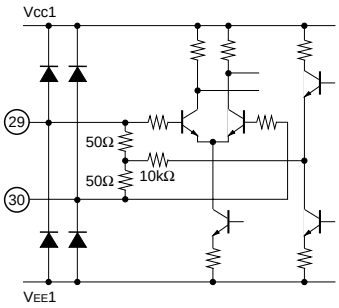
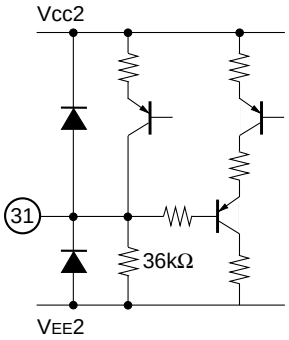
Pin Description

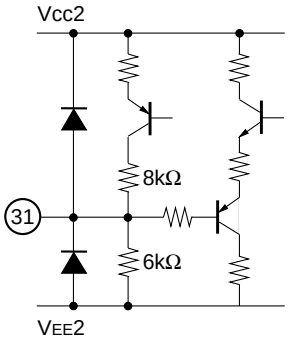
Pin No.	Symbol	Typical pin voltage (V) DC	I/O	Equivalent circuit	Description
1	Vcc2	3.3			Positive power supply.
2	SHUTDOWNB	0 or Vcc	I		TTL input. The modulation current and bias current is shut down by inputting the Low voltage to this pin. High level when open.
3	SHUTDOWN	0 or Vcc	I		TTL input. The modulation current and bias current is shut down by inputting the High voltage to this pin. High level when left open.
4	ALARM		O		TTL output. High when the abnomality is detected from the OP_IN pin voltage. The abnormal voltage of OP_IN is Vop < 0.3V or Vop > 1.8V.
5	RREF				Connect an external resistor of 18kΩ between this pin and Vcc.

Pin No.	Symbol	Typical pin voltage (V) DC	I/O	Equivalent circuit	Description
6	VREF	1.9	O		Reference voltage output. GND reference 1.9V.
7	MOD_SET	0.2 to 2.0	I		Modulation current control. The modulation current is controlled by this pin voltage.
8	BIAS_SET	0.2 to 2.0	I		Bias current control. The bias current is controlled by the voltage of this pin.
9	OP_OUT		O		Internal operational amplifier output. Used for the bias current automatic power control (APC). The OP_OUT pin is connected to the BIAS_SET pin. Connect a 0.1µF capacitor between this pin and GND.
10	OP_IN	0.3 to 1.8	I		The internal operational amplifier input for the bias current automatic power control (APC).

Pin No.	Symbol	Typical pin voltage (V) DC	I/O	Equivalent circuit	Description
11	BIAS		O		Laser bias current output.
12	VEEO2	0			Negative power supply for the modulation and bias output.
13	VEEO1	0			Negative power supply for the modulation output.
14	Q		O		Laser modulation current output. Open collector output.
15	QB		O		Complementary current output. Connect the laser diode not to this pin, but to the Q pin.
16	VccO	3.3			Positive power supply for the modulation output.
17	BIAS_MON		O		Bias current monitor. 1/50 of the bias current flows to this pin. This pin is connected to Vcc either through a resistor 1kΩ or directly.
18	MOD_MON		O		Modulation current monitor. 1/50 of the modulation current flows to this pin. This pin is connected to Vcc either through a resistor 1kΩ or directly.

Pin No.	Symbol	Typical pin voltage (V) DC	I/O	Equivalent circuit	Description
19	AED_CAP				Capacitor connection for the activity error detector. If the active detector function is not required, this pin can be left open. When a capacitor is connected between the AED_CAP pin and Vcc, the time till the error is detected can be extended.
20	TIME_CAP				Capacitor connection for the alarm power-on reset. The period of the power-on reset time is controlled by a capacitor (recommended value is 0.01µF) connected between the TIME_CAP pin and GND. If the ALARM function is not required, this pin can be left open.
21	AED_DISABLE		I		TTL input. This pin controls the activity error detector circuit. When High (open or connected to Vcc), the activity error detector function is disabled. When Low (connected to GND), the activity error detector function is enabled.
22	THRUMODE		I		TTL input. When High (open or connected to Vcc), the input data goes not through the D flip-flop. When Low (connected to GND), the serial input data goes through the D flip-flop within the chip.

Pin No.	Symbol	Typical pin voltage (V) DC	I/O	Equivalent circuit	Description
23	DUTY				Resistor connection for the duty cycle control. When an external resistor is connected between the DUTY pin and GND, the modulation pulse width can be expanded.
24	VEE2	0			Negative power supply.
25	DIN	PECL or CML	I		Differential PECL and CML data inputs. These two inputs are internally connected by 100Ω and biased by 10kΩ to Vcc – 1.4V.
26	DINB				
27	VEE1	0			Negative power supply.
28	Vcc1	3.3			Positive power supply.
29	CKIN	PECL or CML	I		Differential PECL and CML clock inputs. These two inputs are internally connected by 10kΩ and biased by 10kΩ to Vcc – 1.4V.
30	CKINB				
31	WCVH	1.8			Window comparator's higher threshold voltage for ALARM. The default high alarm assert voltage for the comparator is 1.8V.

Pin No.	Symbol	Typical pin voltage (V) DC	I/O	Equivalent circuit	Description
32	WCVL	0.3			Window comparator's lower threshold voltage for ALARM. The default low alarm assert voltage for the comparator is 0.3V.

Electrical Characteristics

DC Characteristics

($V_{CC} – V_{EE}$ = 3.14 to 3.46V, Ta = –40 to +85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
DC power supply voltage	V_{DC}	$V_{CC} – V_{EE}$	3.14	3.3	3.46	V
Supply current (DATA THRU MODE)	ICC_THRU	I_Q = 0mA, I_B = 0mA		62	84	mA
Supply current (D-FF MODE)	ICC_DFF	I_Q = 0mA, I_B = 0mA		65	88	mA
Maximum modulation output current	I_{QMAX}		50			mA
Minimum modulation output current	I_{QMIN}				7	mA
Modulation output voltage range	V_Q		Vcc – 2		Vcc	V
Maximum bias output current	I_{BMAX}		50			mA
Minimum bias output current	I_{BMIN}				3	mA
Bias output voltage range	V_B		Vcc – 2		Vcc	V
Modulation shutdown current	I_{QSHD}				100	µA
Bias shutdown current	I_{BSHD}				100	µA
DIN, CKIN input High voltage (PECL)	V_{EIH}	*1	Vcc – 1.17		Vcc – 0.81	V
DIN, CKIN input Low voltage (PECL)	V_{EIL}	*1	Vcc – 1.84		Vcc – 1.48	V
DIN, CKIN differential input voltage (CML)	V_{IN}	*2	400		2000	mVp-p
Internal resistance between DIN and DINB, CKIN and CKINB	R_{DI}, R_{CK}		70		130	Ω
Internal input reference voltage at DIN, DINB, CKIN, CKINB	V_{EIR}			Vcc – 1.37		V
TTL input High voltage	V_{TIH}		2.0		Vcc + 0.3	V
TTL input Low voltage	V_{TIL}		–0.3		0.8	V
TTL input current High	I_{TIH}				5	µA
TTL input current Low	I_{TIL}		–250			µA
ALARM output High voltage	V_{TOH}	Iin = –0.4mA	2.4		Vcc	V
ALARM output Low voltage	V_{TOL}	Iin = 2.0mA	0		0.5	V
VREF output voltage	V_{REF}	Iout = 0 to 500µA	1.80		2.05	V
WCVH output voltage	V_{WH}	Open voltage	1.70		2.05	V
WCVL output voltage	V_{WL}	Open voltage	0.28		0.37	V
Vcc voltage error detect voltage	Vcc_err		2.59		3.08	V

*1 Since the internal input reference voltage may become lower than the Low level of ECL, input the signal into DIN and CKIN by AC coupling at the time of a single phase input.

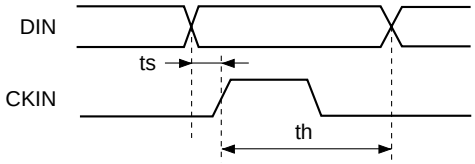
*2

VIN

AC Characteristics (Vcc – VEE = 3.14 to 3.46V, Ta = –40 to +85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Maximum data rate	fdmax		2.488			Gbps
Maximum variable High pulse width by duty cycle control	tdelay	Data rate = 2.5Gbps	100			ps
Rise time (20 to 80%)	tr	IQ = 50mA, RL = 25Ω		80		ps
Fall time (80 to 20%)	tf	IQ = 50mA, RL = 25Ω		90		ps
DIN – CKIN setup time	ts	Rise and fall time of input = 130ps*3	30			ps
DIN – CKIN hold time	th	Rise and fall time of input = 130ps*3	50			ps
Vcc rise time	tvccr	10 to 90%	5			ms
Vcc fall time	tvccf	90 to 10%	5			ms

*3



Setup time, Hold time

DC/AC Characteristics for the APC Circuit (Vcc – VEE = 3.14 to 3.46V, Ta = –40 to +85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
OP_IN input voltage range	VI_OP			Fig. 15		V
OP_OUT output maximum voltage	VO_OPMAX				2.0	V
OP_OUT output minimum voltage	VO_OPMIN		0.2			V
Minimum OP_OUT output voltage at shutdown condition	VO_OPSDN				0.2	V
OP_IN input current	II_OP		–2.0		1	µA
OP_OUT output source current	IO_OPSORC				4	µA
OP_OUT output sink current	IO_OPSINK				4	µA
APC operational amplifier gain	AV			12		dB
Monitor photodiode current range	IMPD		10		1000	µA

Functional Block Description

APC (Automatic power control)

The APC loop consists of the laser driver and APC operational amplifier. The APC operational amplifier is configured as an inverting integrator. It is the input voltage that is derived from the monitor current by the monitor photodiode and an external resistor R_{PD} to OP_IN.

The input voltage is inverted and the output from OP_OUT. The bias current is controlled by inputting the output to the BIAS_SET pin. The bias current is set by R_{PD}. A capacitor C_{PD} with a value of 1000pF works for stability and reduces the noise. Use C_{APC} (recommended value 0.1µF) between the OP_OUT pin and V_{EE}. C_{APC} controls the rapid rise of the OP_OUT pin when the shutdown is cancelled, and suppresses the excess current flowing to the laser diode.

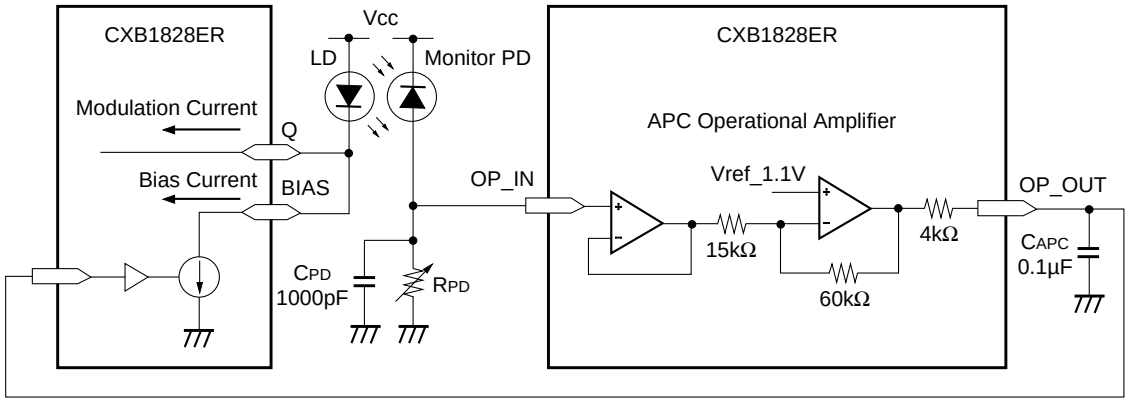


Fig.1. APC Function Block Diagram

Alarm function

This circuit is for the APC operation. When the input OP_IN is provided with an excess voltage or minimal voltage, the window comparator output goes High, and this signal is latched resulting in the output of alarm signal. The WCVH and WCVL pin voltages are the upper and the lower threshold values of the window comparator for ALARM. The default value of WCVH is 1.8V and that of WCVL is 0.3V. If the voltage of OP_IN is lower than WCVL or higher than WCVH, ALARM signal is asserted High. This alarm signal returns to Low only by the Vcc power-on reset function. Power-on reset time (T_{TIME}) is set by the external capacitor put between the TIME_CAP pin and V_{EE}. (Refer to Fig. 8.) It is necessary for the alarm signal output to be Low forcibly because the excess voltage or minimal voltage may be applied to the OP_IN pin till the APC operation completes. The recommended value of the capacitor is 0.01µF.

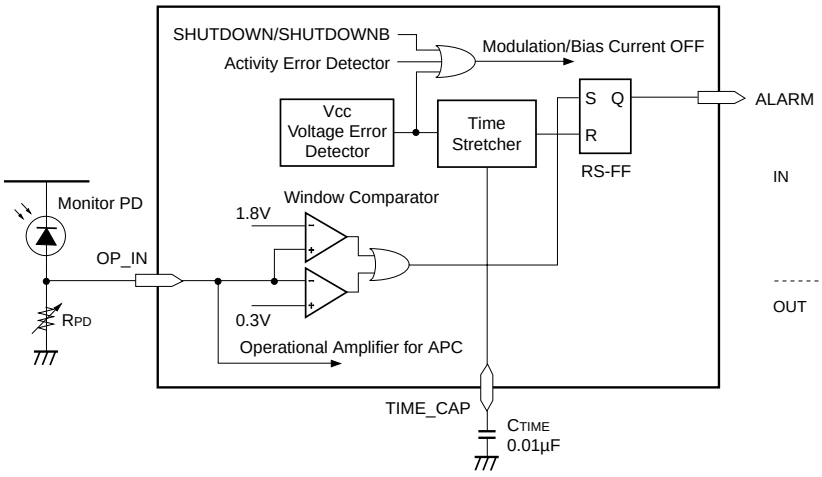


Fig.2. Alarm Function Block Diagram

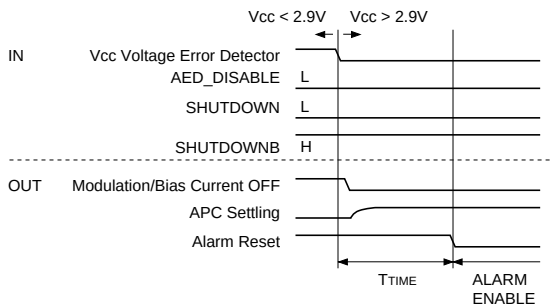


Fig.3. Timing Chart of Alarm Function

Data input

The PECL/CML signal is input to the data buffer at a maximum data rate of 2.5Gbps. This input pin is biased by the reference bias voltage (Vcc – 1.4V) for the AC coupling input. An on-chip 100Ω resistor is put between the DIN and DINB pins. The data buffer has the frequency detector and input amplitude voltage detector for the Activity Error Detector (AED).

Clock input

The PECL/CML clock is input to the clock buffer at a maximum data rate of 2.5GHz. This input pin is biased by the reference bias voltage (Vcc – 1.4V) for the AC coupling input. An on-chip 100Ω resistor is put between the CKIN and CKINB pins.

Signal duty cycle correction

The output pulse width can be extended as shown in Fig.9 by connecting an external resistor between the DUTY pin and V_{EE}, and setting its resistor value from 0Ω to 4kΩ. The output pulse width can be extended up to 100ps (min.). Short the DUTY pin to V_{EE} when not want to vary the duty.

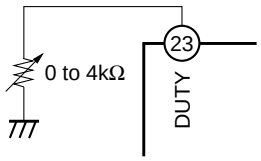


Fig.4. Duty Cycle Control

Bias current and modulation current control

The bias current and modulation current can be controlled linearly by the voltage input to the BIAS_SET and MOD_SET pins as shown in Figs.10 and 11. The voltage applied to the BIAS_SET and MOD_SET pins can be set by the external resistor between the VREF pin and V_{EE}. Refer to Fig.5.

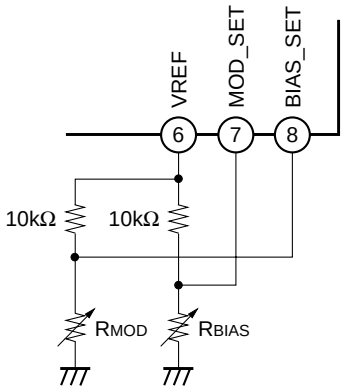


Fig.5. Modulation/Bias Control

Bias current and modulation current monitor

This circuit monitors the bias and modulation current. The BIAS_MON and the MOD_MON pins should be connected to V_{CC} either directly or through a resistor. The modulation current and monitor current are in the rate of approximately 50:1. (Refer to Fig.12 and Fig.13.)

Thru-mode

When this pin is High or connected to Vcc, the input data goes not through the internal flip-flop. If this pin is grounded the input data goes through the D flip-flop.

Shutdown function

This circuit disables the output current, that is, the bias and modulation current is turned off and used to shut off the laser. And the voltage of OP_OUT is set to V_{EE}. The function block diagram for all of the shutdown mechanism for the circuit is shown in Fig.6. The shutdown functions when one of the following conditions is met.

1) SHUTDOWN is High.
2) SHUTDOWNB is Low.
3) The activity error detector detects an error of the DIN/DINB input signal.
4) The voltage error detector detects Vcc is below 2.59 to 3.08V.*

(* The bias current may flow at approximately Vcc = 2.0V.)

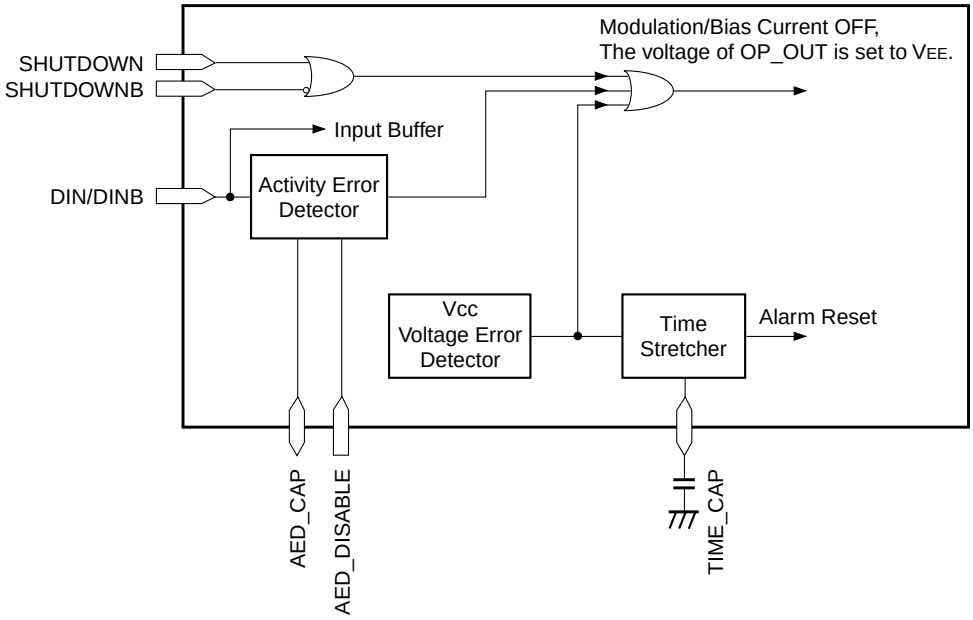


Fig.6. Shutdown Function Block Diagram

Activity error detect function

The activity error detect circuit monitors the DIN/DINB input signal, and shuts down the output current when this circuit determines that the input data signal has no input. The conditions where the input signal is determined to be no signal are when the input data signal logic is not varied over a period of the time set by the user and when the voltage swing is too small (< 100mVpp-diff). Either of these conditions is met, the shutdown circuit is enabled and the modulation current and laser bias current are shut down.

If needed, the time till the activity error detect can be extended. Fig.14 shows the graphs of the activity error detection time (T_{AED}) vs. C_{AED}. When the activity error detect function is not required, connect the AED_DISABE pin to V_{CC} or leave it the pin open.

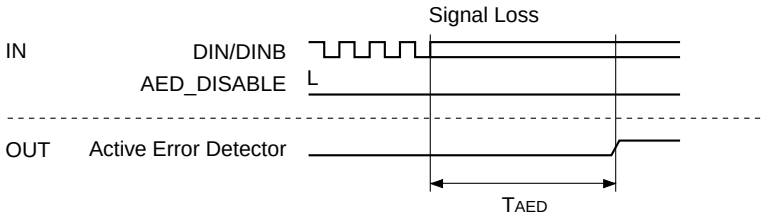
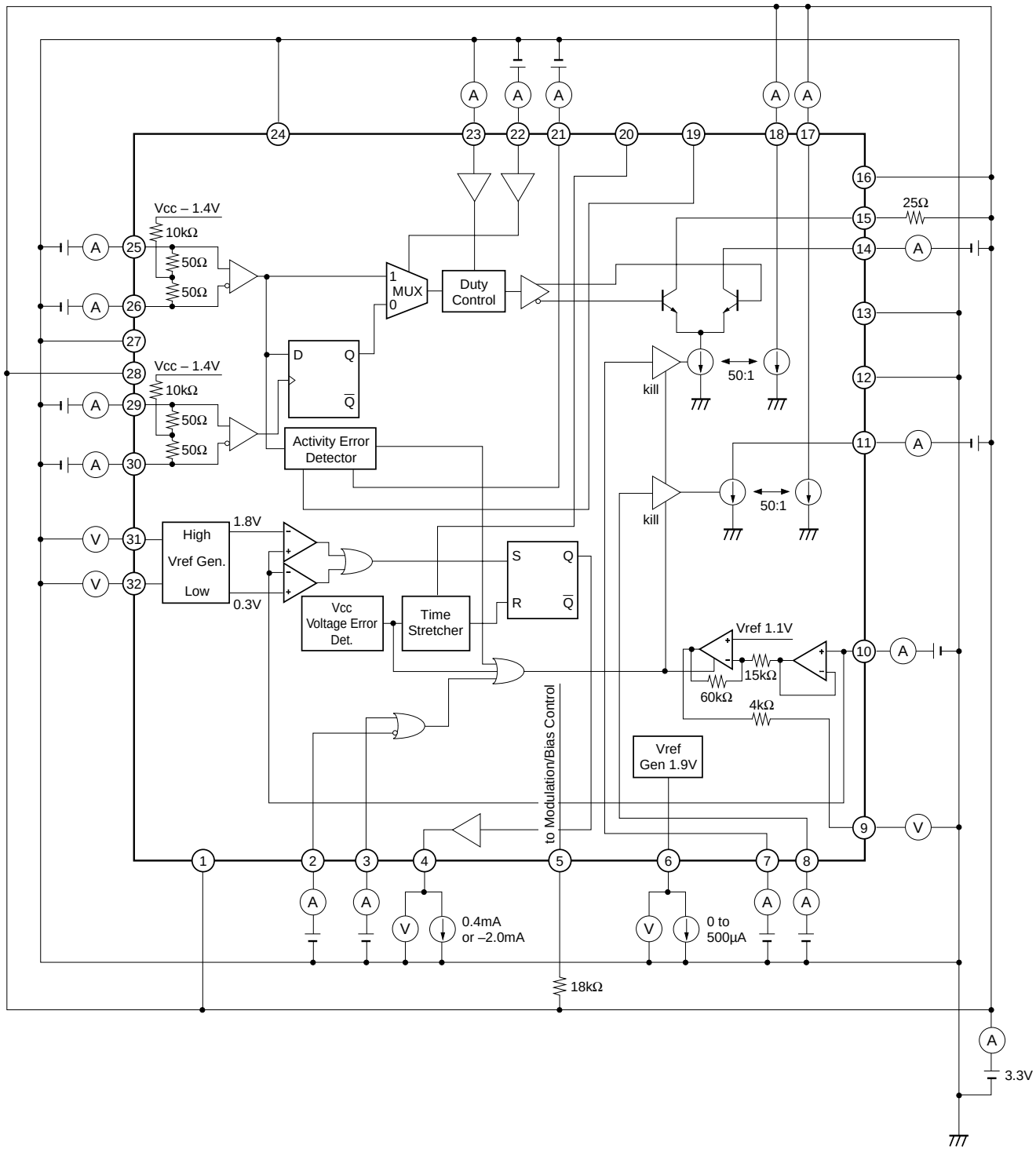
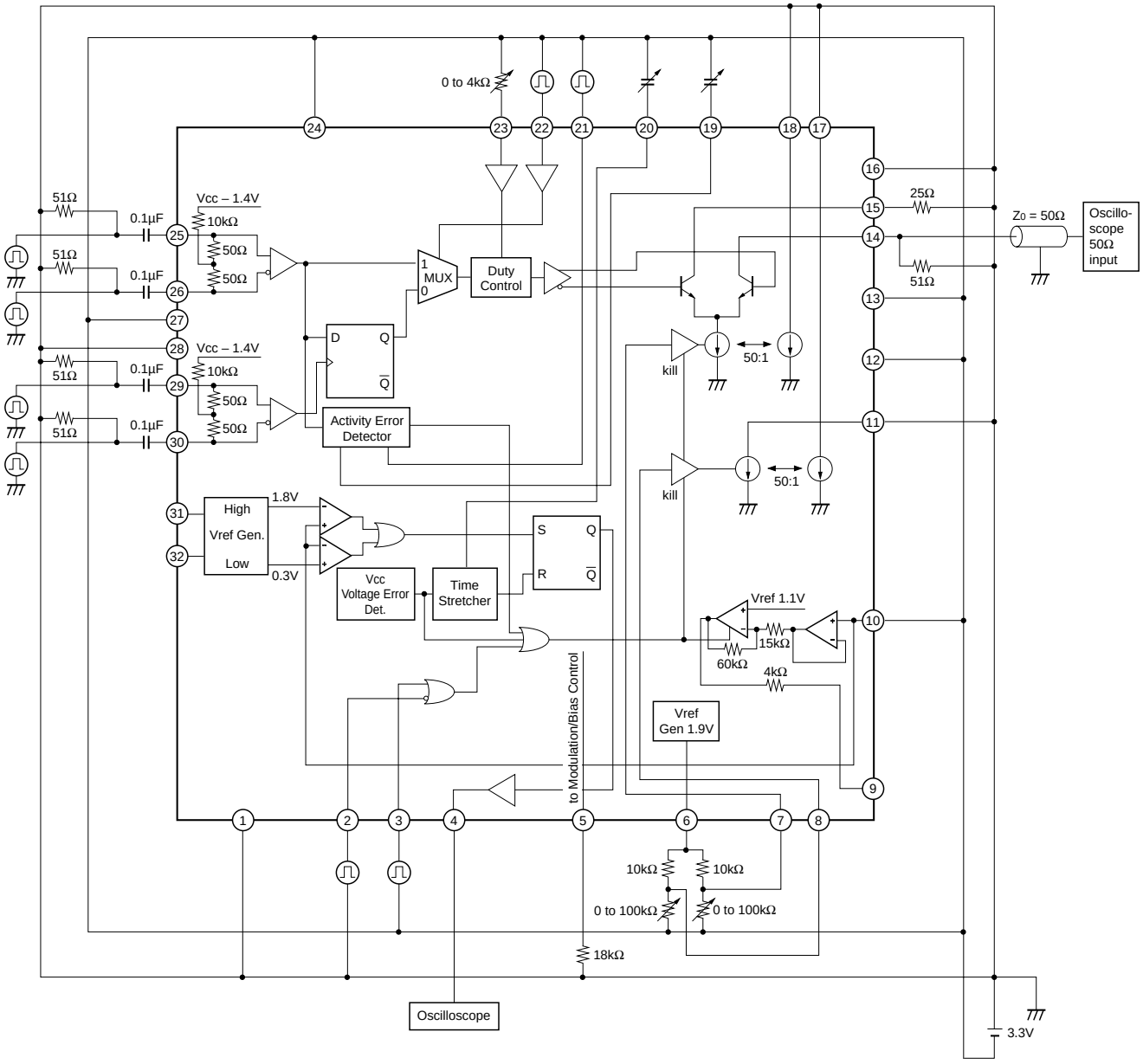


Fig.7. Timing Chart of AED Function

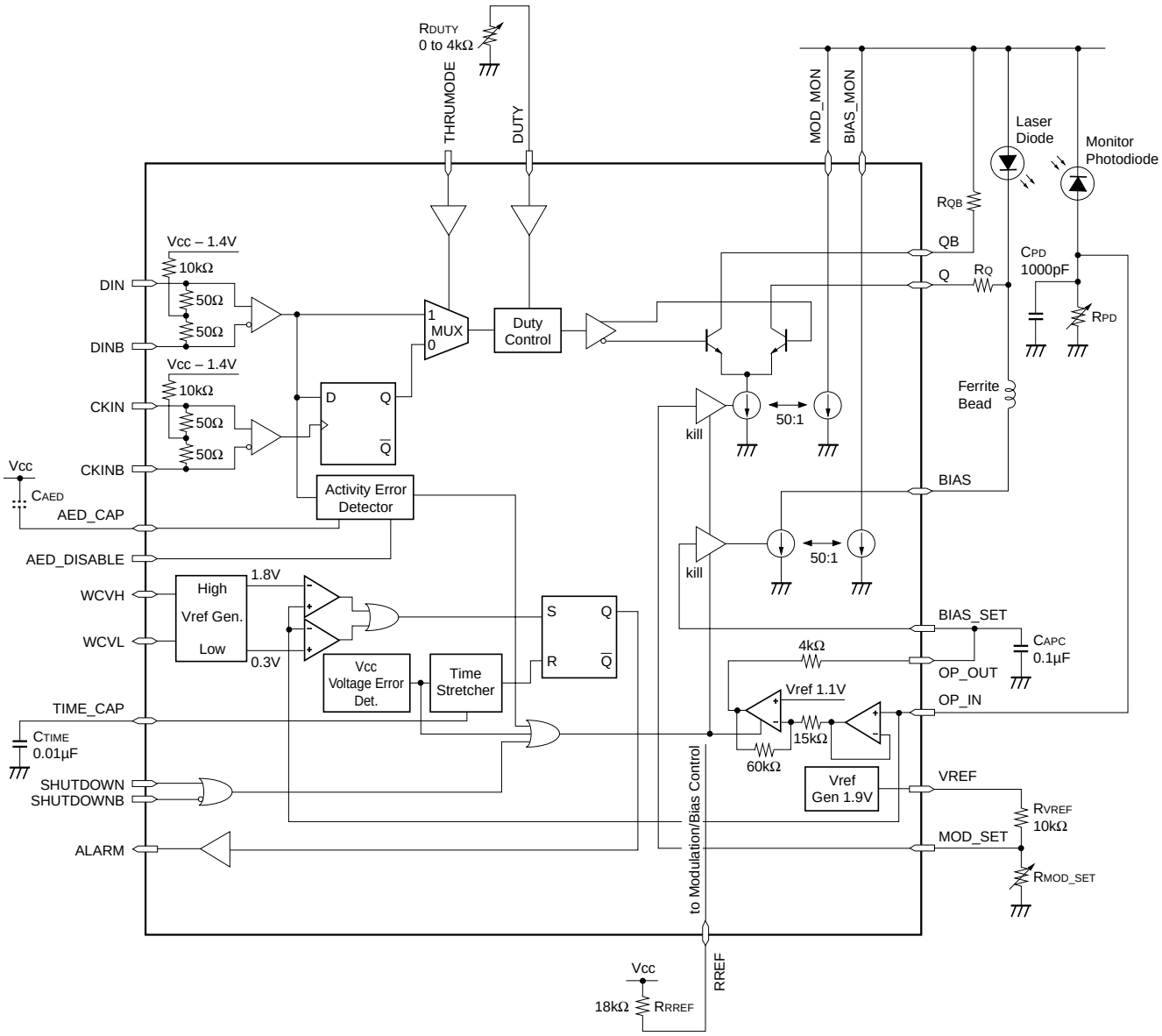
DC Electrical Characteristics Measurement Circuit



AC Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

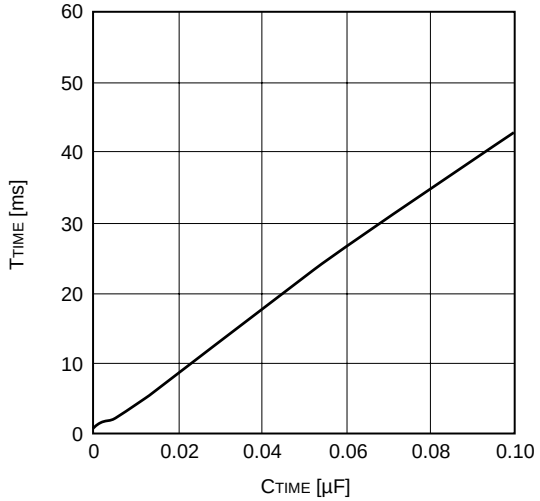


Fig. 8. Power-on reset time (T_{TIME}) vs. C_{TIME}

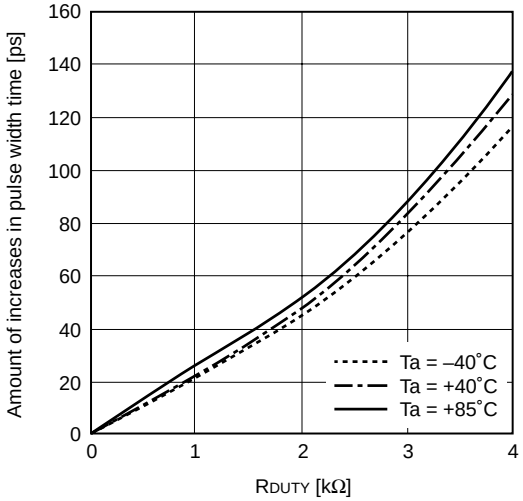


Fig. 9. Increment of output pulse width vs. R_{DUTY}

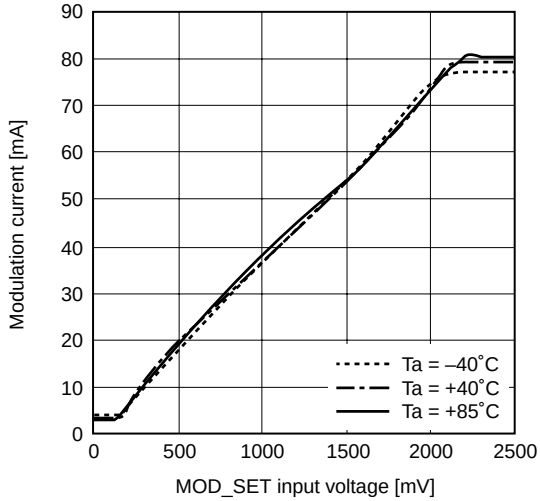


Fig. 10. Modulation current vs. MOD_SET input voltage

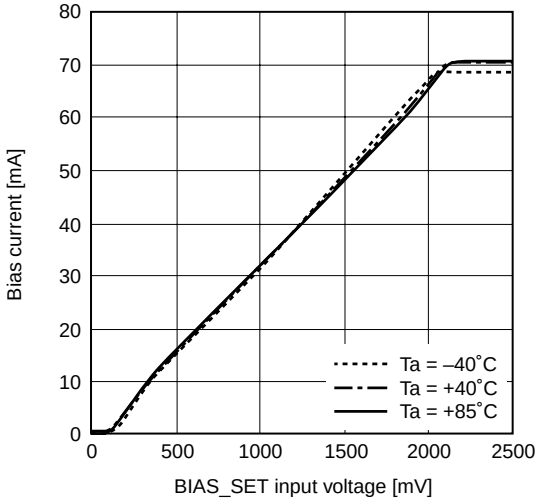


Fig. 11. Bias current vs. BIAS_SET input voltage

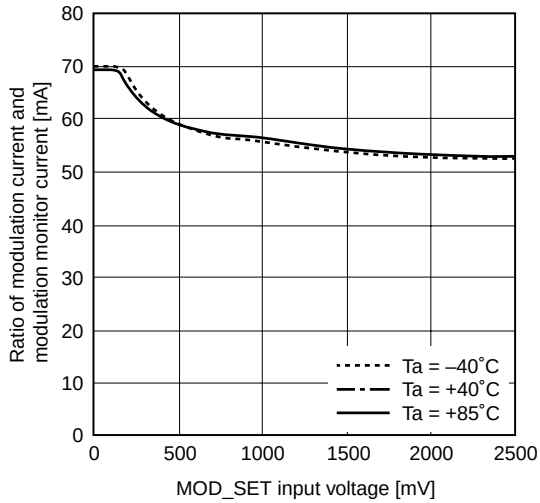


Fig. 12. Ratio of modulation current (I_Q) and modulation monitor current vs. MOD_SET input voltage

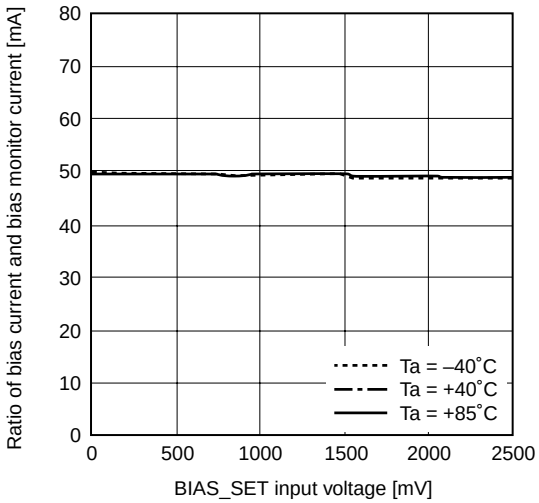


Fig. 13. Ratio of bias current (I_B) and bias monitor current vs. BIAS_SET input voltage

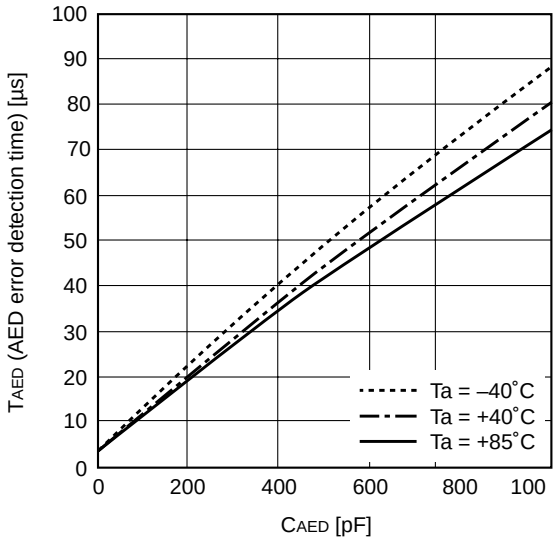


Fig. 14. Activity error detect time (T_{AED}) vs. C_{AED}

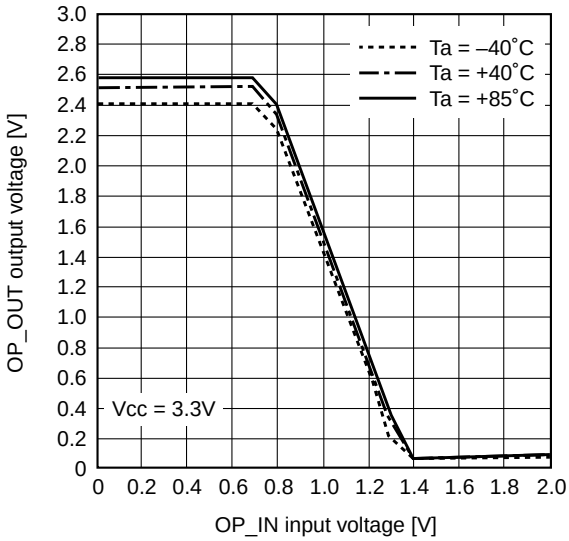
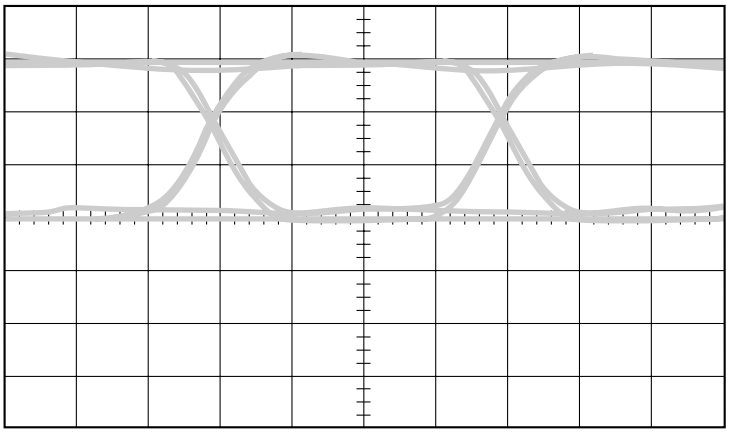


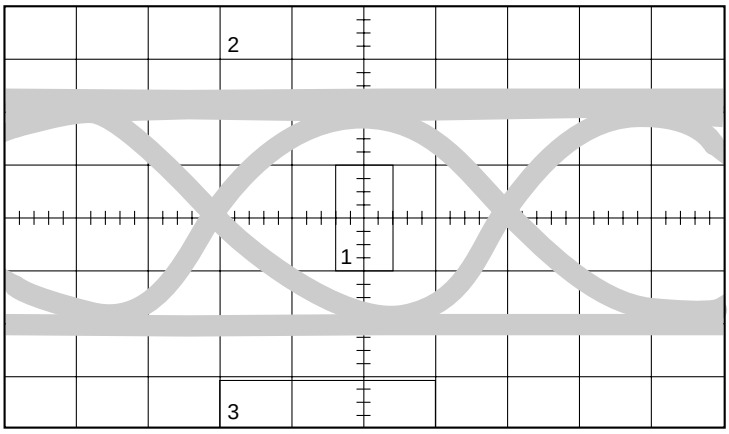
Fig. 15. OP_OUT output voltage vs. OP_IN input voltage



RL = 25Ω
Ta = 25˚C
I_Q = 30mA
Pattern = $PRBS^{23} – 1$
Data Rate = 2.5Gbps

Time base: 100.0ps/div 250mV/div

Fig. 16. Electrical Output Waveform

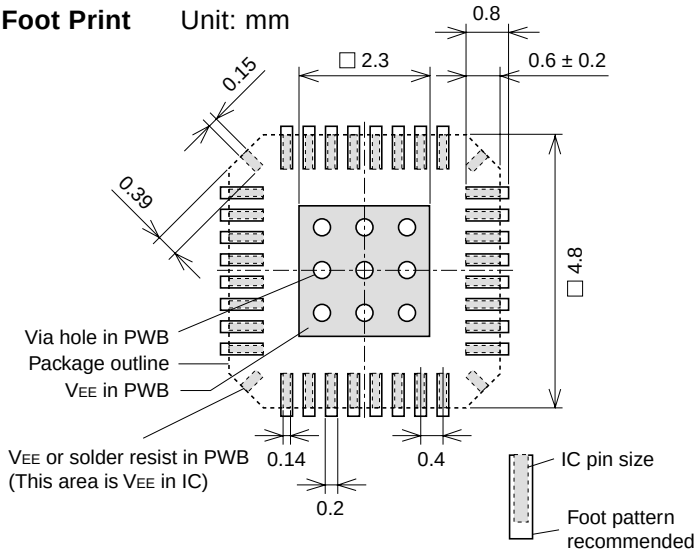


FP LD (λ = 1310nm)
Ta = 25˚C
Pattern = $PRBS^{23} – 1$
Data Rate = 2.5Gbps
Filter
Mask: OC-48

Time base: 100.0ps/div

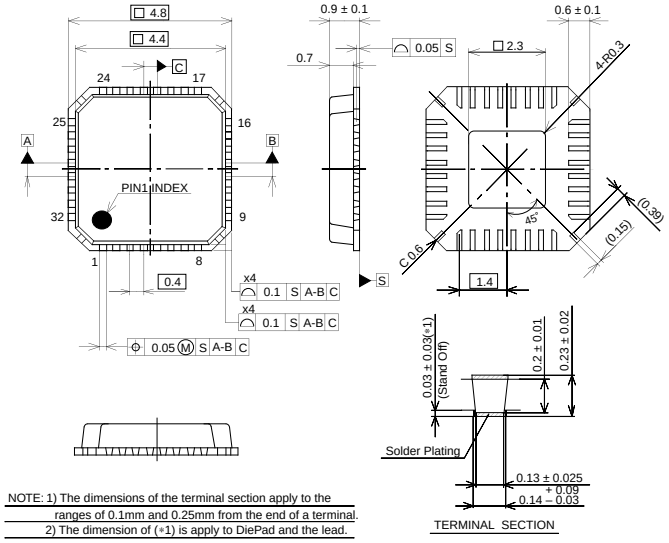
Fig. 17. Optical Output Waveform

Foot Print Unit: mm



Package Outline Unit: mm

32PIN VQFN (PLASTIC)



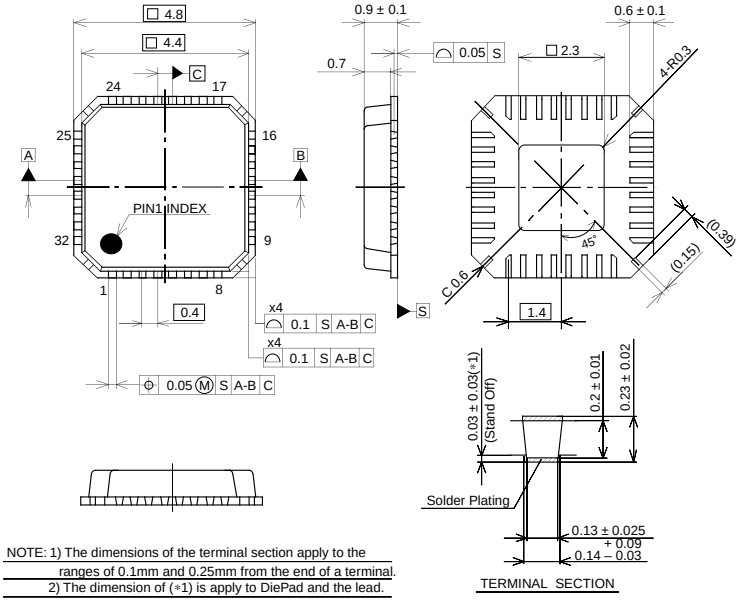
NOTE: 1) The dimensions of the terminal section apply to the ranges of 0.1mm and 0.25mm from the end of a terminal.
2) The dimension of (*1) is apply to DiePad and the lead.

SONY CODE	VQFN-32P-04
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.05g

32PIN VQFN (PLASTIC)



NOTE: 1) The dimensions of the terminal section apply to the ranges of 0.1mm and 0.25mm from the end of a terminal.
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SONY CODE	VQFN-32P-04
EIAJ CODE	————
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PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.05g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm