TOSHIBA Injection Enhanced Gate Transistor Silicon N Channel IEGT

# GT40Q321

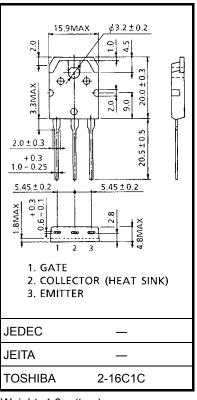
## Voltage Resonance Inverter Switching Application

Unit: mm

- Fifth-generation IGBT
- Enhancement mode type
- High speed :  $t_f = 0.41 \mu s$  (typ.) (IC = 40A)
- Low saturation voltage:  $V_{CE}$  (sat) = 2.8 V (typ.) (IC = 40A)
- FRD included between emitter and collector

# **Absolute Maximum Ratings (Ta = 25°C)**

Characteristics		Symbol	Rating	Unit	
Collector-emitter voltage		V <sub>CES</sub>	1200	V	
Gate-emitter voltage		$V_{GES}$	±25	V	
Continuous collector current	@ Tc = 100°C	lo	23	Α	
	@ Tc = 25°C	IC	42		
Pulsed collector current		I <sub>CP</sub>	80	Α	
Diode forward current	DC	lF	10	А	
	Pulsed	I <sub>FP</sub>	80		
Collector power dissipation	@ Tc = 100°C	D.	68	W	
	@ Tc = 25°C	P <sub>C</sub>	170	W	
Junction temperature		Tj	150	°C	
Storage temperature range		T <sub>stg</sub>	-55 to 150	°C	



Weight: 4.6 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high

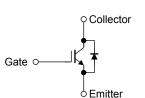
temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

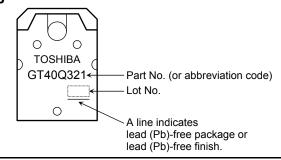
#### **Thermal Characteristics**

Characteristics	Symbol	Max	Unit
Thermal resistance (IGBT)	R <sub>th (j-c)</sub>	0.74	°C/W
Thermal resistance (diode)	R <sub>th (j-c)</sub>	1.79	°C/W

# **Equivalent Circuit**



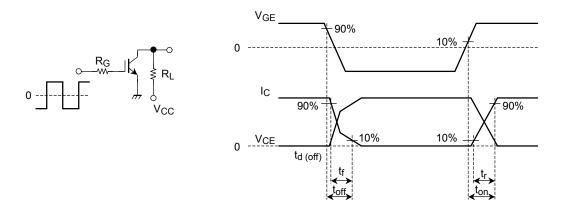
## Marking



## **Electrical Characteristics (Ta = 25°C)**

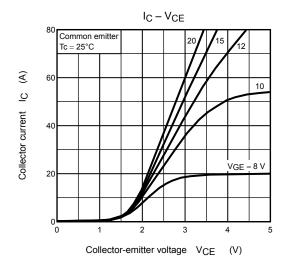
Chara	acteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cur	rent	I <sub>GES</sub>	V <sub>GE</sub> = ±25 V, V <sub>CE</sub> = 0	_	_	±500	nA
Collector cut-off of	current	I <sub>CES</sub>	V <sub>CE</sub> = 1200 V, V <sub>GE</sub> = 0	_	_	5.0	mA
Gate-emitter cut-	off voltage	V <sub>GE</sub> (OFF)	I <sub>C</sub> = 40 mA, V <sub>CE</sub> = 5 V	4.0	_	7.0	V
Collector-emitter	saturation voltage	V <sub>CE</sub> (sat)	I <sub>C</sub> = 40 A, V <sub>GE</sub> = 15 V	_	2.8	3.6	V
Input capacitance		C <sub>ies</sub>	V <sub>CE</sub> = 10 V, V <sub>GE</sub> = 0, f = 1 MHz	_	3200	_	pF
Switching time	Rise time	t <sub>r</sub>	Resistive Load	_	0.19	_	- µs
	Turn-on time	t <sub>on</sub>	V <sub>CC</sub> = 600 V, I <sub>C</sub> = 40 A	_	0.25	_	
	Fall time	t <sub>f</sub>	$V_{GG}$ = ±15 V, $R_{G}$ = 39 $\Omega$	_	0.41	0.72	
	Turn-off time	t <sub>off</sub>	(Note 1)	_	0.57	_	
Diode forward voltage V <sub>F</sub>		I <sub>F</sub> = 10 A, V <sub>GE</sub> = 0	_	_	2.0	V	
Reverse recovery time		t <sub>rr</sub>	I <sub>F</sub> = 10 A, di/dt = -20 A/μs	_	0.6	_	μs

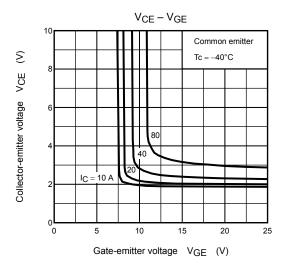
Note 1: Switching time measurement circuit and input/output waveforms

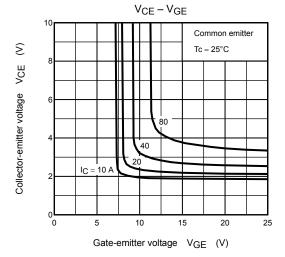


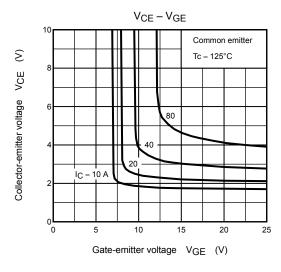
#### **General Safety Precautions and Usage Considerations**

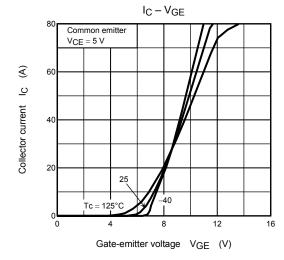
- The GT40Q321 is only intended for single-transistor voltage resonant circuits in induction heating (IH) equipment. For other applications, please contact your nearest Toshiba sales office.
- Do not use devices under conditions in which their maximum ratings will be exceeded. A device may break down or its performance may be degraded, causing thermal runaway or explosion resulting in injury to the user. It is therefore necessary to incorporate device derating into circuit design.
- In all IGBT devices, maximum collector-emitter voltage (VCES) decreases when the junction temperature becomes low. It is therefore necessary to incorporate device derating into circuit design.
- Maximum collector current is calculated from Tj MAX.(150°C), the thermal resistance and DC forward power dissipation. However it's limited in real application by another factor such as switching loss, limitation of the inner bonding wires and so on.

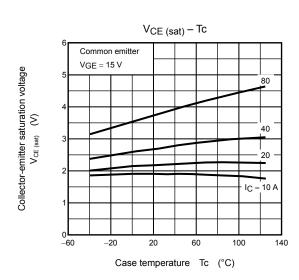




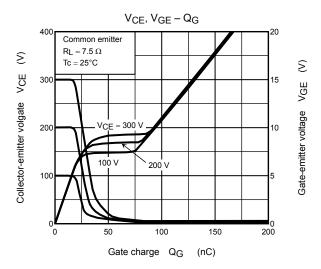


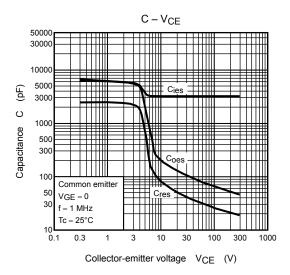


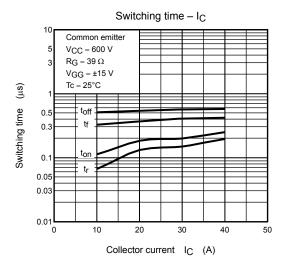


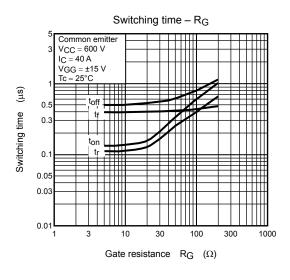


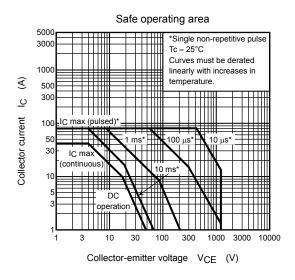
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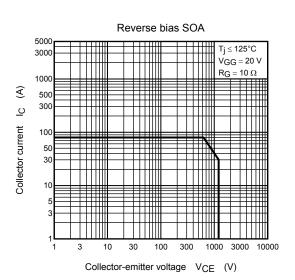


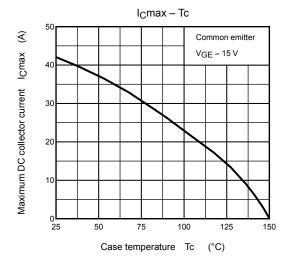


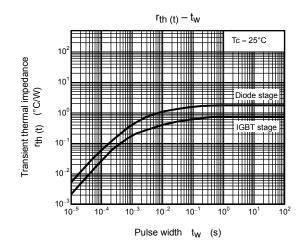


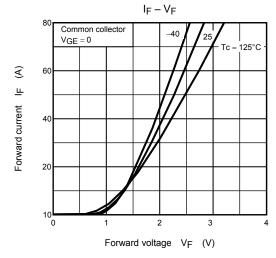


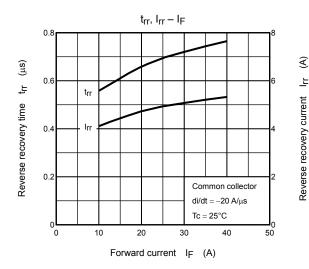


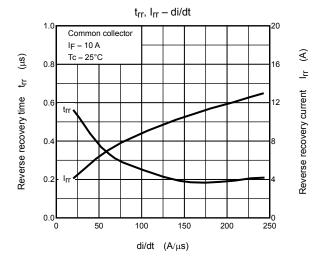












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