POWER MANAGEMENT

Description

The SC2615 is a fully integrated, **Three in One**, **Linear** DDR power solution providing power for the VDDQ and the VTT rails. The SC2615 completely adheres to the ACPI sleep state power requirements per Intel[R] motherboard specifications. A linear regulator controller provides the high current of the VDDQ during S0, via an external Power MOSFET, while an internal **1.8A (min)** sink/source regulator supplies the termination voltage.

In addition to these two blocks, an Internal LDO provides VDDQ power during S3, capable of sourcing **650 mA**. The SC2615 uses Intel[R] defined Latched BF_CUT signal which is also used to drive the external Blocking MOSFET. Additional logic, two UVLOs and three thermal shutdown circuits assure reliability of this single chip DDR power solution. A Power Good Output indicates the rails are in regulation.

A Soft Start/Enable pin assures proper startup and allows external shutdown control. The MLP package provides excellent thermal impedance while keeping a small footprint.

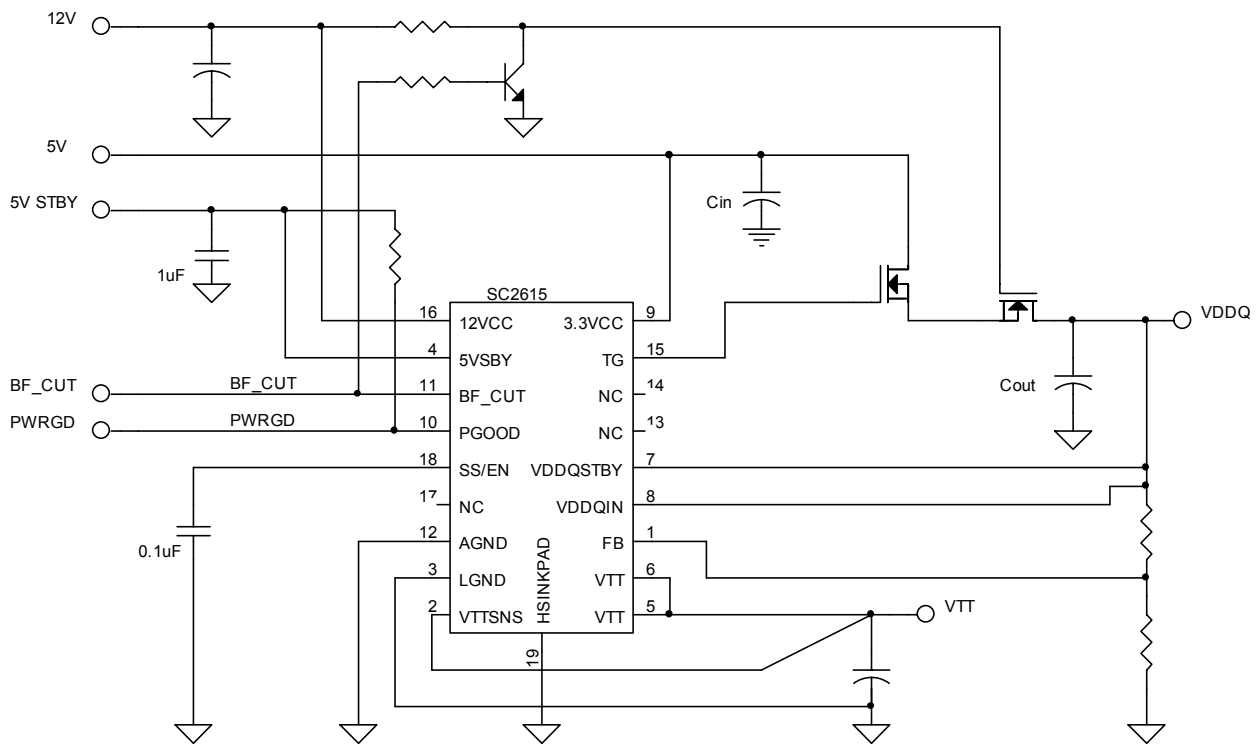
Features

- **Single chip solution adheres to ACPI sleep state requirements using BF_CUT**
- UVLO on 3.3V and 12V
- **Internal S3 state LDO for VDDQ supplies 650 mA**
- Dual thermal shutdown
- Fast transient response
- **Internal VTT regulator Sinks and Sources 1.8A (Min)**
- Power good output
- 18 pin MLP package

Applications

- DDR power solution for Intel[R] motherboard applications
- High speed data line termination
- Graphic cards
- Disk drives

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Input Supply Voltage, 3.3VCC	V_{CC3}	7	V
Input Supply Voltage, 12VCC	V_{CC12}	15	V
VTT Output Current	$I_{O(VTT)}$	±3	A
5V Standby Input Voltage	V_{5SB}	7	V
Inputs and Outputs	I/O	5VSTBY +0.3, GND -0.3	V
AGND to LGND		±0.3	V
Operating Ambient Temperature Range	T_A	0 to 70	°C
Operating Junction Temperature	T_J	125	°C
Thermal Resistance Junction to Ambient (1)	θ_{JA}	25	°C/W
Thermal Resistance Junction to Case (1)	θ_{JC}	4	°C/W
Storage Temperature	T_{STG}	-65 to 150	°C
Lead Temperature (Soldering) 10seconds	T_{LEAD}	300	°C
ESD Rating (Human Body Model)	ESD	2	kV

Electrical Characteristics

Unless specified: T_A = 0 to 70°C, V_{CC12} = 12V, V_{CC3} = 3.3V, 5VSTBY = 5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
3.3V Supply Voltage	$V_{CC3.3}$		3.0	3.3	3.6	V
12V Supply Voltage	V_{CC12}		10.8	12	13.2	V
5V Standby Voltage	V_{5SB}		4.5	5	5.5	V
5V STBY Input Quiescent Current	$I_{Q(STBY)}$	S0		2.4		mA
BF_CUT Threshold				TTL		
12V Under Voltage Lockout	$UVLO_{12}$		7	8.2	10	V
3.3V Under Voltage Lockout	$UVLO_{3.3}$		2.4	2.9	3.0	V
Feedback Reference	V_{REF}			1.25		V
Feedback Current	I_{FB}				2	µA
5V STBY in S3 Current	$I_{Q(STBY)}$			2	5	mA
SS/EN Shutdown Threshold	$V_{EN(TH)}$			0.2		V
Thermal Shutdown				150		°C

Electrical Characteristics (Cont.)

Unless specified: T_A = 0 to 70°C, V_{CC12} = 12V, V_{CC3} = 3.3V, 5VSTBY = 5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VDDQ Linear						
Output Voltage	V_{OUT}	DDR1	2.450	2.5	2.550	V
		DDR2	1.764	1.8	1.836	V
Soft Start Current	I_{SS}			25		µA
Overcurrent Trip Voltage	V_{TRIP}		50	60	70	%
Error Amplifier Bandwidth	BW			5		MHz
Load Regulation		T_{jmax}<125°C			2	%
Error Amplifier Gain	AOL			75		db
Power Good Low		1mA sink		50	400	mV
Power Good High Leakage		5V		0.1	2	µA
STBY LDO						
Output Current		S3	650			mA
Load Regulation		T_{jmax}<125°C			2	%
VTT LDO						
Source and Sink Currents(2)	I_{TT}		1.8	2.0		A
Load Regulation					2.5	%
Error Amplifier Gain	G_{EA}			75		db

Notes:

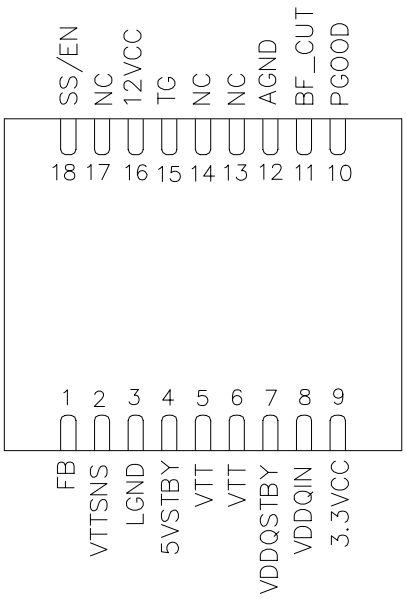
(1) Mounting considerations: The thermal copper pad on bottom of device must be soldered to a solid copper area, of 1 inch * 1 inch (min.) with multiple vias under the device to achieve specified θ_{JA} and θ_{JC}, (See recommended land pattern).

(2) This limit indicates that the regulator has a current limit threshold that is greater than the rated Minimum current. The rated current can only be achieved if the Absolute Maximum Junctions temperatures are not violated. The amount of heatsinking determines the maximum usable VTT current.

POWER MANAGEMENT

Pin Configuration

Top View



(MLP-18)

Ordering Information

Part Numbers	Package
SC2615MLTR(1)	MLP-18

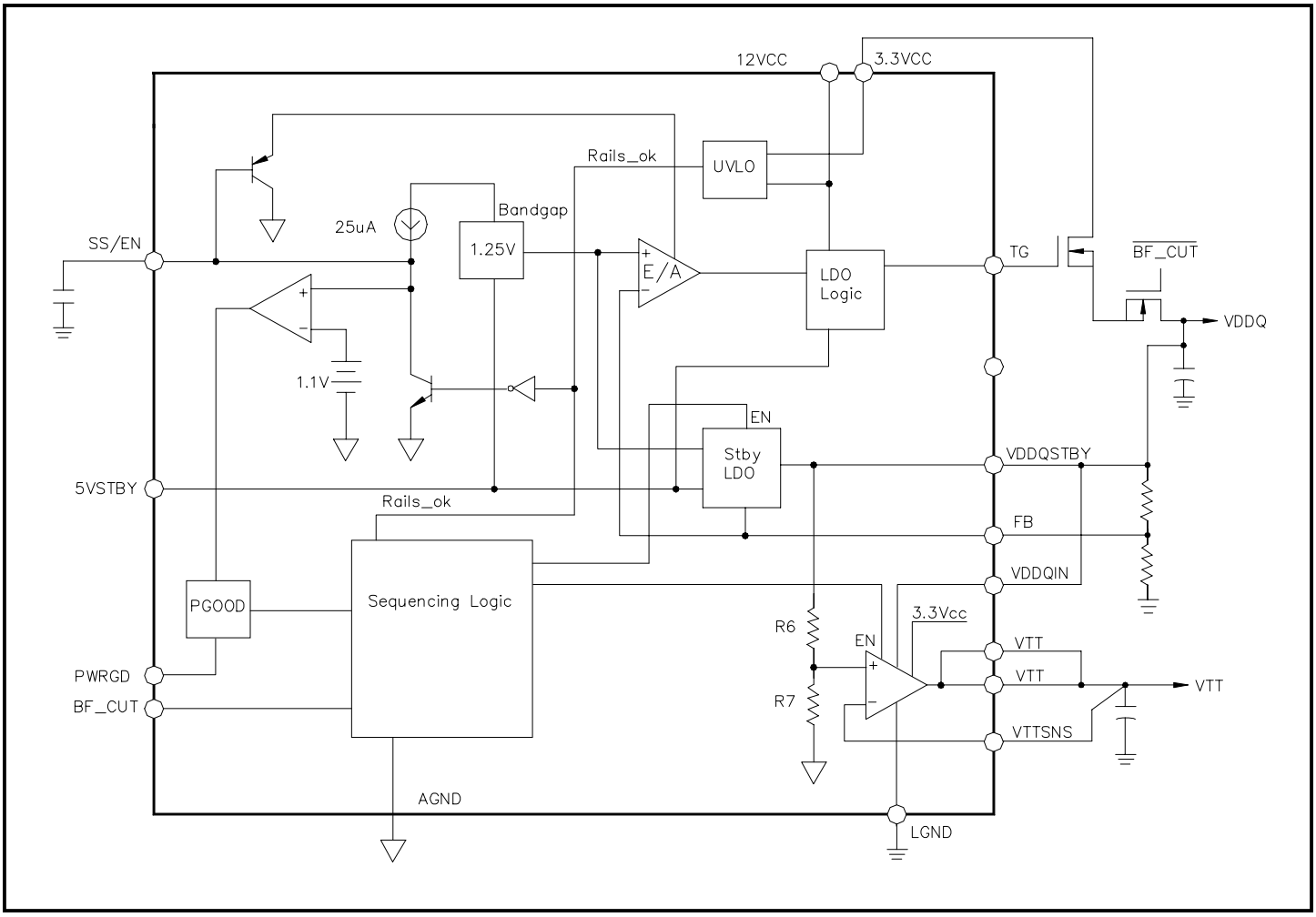
Notes:

(1) Only available in tape and reel packaging. A reel contains 3000 devices.

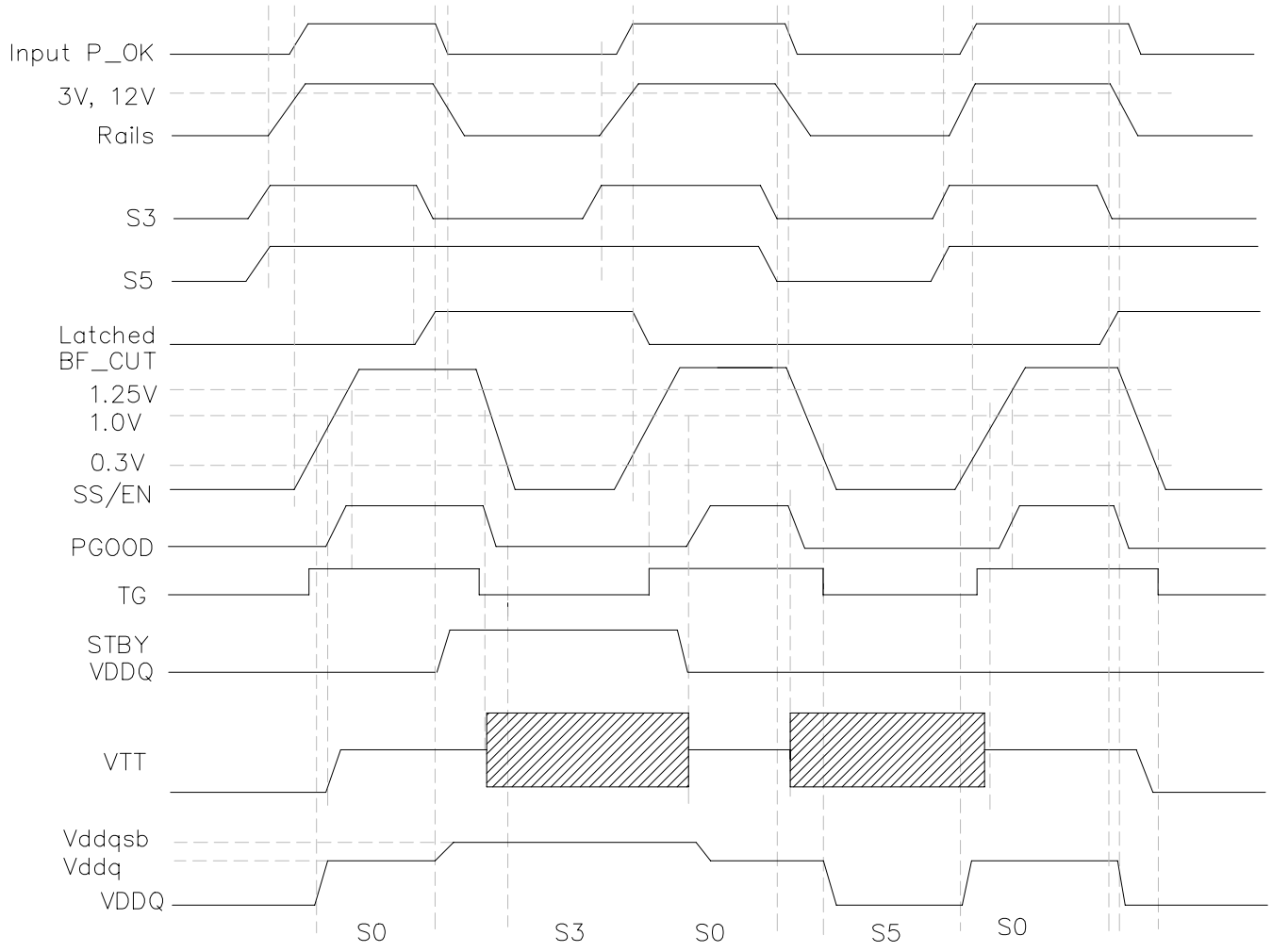
Pin Descriptions

Pin #	Pin Name	Pin Function
1	FB	Feedback for the VDDQ and standby LDO.
2	VTTSNS	V_{TT} LDO feedback and remote sense input.
3	LGND	VTT regulator ground.
4	5VSTBY	IC V_{CC} from 5V standby.
5,6	VTT	VTT regulator output. A 0.1µF - 1µF ceramic capacitor must be placed less than 0.25 inch from VTT pins to Ground.
7	VDDQSTBY	VDDQ "suspend to memory" regulator output.
8	VDDQIN	VDDQ supply input to V_{TT} regulator.
9	3.3VCC	Input Power rail.
10	PGOOD	VDDQ regulator power good indicator.
11	BF_CUT	BF_CUT signal from "Glue" chip. Controls the BF_CUT MOSFET during S3.
12	AGND	Analog ground.
13, 14	NC	No Connection.
15	TG	Regulator control for VDDQ output MOSFET.
16	12VCC	Supply for VDDQ control.
17	NC	No connection.
18	SS/EN	Soft start/Enable control.

Block Diagram



Timing Diagram



Applications Information

Description

The Semtech SC2615 DDR power supply controller is the latest and most complete linear regulator, providing the necessary functions to comply with the BF_CUT signal generated by Intel[R] Motherboards. The BF_CUT input signal is generated via an External "Glue Chip" and can be logically defined as :

BF_CUT=S0 .NAND.P_OK

Where S0 is the "Motherboard Active signal". When S0 is logic "Low", the motherboard is in S3 mode. The Latched BF_CUT signal is the input to the SC2615 controller, and is generated by using the S5 signal. All references made to BF_CUT are referring to the latched signal.

The BF_CUT signal is inverted to externally drive a Back_Feed_Cut MOSEFT, used to prevent current flow from the VDDQ supply back to the 3.3V supply during S3 state. VDDQ supply and the VTT termination voltages are supplied to the DDR SDRAM databus during S0 (normal operation) state. During S0, VDDQ is supplied via the an external pass MOSFET from the 3.3V rail , sourcing high output currents to the VDD bus as well as supplying the termination supply current.
The VTT termination voltage is an internal sink/source linear regulator, which during S0 state receives its power from the VDDQ bus. It is capable of sourcing and sinking 1.8 Amps (Min) . The current limit on this pin is set to 3 Amps (typical). The current handling capacity of this pin depends upon the amount of heat the PC board can sink from the SC2615 thermal pad. (See mounting instructions). The PC board layout must take into consideration the high current paths, and ground returns for both the VDDQ and VTT supply pins. VTT, LGND, VDDQ, 3.3VCC traces must also be routed using wide traces to minimize power loss and heat in these traces, based on the current handling requirements.

S3 and S5 States

The operation of the VDDQ and VTT supplies is governed by the internal sequencing logic in strict adherence with Intel[TM] specifications with regards to the BF_CUT signal. The timing diagram demonstrates the state of the controller, and each of the VDDQ and VTT supplies during S3 and S5 transitions. When S3 is low, the VDDQ internal regulator supplies the "Suspend To RAM" current of 650 mA (max) to maintain the information in memory while in standby mode. Since the Memory read/write cycles are suspended during S3, the VTT termination voltage is not needed and is tri-stated during S3. Once BF_CUT goes low, signifying S0 mode, the VDDQ supply recovers and takes control of the VDDQ bus.
The memory read-write cycles start after the Silver box POWER_OK signal goes high. The Silver-Box supply POWER_OK signal goes high when all the voltages are within a tight tolerance of the nominal voltage (typically with 1-2%). Thus, the transition from S3 to S0 does not cause a drop out in VDDQ voltage, since the higher VDDQ currents follow the transition of POWER_OK signal from the input Silver Box supply. The External VDDQ MOSFET, which is capable of supplying the higher current, is activated from the UVLO transition of the Input Rails, which occur much earlier. Thus the External MOSFET will be activated in time for the Memory's Active state.

Initial Conditions

When the S5 and S3 go high (BF_CUT goes low) for the first time, the VDDQ is supplied via the external MOSFET, thus removing the burden of charging the output capacitors via the internal linear VDDQ regulator.

Reset/restart

The SS/EN pin must be pulled low and high again to restart the SC2615. This can be achieved by cycling the input supplies, 3.3VCC/12VCC. There is a 50mV Hysteresis on the UVLO threshold. When the rails are near the UVLO thresholds, it is possible for noise to trigger the UVLO. Since the reference for the UVLO threshold is derived from the 5VSBY voltage, sufficient bypassing of the 5VSBY improves noise immunity of the UVLO circuit. The Short Circuit Protection function is disabled when any of the input rails are below their respective UVLO thresholds.

Back-feeding the Input Supply

When in S3 state, VDDQ is supplied by the internal linear regulator. Current can flow back from the VDDQ supply through the body diode of the Top MOSFET to the 3.3V input supply from the Silver Box, which is off during this state. This in turn shorts out the VDDQ bus and is not

desirable.

A MOSFET in series with the top pass MOSFET (See typical application circuit) must block this reverse current during S3. This MOSFET can be driven from the inverted BF_CUT signal. By removing the gate drive for this series MOSFET, the current path from the VDDQ supply back into the input power source is removed. This MOSFET is enhanced during S0 state.

Short Circuit Protection

Short Circuit Protection is implemented by sensing the VDDQ voltage. If the SS/EN pin has risen above 1.25V (i.e. the controller has completed the startup cycle), and the output falls to 60% of its nominal voltage, as sensed by the FB pin, the TG pin is latched off and the linear controllers shut down. To recover from this condition, either the power rails have to be recycled, or the SS/EN pin must be pulled low and released to restart controller operation. The short circuit protection function is disabled when any of the input rails are below their respective UVLO thresholds.

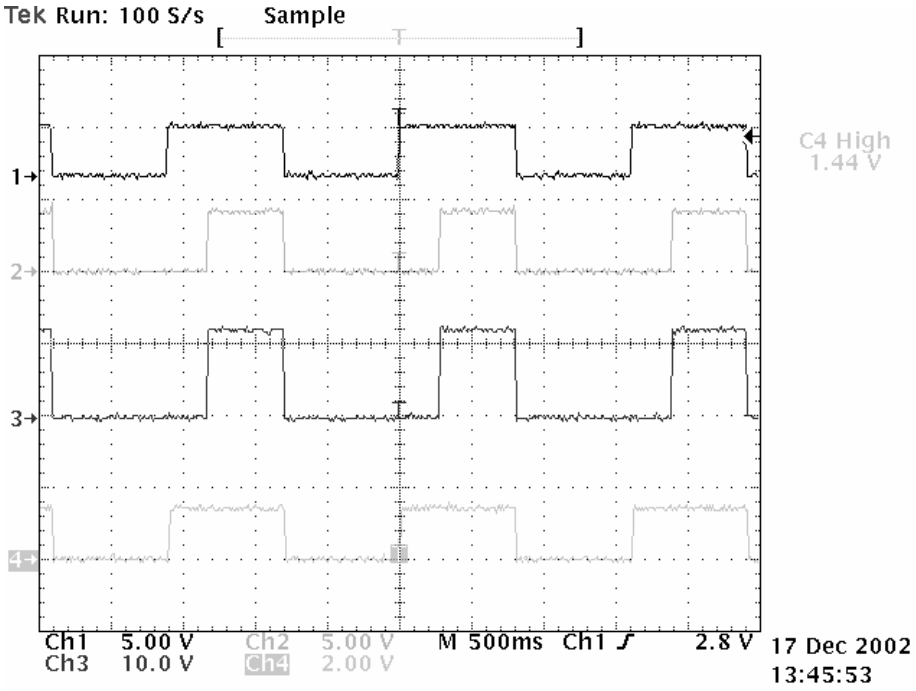
Thermal Shutdown

There are three independent Thermal Shutdown protection circuits in the SC2615, the VDDQ linear regulator the VTT source regulator, and the VTT sink regulator. If any of the three regulators' temperature rises above the threshold, that regulator will turn off independently, until the temperature falls below the thermal shutdown limit.

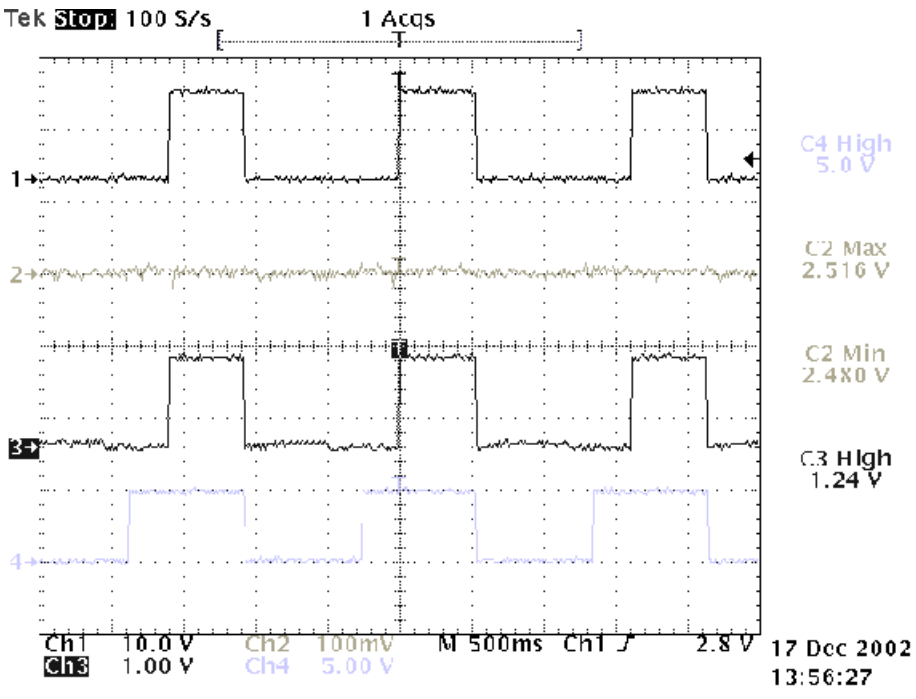
Power Good

An open collector output provides indication that the VDDQ is regulating. This is accomplished by monitoring the SS/EN pin. When the voltage on this pin has risen above 1.0V, the PGOOD goes high (open). When BF_CUT goes high (standby), the 5V and 12V rails go low, and the SS/EN also goes low. Subsequently, PWRGD will also go low, and stays low until the 3.3V and/or 12V rails are recycled and rise above their respective UVLO thresholds.

Typical Characteristics

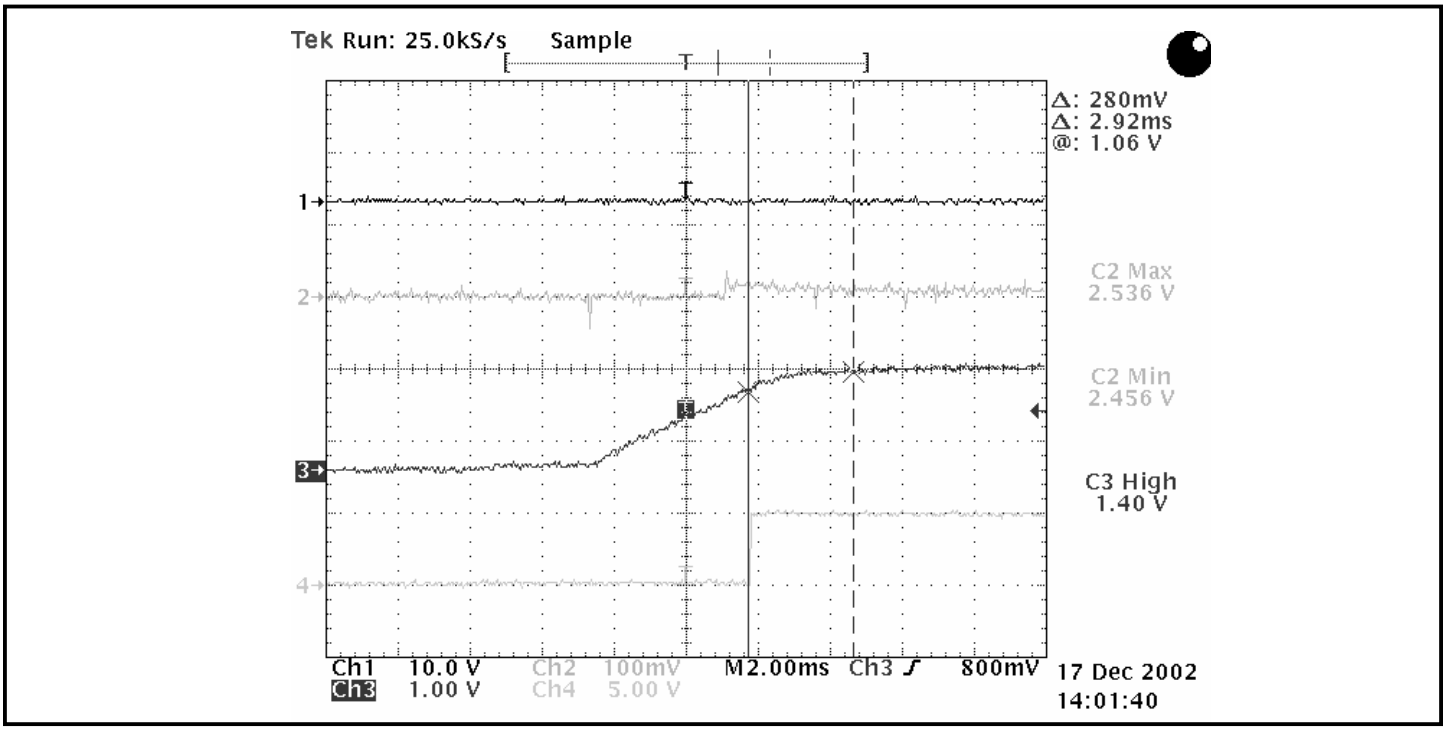


SC2615 DDR controller's timing : BF_CUT generated from S3 and P_OK
Ch1: S3 signal to Silverbox
Ch2: Power_OK from Silverbox
Ch3: BF_CUT(NOT)=S3.AND.P_OK
Ch4: SS/EN



SC2615 DDR controller's timing : VDDQ and VTT vs. BF_CUT
Ch1: BF_CUT (NOT)
Ch2: VDDQ with 2.5V offset, @ 650mA
Ch3: VTT @ 650 mA
Ch4: PGOOD output

Typical Characteristics (Cont.)



SC2615 DDR controller's timing : Power Good vs. SS/EN pin
Ch1: BF_CUT (NOT)
Ch2: VDDQ with 2.5V offset, @ 650mA
Ch3: VTT @ 650 mA
Ch4: PGOOD output

Mounting Considerations

Description

The MLP18 is a leadless package whose electrical connections are made by lands on the bottom surface of the component. These lands are soldered directly to the PC board. The MLP has an exposed die attach pad, which enhances the thermal and electrical characteristics enabling high power applications. Power handling capability of the MLP package is typically >2x the power of other SMT packages. In order to take full advantage of this feature the exposed pad must be physically connected to the PCB substrate with solder.

Thermal Pad Via Design

Thermal data (θja) for the MLP18 is based on a 4 layer PCB incorporating vias which act as the thermal path to other layers. (Ref: Jedec Specification JESD 51-5). Based on thermal performance, four-layer PCB's with vias are recommended to effectively remove heat from the device. Vias should be 0.3mm diameter on a 1.2mm pitch, and should be plugged to prevent voids being formed between the exposed pad and PCB thermal pad due to solder escaping by capillary action. Plugging can be accomplished by "tenting" the via during the solder mask process. The via solder mask diameter should be 100µm larger than the via diameter.
Two layer boards have no vias, thus any heat sinking must be accomplished in the same plane as the metal traces. This will typically require an increase in the PC board area.

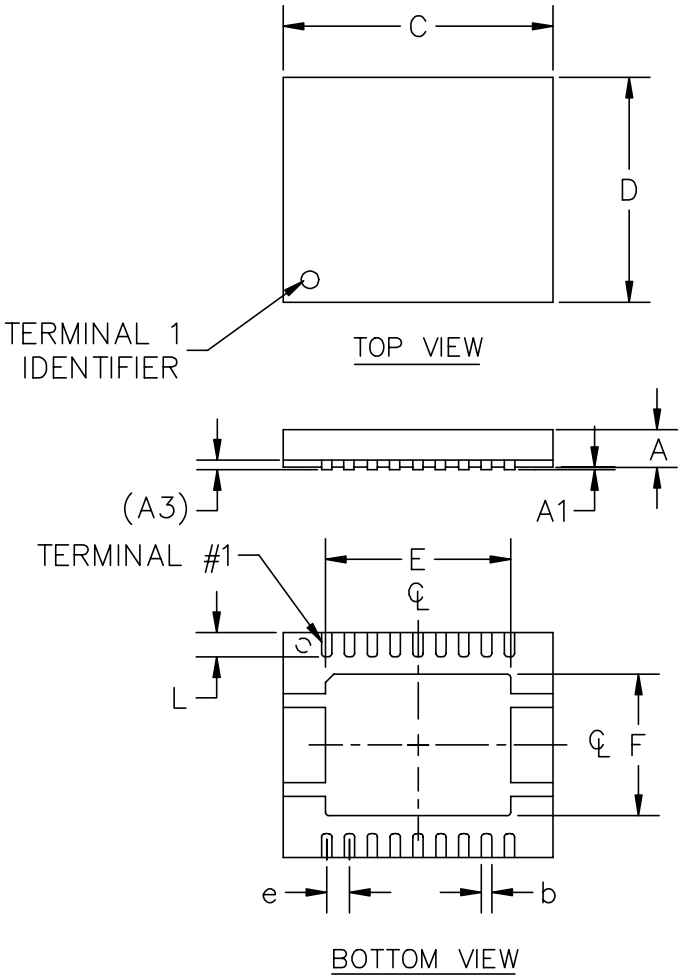
Solder Mask

Design the solder mask around all pads on each side, i.e. there should be no solder mask between adjacent terminal fingers.

Exposed Pad Stencil Design

It is good practice to minimize the presence of voids within the exposed pad inter-connection. Total elimination is difficult but the design of the exposed pad stencil is important, a single slotted rectangular pattern is recommended. (If large exposed pads are screened with excessive solder, the device may "float", thus causing a gap between the MLP terminal and the PCB land metalization.) The proposed stencil designs enables out-gassing of the solder paste during reflow as well as controlling the finished solder thickness.

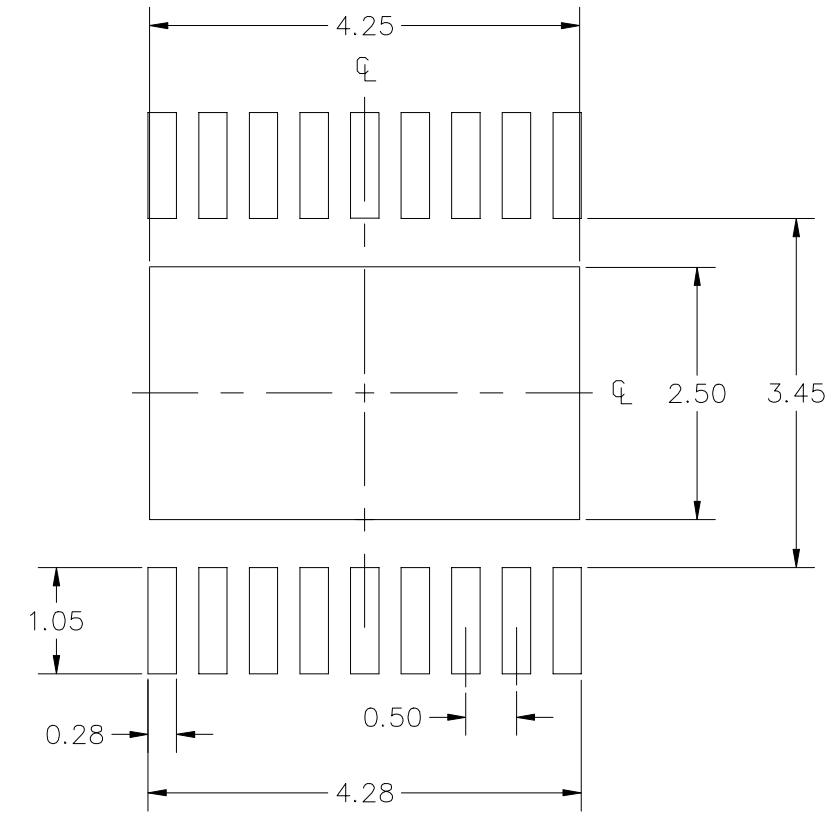
Outline Drawing - MLP-18



DIMENSIONS					
DIM[N]	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.032	.039	0.80	1.00	–
A1	0	.002	0	0.05	–
A3	–	.008	–	0.20	REF
b	.007	.012	0.18	0.30	–
C	.236		6.00		NOM
D	.197		5.00		NOM
E	.157	.167	4.00	4.25	–
F	.118	.128	3.00	3.25	–
e	.020 BSC		0.50 BSC		–
L	.017	.026	0.45	0.65	–

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

Land Pattern - MLP-18



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