

Four channel valve driver

Data Brief

Features

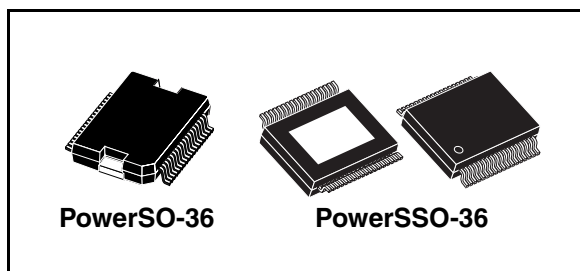
- Four low-side output drivers with protection diagnostic
 - 2 PWM controlled channels (0.2Ω typ)
 - 2 current controlled channels with 6% accuracy (0.3Ω typ)
- All outputs with 35V Zener clamp
- Programmable channel timer
- Clock monitor
- Integrated recirculation diodes
- Serial Peripheral Interface with 16bits, up to 5MHz with diagnosis
- Battery compatible supply voltage
- Detailed Load diagnosis
 - Over load protection
 - Open Load
 - Under-current
 - Under Voltage
 - Temperature Warning and Shutdown
 - Power or Signal GND loss
 - Freewheeling diode loss
 - Silent valve driver test

Description

The L9374 is a four channel low side driver with integrated recirculation diodes. The switching of the channels is programmable via a SPI (Serial Peripheral Interface). The main time base is given by an external clock via CLKin. The Clock Unit monitors this external clock and provides the system clock for all timings.

A Synchronization Unit is used to monitor the SPI communication and provides a sync signal for the channel activation.

The Output Duty Cycle for each channel can be programmed individually and will be activated by the Set Point Unit. Is possible to program two output Duty Cycles per channel with a block of 16 SPI commands as well as an individual Duration Time for each channel actuation. Both information



are stored in the PWM and in the Counter Configuration Register respectively. The PWM Controller translates the programmed digital duty cycle value in a PWM signal which controls the output.

For the current controlled channels the target current value is programmed. It is also possible to program two different target currents. The target current is compared with the real load current. The output duty cycle is then calculated with an Arithmetic Logic Unit. As base for the calculation a load model is used respecting the resistivity of the load, the supply voltage as well as the internal recirculation path. To check the plausibility of the current controller all measured and calculated values are available and accessible via SPI.

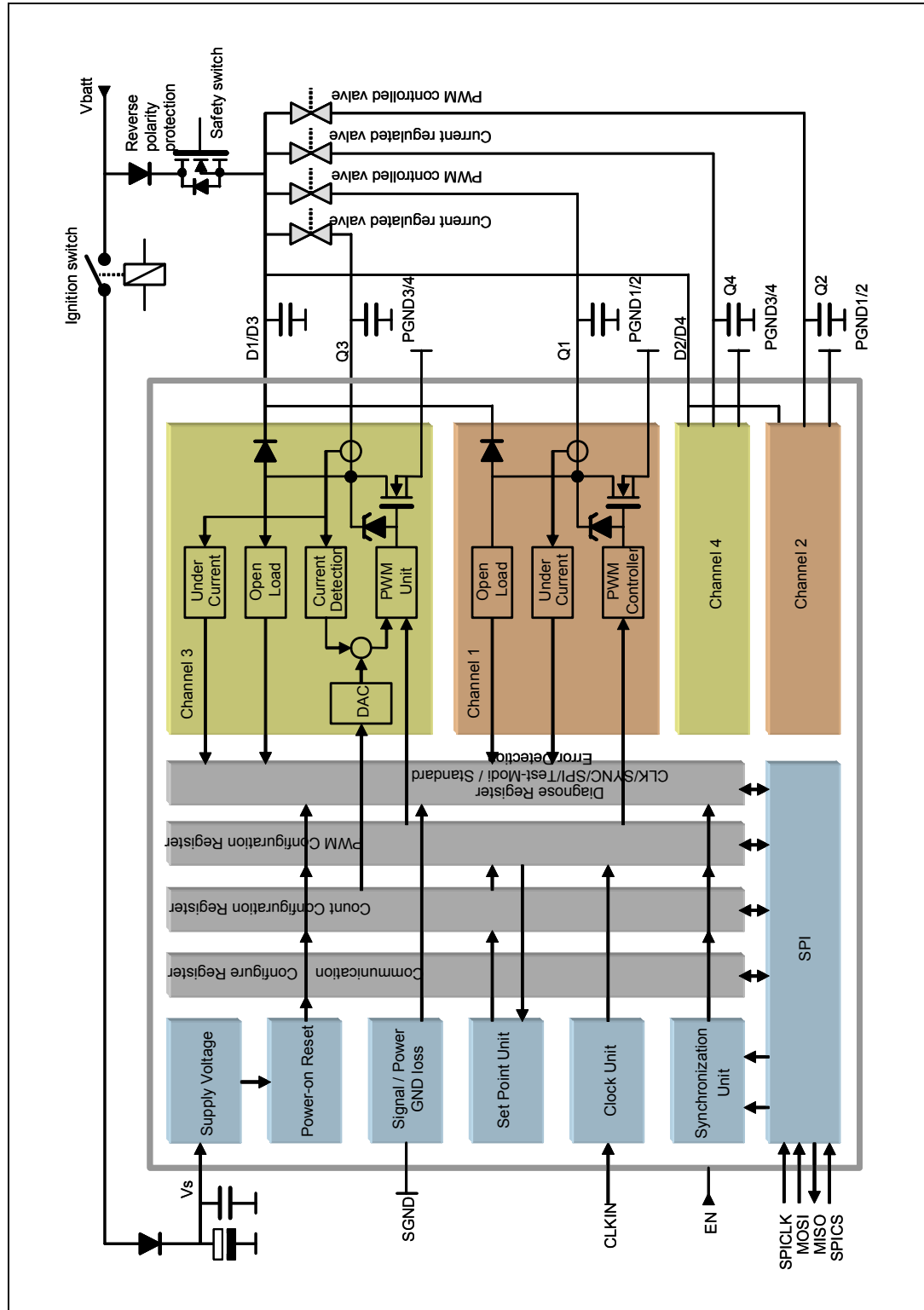
All channels are equipped with a load Diagnostic. This allows to detect an open load in off condition as well as an under current in on condition. The power stage is protected against over current and over temperature. A weak connection in power ground or in the recirculation path is monitored. All monitored functions can be read out in a serial diagnostic protocol dedicated for each channel via SPI..

Table 1. Device summary

Order code	Package	Packing
L9374	PowerSO-36 (slug down)	Tube
L9374XP	PowerSSO-36 (exp. pad)	Tube

1 Block diagram

Figure 1. Block diagram



2 Pins description

Figure 2. PowerSSO36 pins connection (top view)

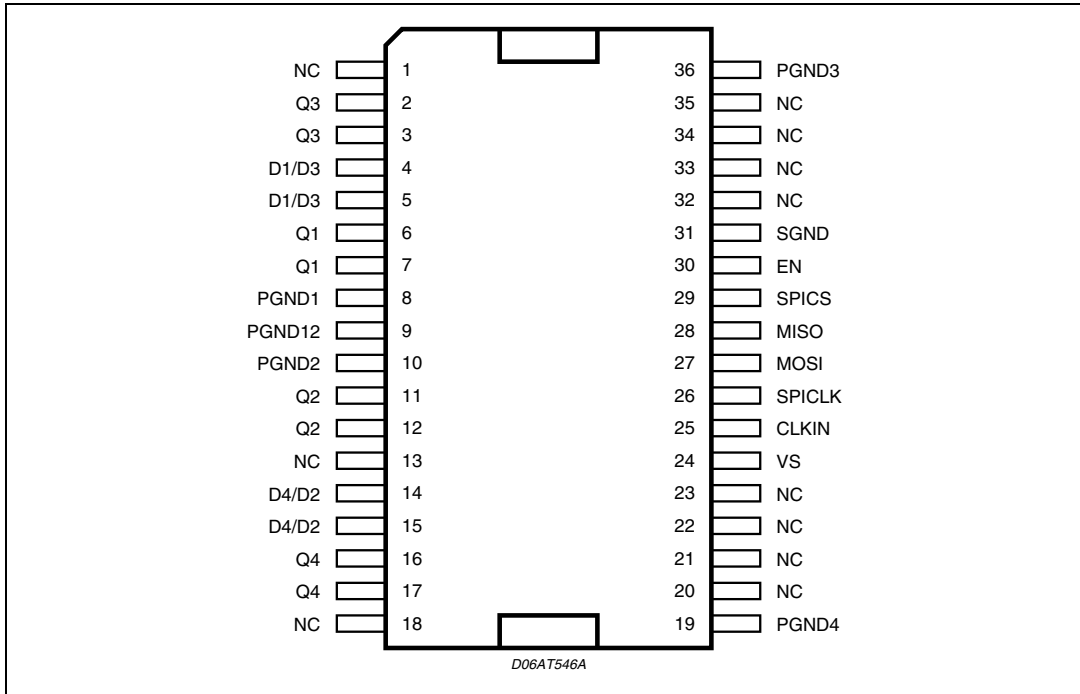


Figure 3. PowerSO36 pins connection (top view)

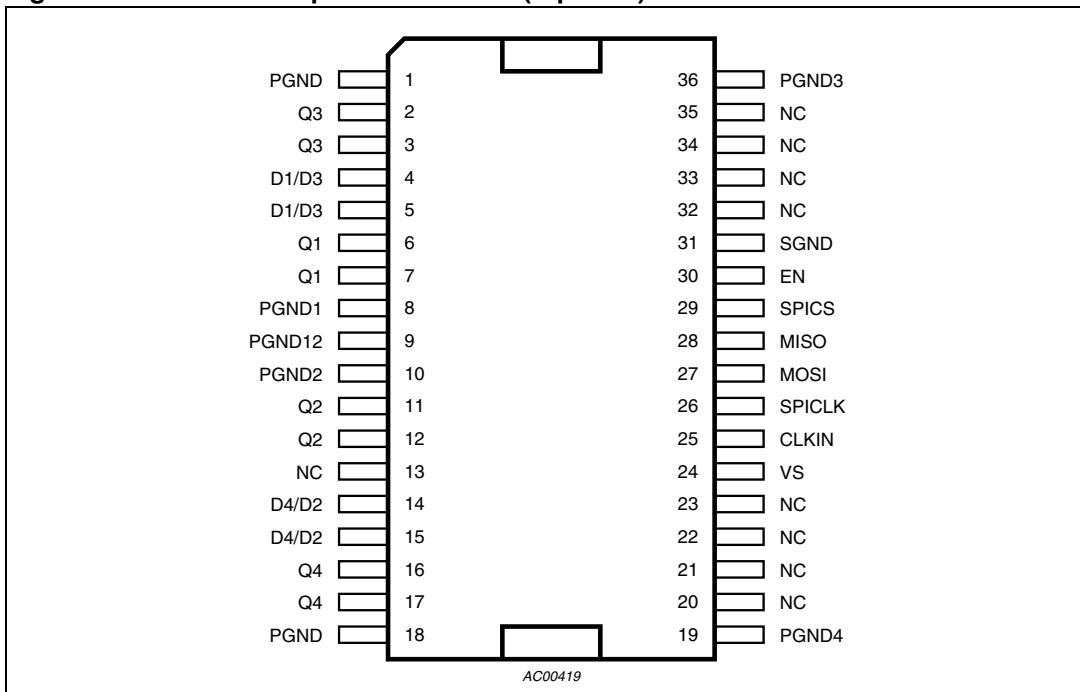


Table 2. Pins description

Pin No.	PwSSO36	PwSO36	Description
1	N.C.	PGND	Not connected/Power ground
2	Q3	Q3	Output.
3	Q3	Q3	Output.
4	D1/D3	D1/D3	Free wheeling diode.
5	D1/D3	D1/D3	Free wheeling diode.
6	Q1	Q1	Output.
7	Q1	Q1	Output.
8	PGND1	PGND1	Power ground of the output driver 1 & 2.
9	PGND12	PGND12	Power ground of the output driver 1 & 2.
10	PGND2	PGND2	Power ground of the output driver 1 & 2.
11	Q2	Q2	Output.
12	Q2	Q2	Output.
13	N.C.	N.C.	Not connected.
14	D4/D2	D4/D2	Free wheeling diode.
15	D4/D2	D4/D2	Free wheeling diode.
16	Q4	Q4	Output.
17	Q4	Q4	Output.
18	N.C.	PGND	Not connected/Power ground
19	PGND4	PGND4	Power ground of the output driver 4.
20	N.C.	N.C.	Not connected.
21	N.C.	N.C.	Not connected.
22	N.C.	N.C.	Not connected.
23	N.C.	N.C.	Not connected.
24	VS	VS	Supply pin
25	CLKIN	CLKIN	Input for precise clock.
26	SPICLK	SPICLK	SPI communication CLoCK.
27	MOSI	MOSI	Master Out Slave In for SPI communication.
28	MISO	MISO	Master In Slave Out for SPI communication.
29	SPICS	SPICS	SPI Chip Select.
30	EN	EN	Enable
31	SGND	SGND	Signal ground.
32	N.C.	N.C.	Not connected.
33	N.C.	N.C.	Not connected.
34	N.C.	N.C.	Not connected.
35	N.C.	N.C.	Not connected.
36	PGND3	PGND3	Power ground of the output driver 3.

3 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_s	Supply voltage	-0.3	38	V
V_{Dx}	Freewheeling diode voltage	-0.3	35	V
V_{Qx}	Output voltage	-0.3	35	V
V_{EN} V_{SPICLK} V_{SPICS} V_{MOSI} V_{MISO} V_{CLKIN}	Enable voltage SPI clock voltage SPI chip select voltage SPI MOSI voltage SPI MISO voltage SPI clock input voltage	-0.3	6	V
$I_{Q1; 2}$	Output current at reversal voltage		-4	A
$I_{Q3; 4}$			-2	A
I_{EN_CL} I_{SPICLK_CL} I_{SPICS_CL} I_{MOSI_CL} I_{CLKIN_CL}	Input clamping currents (static) Input clamping currents (dynamic)	-3 -10	+3 +10	mA

Definition: Current from outside into the L9374-> " + "
Current from L9374 towards external components -> " - "

Warning: Transients beyond this limit will cause currents into ESD structures which must be limited externally to ± 10 mA (maximum energy to be dissipated: 2 mJ).

4 ESD susceptibility

4.1 HBM

ESD susceptibility HBM according to EIA/JESD 22-A 114B otherwise defined.

Table 4. HBM

Pin	Condition	Min	Max	Unit
All Pins		± 2		kV
Output pins D _X ; Q _X ;	PGND12, PGND3, PGND4, LGND and GND are connected together.	± 4		kV

4.2 MM

ESD susceptibility according to EIA/JESD22-A115-A

Table 5. MM

Parameter	Condition	Min	Max	Unit
Machine Model (MM)	All pins	± 250		V

5 Package informations

In order to meet environmental requirements, ST offers this device in ECOPACK® package. This package has a Lead-free second level interconnect. The category of second level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at: www.st.com.

Figure 4. PowerSO-36 (slug down) mechanical data and package dimensions

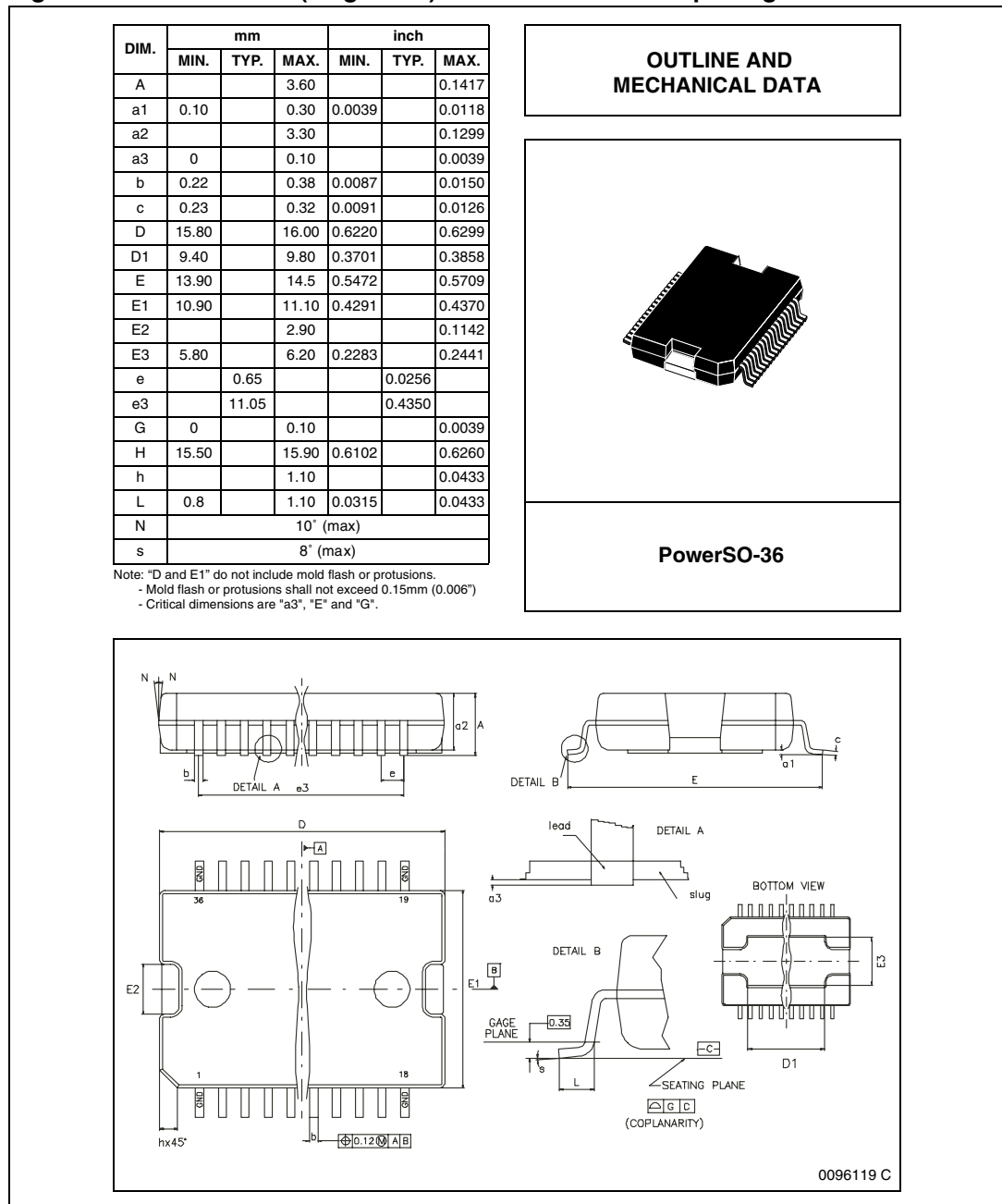
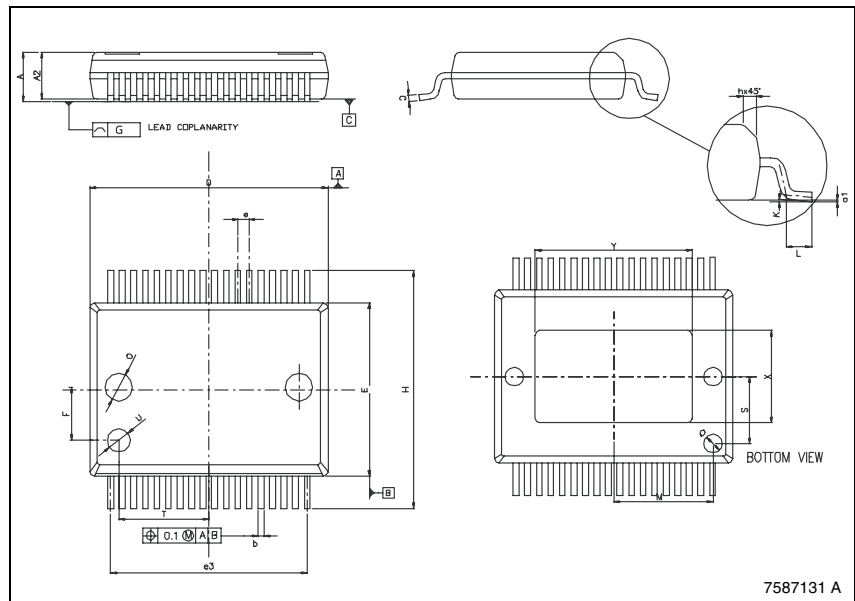
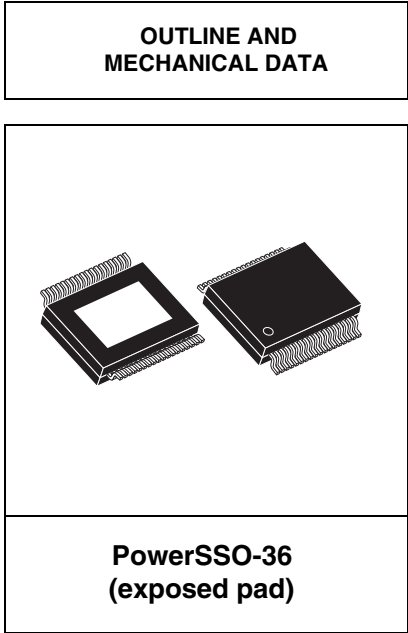


Figure 5. PowerSSO-36 (exposed pad) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.15		2.47	0.084		0.097
A2	2.15		2.40	0.084		0.094
a1	0		0.075	0		0.003
b	0.18		0.36	0.007		0.014
c	0.23		0.32	0.009		0.012
D (1)	10.10		10.50	0.398		0.413
E (1)	7.4		7.6	0.291		0.299
e		0.50			0.020	
e3		8.50			0.035	
F		2.3			0.090	
G			0.10			0.004
G1			0.06			0.002
H	10.10		10.50	0.398		0.413
h			0.40			0.016
L	0.55		0.85	0.022		0.033
M		4.3			0.169	
N			10° (max)			
O		1.2			0.047	
Q		0.8			0.031	
S		2.9			0.114	
T		3.65			0.144	
U		1.0			0.039	
X	4.10		4.70	0.161		0.185
Y	6.50		7.10	0.256		0.279

- (1) "D and E" do not include mold flash or protrusions.
Mold flash or protrusions shall not exceed 0.15mm (0.006")
- (2) No intrusion allowed inwards the leads.
- (3) Flash or bleeds on exposed die pad shall not exceed 0.4 mm per side



6 Revision history

Table 6. Document revision history

Date	Revision	Changes
4-Jun-2007	1	Initial release.
31-Jul-2007	2	Updated <i>Section 1: Block diagram</i> , <i>Section 2: Pins description</i> and <i>Section 4: ESD susceptibility</i> .

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