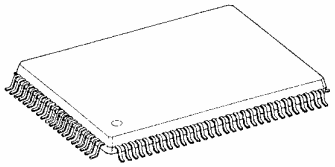
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC93P24FG

Single-Chip DTS Microcontroller (DTS-20)

The TC93P24FG is a single-chip digital tuning system (DTS) microcontroller incorporating a 230 MHz prescaler, PLL, and LCD driver. In addition to a 20-bit IF counter, an 8-channel, 8-bit AD converter, two types of serial interface, and buzzer function, the TC9324FG offers a range of functions required for DTS, including an interrupt function, an 8-bit timer-counter, and an 8-bit pulse counter. In addition, the LCD driver features six modes combining 1/4, 1/3, and 1/2 duty and 1/2 and 1/3 bias. This product is suitable for use in a wide variety of DTS systems, from automobile to home audio, including compact stereo systems.



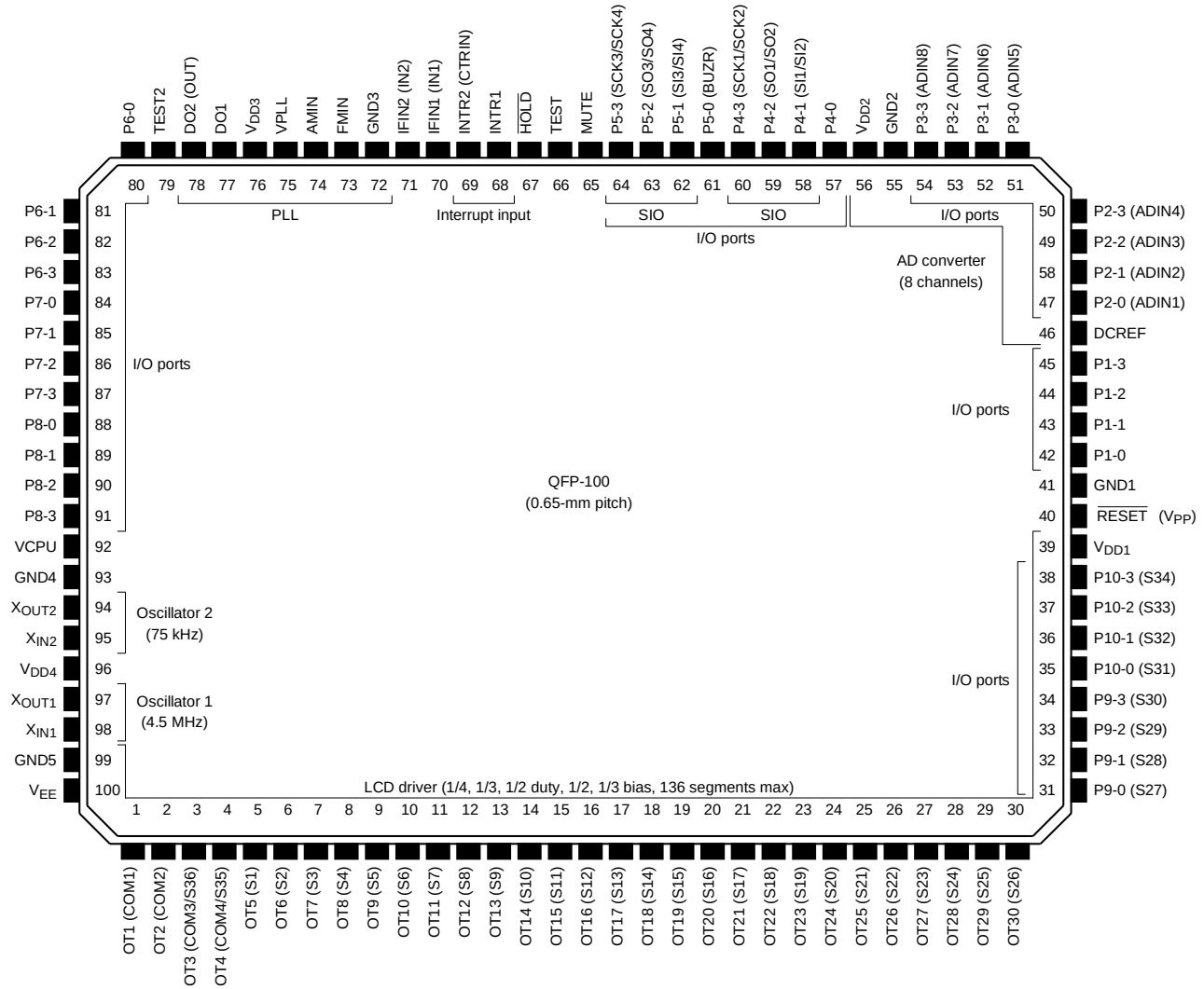
QFP100-P-1420-0.65Q

Weight: 1.6 g (typ.)

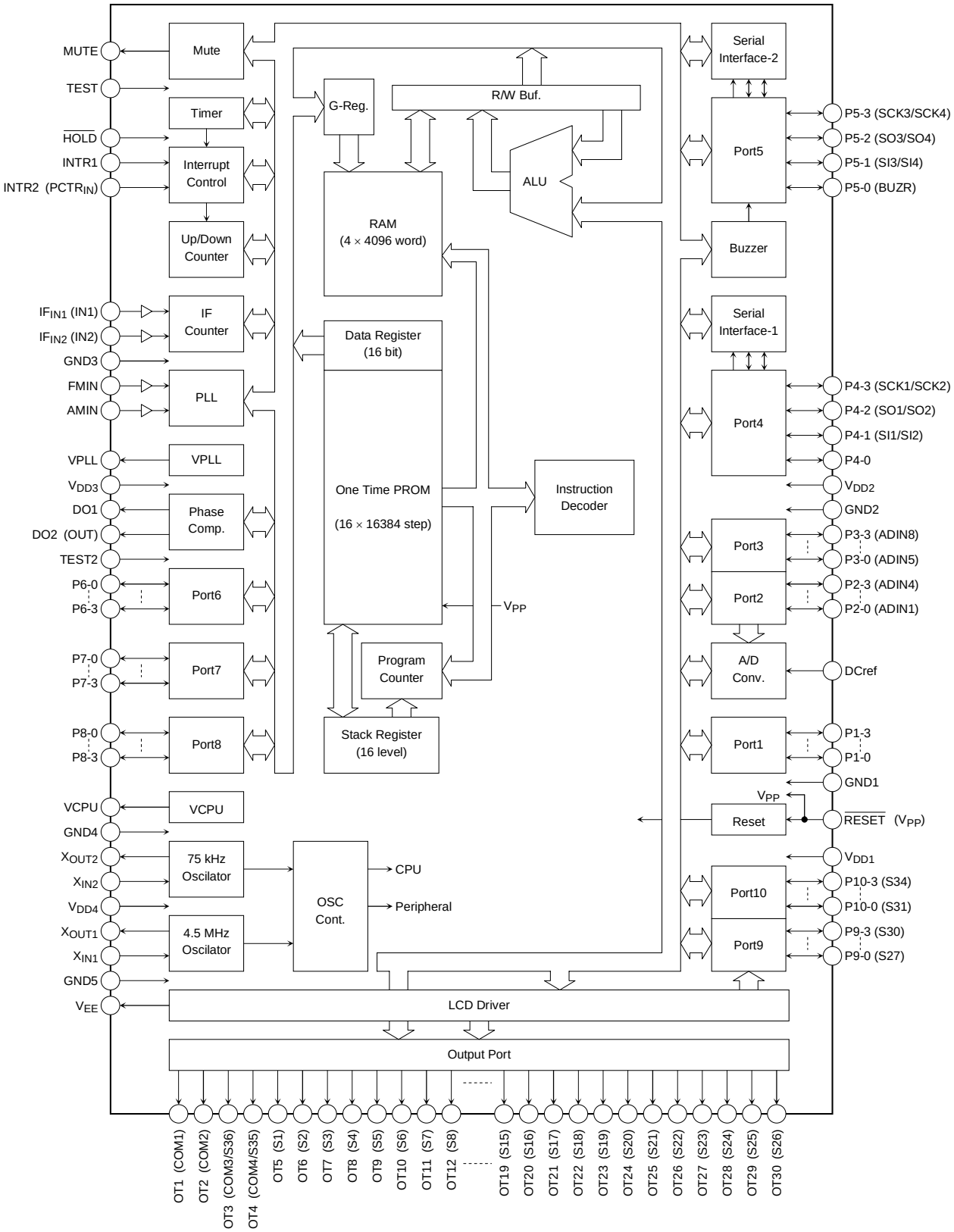
Features

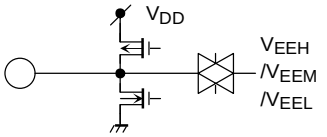
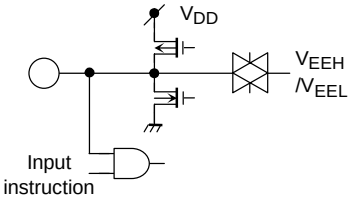
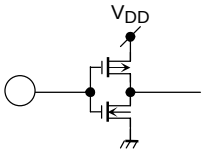
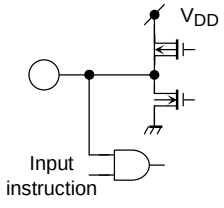
- CMOS DTS microcontroller LSI with built-in 230 MHz prescaler, PLL, and LCD driver
- Operating voltage: PLL operating: VDD = 4.0 to 5.5 V (typ. 5.0 V)
  PLL off: VDD = 3.5 to 5.5 V (when CPU only operating)
- Crystal oscillator frequency: 4.5 MHz, 75 kHz
- Current dissipation: PLL operating: IDD = 3 mA (typ.) (crystal oscillator frequency 4.5 MHz, VHF mode)
  PLL off: IDD = 1 mA (typ.) (crystal oscillator frequency 4.5 MHz, CPU only operating)
  PLL off:IDD = 0.3 mA (typ.) (crystal oscillator frequency 75 kHz, CPU only operating)
- Operating temperature range: Ta = −40 to 85°C
- Program memory (ROM): 16 bits × 16,384 steps
- Data memory (RAM): 4 bits × 4,096 words
- Instruction execution time: 1.78 μs (crystal oscillator frequency 4.5 MHz)
  40 μs (crystal oscillator frequency 75 kHz)
- Stack levels: 16
- General-purpose IF counter: 20-bit (CMOS input supported)
- AD converter: 8 bits × 8 channels
- LCD driver: 1/4, 1/3, 1/2 duty, 1/2, 1/3 bias modes selectable, 136 segments maximum
- I/O ports: CMOS I/O ports: 40
  Output-only ports: Up to 31. Input-only ports: Up to 5
- Timer-counter: 8-bit (as timer clock: INTR1, INTR2, instruction cycle, 25kHz, or 1 kHz selectable)
- Pulse counter: 8-bit up/down counter (input from INTR2 pin)
- Buzzer: 0.625 to 3 kHz (8 settings)
  Four modes: Continuous, Single-Shot, 10-Hz Intermittent, 10-Hz Intermittent at 1-Hz Intervals
- Interrupts: 2 external, 4 internal (three types of serial interface, 8-bit timer)
- Package: QFP-100 (0.65-mm pitch)

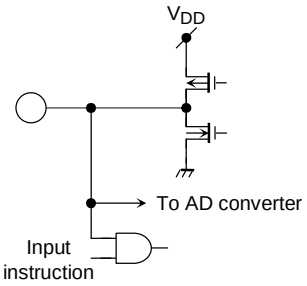
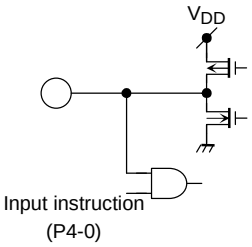
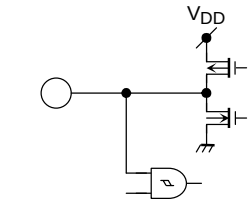
Pin Assignment

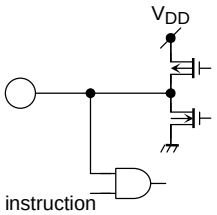
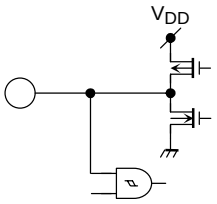
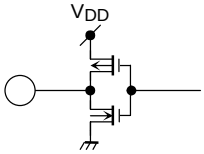
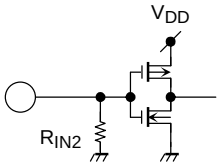


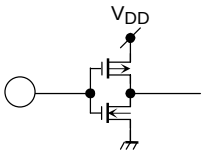
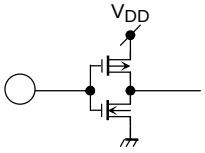
Block Diagram

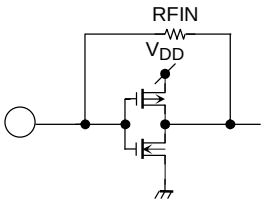
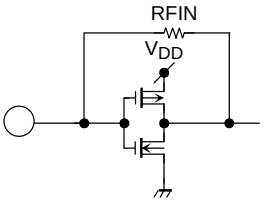
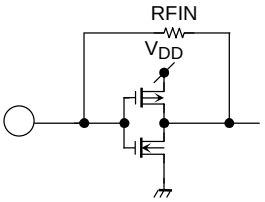
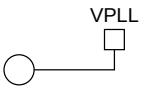


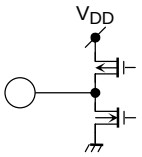
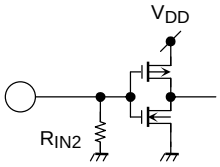
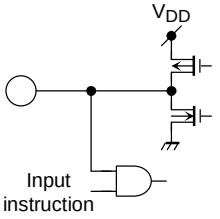
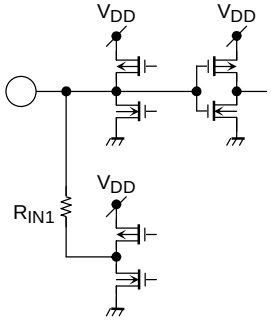
Pin No.	Symbol	Pin Name	Function and Operation	Remarks
1	OT1/COM1	Output port /LCD common output	Output ports. Pins OT1 to OT20 can be incremented by software, allowing easy data access to external RAM/ROM. Can be set to LCD driver output by software. At 1/4 duty, controller can display up to 136 segments using a matrix consisting of COM1 to 4 and SEG1 to 34. At 1/3 duty, can display up to 105 segments using a matrix consisting of COM1 to 3 and SEG1 to 35. At 1/2 duty, can display up to 72 segments using a matrix consisting of COM1 to 2 and SEG1 to 36. Set to output ports after a system reset or clock stop.	
2	OT2/COM2			
3	OT3/COM3 /S36	Output port /LCD common output /LCD segment output		
4	OT4/COM4 /S35			
5~30	OT5/S1 ~ OT30/S26	Output port /LCD segment output		
31~34	P9-0/S27 ~ P9-3/S30	I/O port 9 /LCD segment output	4-bit CMOS I/O ports. Input and output can be programmed in 1-bit units. These can be set bit by bit to LCD driver output by software. After a system reset, set to I/O port input. When a clock stop is executed, the pins used as the LCD driver must be set to output Low level (function as an I/O port).	
35~38	P10-0/S31 ~ P10-3/S34	I/O port 10 /LCD segment output		
40	$\overline{RESET}$ /V_{PP}	Reset input /Program voltage supply	Device's system reset signal input pin. Setting $\overline{RESET}$ to Low level triggers a reset. When the pin is set to High, the program starts from address 0. Since system reset will start if a voltage beyond 0 V to 3.5 V is supplied to V_{DD} pin, this pin is used by fixed at High level. This pin is used as program voltage supply for One Time PROM. In case of writing program into the internal PROM, 12.5 V is supplied to this pin.	
42~45	P1-0 ~ P1-3	I/O port 1	4-bit CMOS I/O port. Input and output can be programmed in 1-bit unit.	

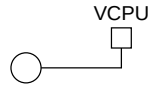
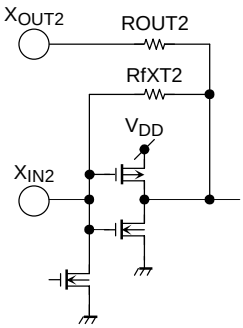
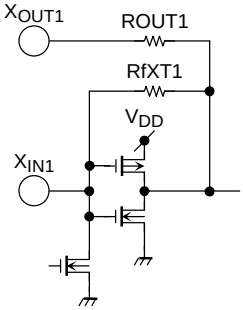
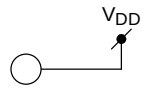
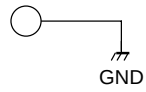
Pin No.	Symbol	Pin Name	Function and Operation	Remarks
46	DCREF	AD converter reference voltage input	AD converter reference voltage input pin. Normally apply V_{DD}.	
47~50	P2-0 /ADIN1 ~ P2-3 /ADIN4	I/O port 2 /A/D analog voltage input	4-bit CMOS I/O ports. Input and output can be programmed in 1-bit units. Pins P2-0 to P3-3 are also used for the built-in 8-bit, 8-channel AD converter analog input. The built-in AD converter uses a successive comparison system. When using a 4.5 MHz oscillator, the conversion clock can be selected from among 900 kHz, 100 kHz, and 50 kHz. When using a 75 kHz oscillator, the conversion clock is set to 75 kHz. The conversion times are respectively 23, 192, 382, and 294 μs. The necessary pins can be programmed to A/D analog input in 1-bit units. Voltage up to the V_{DD} can be input as the AD converter analog input voltage. Settings for the AD converter and its associated control can be performed by software.	
51~54	P3-0 /ADIN5 ~ P3-3 /ADIN8	I/O port 3 /A/D analog voltage input		
57	P4-0	I/O port 4	4-bit CMOS I/O ports. Input and output can be programmed in 1-bit units. Pins P4-1 to P4-3 also input/output the two serial interface circuits (SIO1, SIO2). On the clock edge of the SCK1 pin, SIO1 can input 4-bit or 8-bit serial data to pin SI1 or input/output data to pin SO1. For the serial operation clock (SCK1), an internal (SCK = 37.5 kHz) or external clock can be selected. This design facilitates LSI control and communication between controllers. Enabling the SIO1 interrupt jumps the program to address 4 when SIO1 execution is complete. On the falling edge of the SCK2 pin, SIO2 can input 26-bit serial data to the SI2 pin. SIO2 incorporates a data detector. Enabling the SIO2 interrupt triggers the interrupt on the falling edge of the SCK2 pin and jumps the program to address 6. The SIO1 and SIO2 inputs all incorporate Schmitt circuits. SIO1 and SIO2 and their associated controls can be operated and set by software.	
58	P4-1 /SI1 /SI2	Serial data input 1 /Serial data input 2		
59	P4-2 /SO1 /SO2	Serial data input/output 1 /Serial data input 2		
60	P4-3 /SCK1 /SCK2	Serial clock input/output 1 /Serial clock input 2		

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
61 62 63 64	P5-0/BUZR P5-1 /SI3 P5-2 /SO3 /SO4 P5-3 /SCK3 /SCK4	I/O port 5 /buzzer output /Serial data input 3 /Serial data input/output 3 /Serial data input/output 4 /Serial clock input/output 3 /Serial clock input/output 4	4-bit CMOS I/O ports. Input and output can be programmed in 1-bit unit. Pin 5-0 is also used to output a buzzer signal. Pins P5-1 to P5-3 are also used to input/output the two serial interface circuits (SIO3, SIO4). The buzzer output can be selected from eight frequency settings (0.625 to 3 kHz), which can be output in four modes: Continuous, Single-Shot, 10 Hz-Intermittent, and 10-Hz Intermittent at 1-Hz Intervals. SIO3 is a serial interface supporting three lines, while the SIO4 serial interface supports two lines. On the clock edge of the SCK3/SCK4 pin, SIO3/SIO4 can input 4- or 8-bit serial data to pin SI3 or output data to the SO3/SO4 pin. For the serial operating clock (SCK3/SCK4), an internal (450/225/150/75 kHz) clock or external clock can be selected. Rising and falling shift can also be selected. The clock data output is N-channel open drain. This design facilitates LSI control and communication between controllers. Enabling the SIO3 or SIO4 interrupts triggers the interrupt and jumps the program to address 3 when interface SIO3 or SIO4 completes execution. This is effective for high-speed serial communications. The SIO3 and SIO4 inputs all incorporate Schmitt circuits. SIO3, SIO4, and their associated controls can be used and set by software.	 Input instruction (P5-0)  Input instruction + SIOon (P5-1~P5-3)
65	MUTE	Muting output port	1-bit output port. Normally used as a muting control signal output. This pin can set the internal MUTE bit to 1 according to changes in the I/O port 8 input and $\overline{\text{HOLD}}$ input. The MUTE bit output logic can be changed.	
66	TEST	Test mode control input	Input pin for controlling Test mode. When the pins are at High level, the device is in Test mode; at Low level, in normal operation. Normally, set the pins to Low level or NC (pull-down resistors are incorporated).	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
67	$\overline{\text{HOLD}}$	Hold mode control input	Input pin for requesting and releasing Hold mode. Normally used to input radio mode selection or battery detection signals. Hold mode includes Clock Stop mode (crystal oscillator stopped) and Wait mode (CPU stopped), which can be set by the CKSTP and WAIT instructions respectively. Clock Stop mode can be entered by software in one of two ways: on command or when Low level is detected on the $\overline{\text{HOLD}}$ pin. Clock Stop mode can be released when High level is detected on the $\overline{\text{HOLD}}$ pin or when the input changes. Executing the CKSTP instruction stops the clock generator and CPU, entering memory backup mode. In this state the device is set to low current dissipation (10 μA max). Wait mode is executed, regardless of the $\overline{\text{HOLD}}$ pin input state, and the device is set to low current dissipation. To set wait mode, specify by software either crystal oscillator only operating or CPU suspended. Wait mode is released when the $\overline{\text{HOLD}}$ pin input changes.	
68 69	INTR1 INTR2 /PCTRin	External interrupt input /pulse count input	External interrupt input pins. Enabling the interrupt function and inputting a pulse (of at least 1.11 to 3.33 μs when the 4.5 MHz clock is in use, or at least 13.3 to 40 μs when the 75 kHz clock used) to these input pins generates an interrupt (INTR1/2) and jumps the program to address 1/2. The input logic and the clock edge (rising/falling) can be individually selected for each interrupt input. The internal 8-bit timer clock can be selected as input to the pins. At the pulse count or when the count reaches a specified value, an interrupt can be generated (to address 5). These pins are also used to input an 8-bit pulse counter. This counter can be selected from either rising and falling edge input, or an up-counter and a down-counter. These pins are Schmitt inputs and can also be used as input ports. The pins can also be utilized as ports for inputting remote control signals or tape counts.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
70 71	IF_{IN1}/IN1 IF_{IN2}/IN2	IF signal inputs /input port	IF signal input pins for the IF counter to count the IF signals of the FM and AM bands and detect the automatic stop position. The input frequency is in the range 0.3 to 20 MHz. A built-in input amp and capacitive coupling support low-amplitude operation. The IF counter is a 20-bit counter with selectable gate times of 1, 4, 16, and 64 ms. 20 bits of data can be easily stored in memory. In Manual mode, the gates can be switched on and off by instruction. These input pins can also be programmed as an input port (IN port). In this case, they become CMOS inputs and the clocks of those inputs can be counted using the IF counter. Note: Pins set as IF input go Low in PLL Off mode.	
73	FMIN	FM local oscillation signal input	Programmable counter input pins for the FM/AM band. Their input mode can be switched by software from either 1/2 + pulse swallow (VHF/FM) mode for FM input, or pulse swallow (HF) or direct division (LF) mode for AM input. The local oscillation output (voltage-controlled oscillator or V_{CO} output) is normally input at the following frequencies: 50 to 230 MHz in VHF mode, 50 to 140 MHz in FM1 mode, 10 to 60 MHz in FM2 mode, 1 to 30 MHz in HF mode, and 0.5 to 20 MHz in LF mode. A built-in input amp and capacitive coupling support low-amplitude operation. Note: In PLL Off mode or when the pins are not set for input, the input goes to high impedance.	
74	AMIN	AM local oscillation signal input		
75	VPLL	PLL constant voltage output	Constant voltage output for the PLL. The PLL constant voltage is used as the power supply for the PLL and IF counter. In PLL On mode, the constant voltage power supply is 3.55 V (typ.). In PLL Off mode, the V_{DD} is output. Connecting a capacitor (0.1 μF, 10 μF typ.) stabilizes the power supply.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
77 78	DO1 DO2/OUT	Phase comparator output /output port	PLL phase comparator output pins. In tri-state output, when the programmable counter divider output is higher than the reference frequency, the pins output High level; when the output is lower than the reference frequency, the pins output Low level. When the outputs match, the pins go to high impedance. Because DO1 and DO2 are output in parallel, optimal filter constants can be designed for both the AM and FM bands. The DO2 pin can be programmed to high impedance or set as an output port (OUT). Therefore, lockup time can be improved using the DO1 and DO2 pins or the pins can be effectively used as output ports. Lock-up time can also be improved by using DO1 and DO2 together by setting the pins to High-Speed Lock mode when using a 4.5 MHz oscillator. When the phase difference equals or exceeds ±1.11 μs, DO1 and DO2 output the phase difference pulse. When the phase difference is less than ±1.11 μs, the DO2 output goes to high impedance and only DO1 outputs the phase difference pulse.	
79	TEST2	Test mode control input 2	Input pin for controlling Test mode. When the pins are at High level, the device is in Test mode; at Low level, in normal operation. Normally, set the pins to Low level or NC (pull-down resistors are incorporated).	
80~83	P6-0 ι P6-3	I/O port 6	4-bit CMOS I/O ports. Input and output can be programmed in 1-bit units.	
84~87	P7-0 ι P7-3	I/O port 7		
88~91	P8-0 ι P8-3	I/O port 8	4-bit CMOS I/O port. Input and output can be programmed in 1-bit units. As the pins can be pulled up or pulled down by software they can be used as key input pins. When set to an I/O port input, that input can be varied to release Clock Stop or Wait modes or to set the MUTE bit of the MUTE pin to 1.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
92	VCPU	CPU constant voltage output	Constant voltage output pin for the CPU or oscillators. In normal mode, a constant voltage power supply of 2.95 V (typ.) is output; in Clock Stop mode, V_{DD} is output. Connecting a capacitor (0.1 μF, 10 μF typ.) stabilizes the power supply.	
94	X_{OUT2}	75 kHz crystal oscillator pins	Crystal oscillator pins. Connect a 4.5 MHz crystal (Ci = Co = 30 pF typ.) to X_{IN1} and X_{OUT1} and a 75 kHz crystal (Ci = Co = 30 pF typ.) to X_{IN2} and X_{OUT2}. Two different types of crystal resonators (4.5 MHz and 75 kHz) can be connected, or simply connect one (either 4.5 MHz or 75 kHz). Note that if a 75 kHz crystal only is connected, X_{IN1} must be fixed to GND level. If a 4.5 MHz crystal only is connected, it is not necessary to fix the 75 kHz crystal oscillator pins. If both 4.5 MHz and 75 kHz crystal oscillators are connected, after a reset the CPU operates on the 4.5 MHz crystal oscillator clock. The clock can be readily switched by software between the CPU operating clock and the peripheral clock. Oscillation stops during execution of the CKSTP instruction.	
95	X_{IN2}			
97	X_{OUT1}	4.5 MHz crystal oscillator pins		
98	XIN1			
100	V_{EE}	LCD driver bias voltage output pin	This is the bias voltage output pin for the LCD driver.	—
39 56 76 96	V_{DD1} V_{DD2} V_{DD3} V_{DD4}	Power supply pins	Pins used for supplying power. In PLL On mode, the pins supply V_{DD} = 4.0 to 5.5 V; in PLL Off mode, the pins supply V_{DD} = 3.5 to 5.5 V. In backup state (on execution of the CKSTP instruction), current dissipation becomes low (10 μA max), reducing the power supply voltage to 2.0 V. If 3.5 V or more is applied to these pins when the voltage is 0 V, a system reset is applied to the device and the program starts from address 0 (power-on reset). Note: To operate the power-on reset, allow 10 to 100 ms while the device power supply voltage rises.	
41 55 72 93 99	GND1 GND2 GND3 GND4 GND5			

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3~6.0	V
V_{PP} Power supply voltage	V_{PP}	−0.3~13.0	V
Input voltage 1	V_{IN1} (*)	−0.3~VCPU + 0.3	V
Input voltage 2	V_{IN2} (*)	−0.3~VPLL + 0.3	V
Input voltage 3	V_{IN3} (*)	−0.3~V_{DD} + 0.3	V
Power dissipation	P_D	400	mW
Operating temperature	T_{opr}	−40~85	°C
Storage temperature	T_{stg}	−65~150	°C

*: V_{IN1}: Includes X_{IN1}, X_{OUT1}, X_{IN2}, and X_{OUT2} pins
V_{IN2}: Includes AMin, FMin, IFin1, IFin2 (when IF input set) pins
V_{IN3}: Input pins, apart from V_{IN1} and V_{IN2}

Electrical Characteristics (unless otherwise specified, Ta = –40~85°C, V_{DD} = 3.5~5.5 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating power supply voltage range	V_{DD1}	—	When CPU operating	3.5	~	5.5	V
	V_{DD2}	—	When PLL operating	4.0	~	5.5	
Memory hold voltage range	VHD	—	Crystal oscillation stopped (CKSTP instruction executed)	2.0	~	5.5	V
Operating power supply current	I_{DD1}	—	When PLL operating (VHF mode) and at FMin = 230 MHz input, Ta = 25°C	—	3	5	mA
	I_{DD2}	—	When CPU only operating (4.5-MHz clock operating, 75-kHz oscillation stopped, PLL off, display lit), Ta = 25°C	—	1.0	1.5	
	I_{DD3}	—	When CPU only operating (75-kHz clock operating, 4.5-MHz oscillation stopped, PLL off, display lit), Ta = 25°C	—	0.3	0.5	
	I_{DD4}	—	In Hard Wait mode (4.5-MHz crystal only operating), Ta = 25°C	—	200	—	μA
	I_{DD5}	—	In Hard Wait mode (75-kHz crystal only operating), Ta = 25°C	—	70	—	
	I_{DD6}	—	When soft wait executed (PLL off, CPU operating intermittently on 4.5-MHz clock, display lit), Ta = 25°C	—	350	—	
	I_{DD7}	—	When soft wait executed (PLL off, CPU operating intermittently on 75-kHz clock, display lit), Ta = 25°C	—	250	—	
Memory hold current	IHD	—	Crystal oscillator stopped (CKSTP instruction executed)	—	0.1	10	μA
Crystal oscillator frequency	fXT1	—	Crystal oscillator 1 (X_{IN1}, X_{OUT1})	—	4.5	—	MHz
	fXT2	—	Crystal oscillator 2 (X_{IN2}, X_{OUT2})	—	75	—	kHz
Crystal oscillation startup time	tst	—	Crystal oscillator fXT2 = 75 kHz (X_{IN2}, X_{OUT2})	—	—	1.0	s
Constant voltage power supply voltage for CPU	VCPU	—	GND reference (VCPU)	2.65	2.95	3.25	V
Constant voltage power supply voltage for PLL	VPLL	—	GND reference (VPLL), V_{DD} = 4.0 to 5.5 V	3.15	3.55	3.95	V
Low voltage detection voltage	VSTOP	—	(VCPU), STOP F/F bit detected	2.15	2.40	2.65	V

Programmable Counter and IF Counter Operating Frequency Ranges

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
FMin (VHF mode)	fVHF	—	V_{IN} = 0.2 V_{p-p}, V_{DD} = 4.0~5.5 V	50	~	230	MHz
FMin (FM mode)	fFM1	—	V_{IN} = 0.1 V_{p-p}, V_{DD} = 4.0~5.5 V	50	~	140	
	fFM2	—	V_{IN} = 0.1 V_{p-p}, V_{DD} = 4.0~5.5 V	10	~	60	
AMin (HF mode)	fHF	—	V_{IN} = 0.1 V_{p-p}, V_{DD} = 4.0~5.5 V	1.0	~	30	
AMin (LF mode)	fLF	—	V_{IN} = 0.1 V_{p-p}, V_{DD} = 4.0~5.5 V	0.5	~	20	
IFIN1, IFIN2	fIF	—	V_{IN} = 0.1 V_{p-p}, V_{DD} = 4.0~5.5 V	0.3	~	20	

Programmable Counter and IF Counter Input Oscillation Ranges

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
FMin (VHF mode)	VVHF	—	fVHF, V_{DD} = 4.0~5.5 V	0.2	~	1.0	V_{p-p}
FMin (FM mode)	VFM	—	fFM1/fFM2, V_{DD} = 4.0~5.5 V	0.1	~	1.0	
AMin (HF mode)	VHF	—	fHF, V_{DD} = 4.0~5.5 V	0.1	~	1.0	
AMin (LF mode)	VLF	—	fLF, V_{DD} = 4.0~5.5 V	0.1	~	1.0	
IFIN1, IFIN2	VIF	—	fIF, V_{DD} = 4.0~5.5 V	0.1	~	1.0	

LCD Common Outputs/Segment Outputs (COM~COM4, S1~S22)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Bias output voltage	GND level	VBS1	—	V_{DD} = 5 V, no load	—	0.00	0.15	V
	1/3 V_{DD} level	VBS2	—	V_{DD} = 5 V, no load	1.52	1.67	1.82	
	1/2 V_{DD} level	VBS3	—	V_{DD} = 5 V, no load	2.35	2.50	2.65	
	2/3 V_{DD} level	VBS4	—	V_{DD} = 5 V, no load	3.18	3.33	3.48	
	V_{DD} level	VBS5	—	V_{DD} = 5 V, no load	4.85	5.00	—	

Output Ports and I/O Ports (OT1~OT30, P1-0~P10-3)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	High level	IOH1	—	V_{DD} = 5 V, V_{OH} = V_{DD} − 0.5 V	−1.00	−2.50	—	mA
	Low level	IOL1	—	V_{DD} = 5 V, V_{OL} = 0.5 V, except for P5-1 to P5-3	1.00	2.50	—	
		IOL2	—	V_{DD} = 5 V, V_{OL} = 0.5V, P5-1~P5-3	4.00	10.00	—	
Input leakage current		ILI	—	V_{IH} = VDD, V_{IL} = 0V (P1-0~P10-3)	—	—	±1.0	μA
Input voltage	High level	V_{IH}	—	(P1-0~P10-3)	V_{DD} × 0.8	~	V_{DD}	V
	Low level	V_{IL}	—	(P1-0~P10-3)	0	~	V_{DD} × 0.2	
Input pulled-up/down resistor		RIN1	—	When P8-0 to P8-3 pulled up/down	15	60	250	kΩ

MUTE, DO1, DO2 Output

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	High level	IOH1	—	V_{DD} = 5 V, V_{OH} = V_{DD} − 0.5 V	−1.25	−2.50	—	mA
	Low level	IOL1	—	V_{DD} = 5 V, V_{OL} = 0.5 V	1.25	2.50	—	
Output off leakage current		ITL	—	V_{DD} = 5 V, VTLH = 5 V, VTLL = 0 V (DO1, DO2)	—	—	±100	nA

$\overline{\text{HOLD}}$, INTR1/2, IN1/2 Input Ports, $\overline{\text{RESET}}$ Input

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input leakage current		ILI	—	V_{IH} = V_{DD}, V_{IL} = 0 V	—	—	±1.0	μA
Output current	High level	V_{IH}	—	—	V_{DD} × 0.8	~	V_{DD}	V
	Low level	V_{IL}	—	—	0	~	V_{DD} × 0.2	

AD Converter (ADIN1~ADIN8, DCREF)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analog input voltage range	VAD	—	ADin1~ADin8	0	~	V_{DD}	V
Resolution	VRES	—	—	—	8	—	bit
Linear error	—	—	—	—	±0.5	±1.0	LSB
Conversion total error	—	—	V_{DD} = 5 V, DCREF = 5 V	—	±3.0	±8.0	
Analog input leakage	ILI	—	V_{DD} = 5V, V_{IH} = 5V, V_{IL} = 0 V (ADin1~ADin8)	—	—	±1.0	μA
Reference voltage input current	IREF	—	V_{DD} = 5V, DCREF = 5 V (DCREF)	—	0.5	1.0	mA

Crystal Oscillators

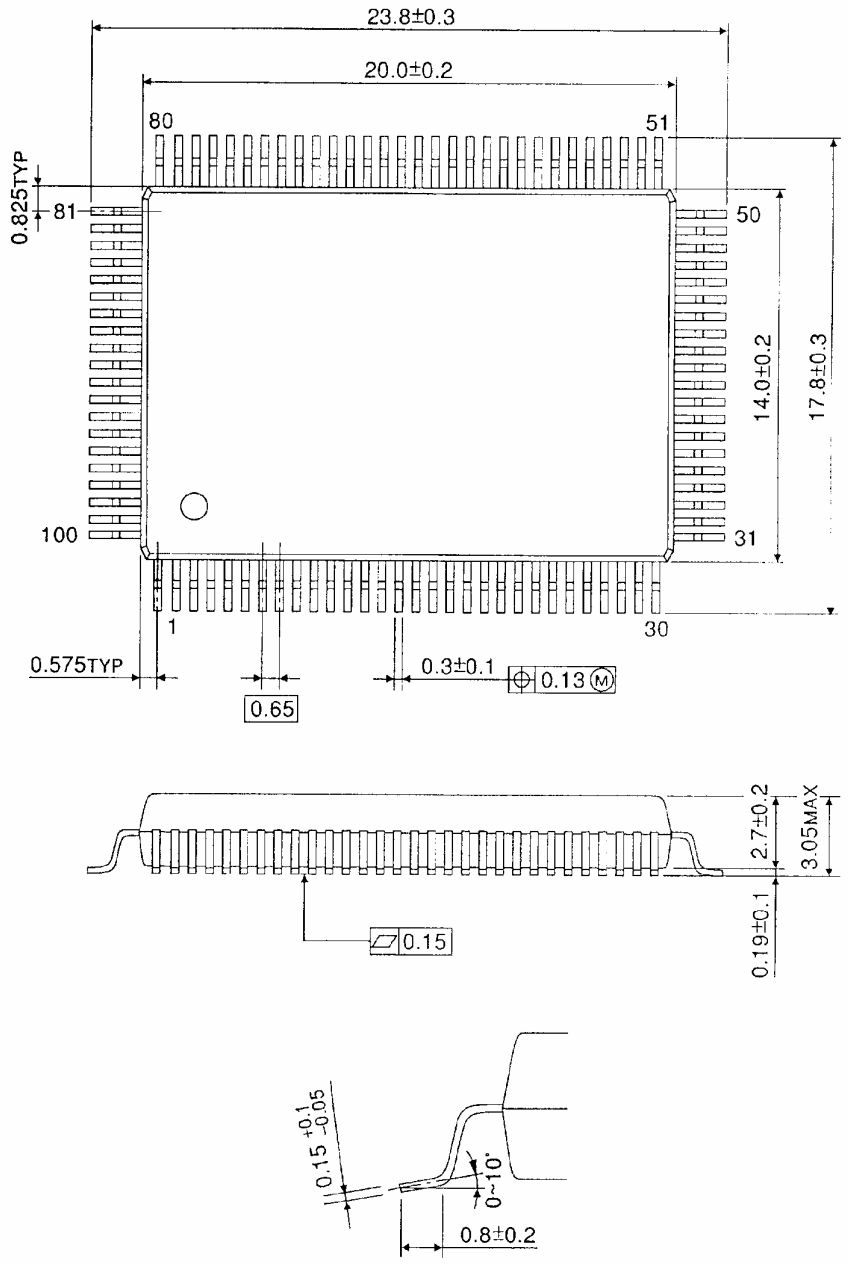
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
X_{IN1} amp feedback resistance	RfXT1	—	(X_{IN1}–X_{OUT1})	0.35	1.0	3.00	MΩ
X_{IN2} amp feedback resistance	RfXT2	—	(X_{IN2}–X_{OUT2})	3.5	10	30.0	
X_{OUT1} output resistance	ROUT1	—	(X_{OUT1})	1.2	3.0	10.0	kΩ
X_{OUT2} output resistance	ROUT2	—	(X_{OUT2})	1.5	4.0	15.0	

Others

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input pulled-down resistance	RIN2	—	(TEST)	15.0	60	250	kΩ
Input amp feedback resistance	RfIN	—	VPLL = 3.5 V (FMin, AMin, IFin1, IFin2)	350	800	3500	

Package Dimensions

QFP100-P-1420-0.65Q Unit : mm



Weight: 1.6 g (typ.)
Note: Lead type PD-Pff

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