KINGMAX™

MPMB62D-68KX3   PC-2700 CL2.5 184pin DDR DIMM
32Mx64 DDR DIMM based on 16Mx8 DDR SDRAMs with SPD

DESCRIPTION

The MPMB62D-68KX3 is 32M bit x 64 Double Data Rate Synchronous Dynamic RAM high density memory module based on 128Mb DDR SDRAM respectively.

The MPMB62D-68KX3 consists of sixteen CMOS 16M $\times$ 8 bit with 4 banks Double Data Rate Synchronous DRAMs in TinyBGA package and a 2K EEPROM in 8-Pin TSSOP package mounted on a 184pin glass-epoxy substrate. Two 0.1μF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM.

The MPMB62D-68KX3 is a Dual In-line Memory Module and is intended for mounting into 184pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of every clock cycle. Range of operating frequencies, programmable latencies and burst lengths allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURES

- Performance range - 166MHz (DDR333, CL2.5)
- Double-data-rate architecture; two data transfers per clock cycle
- Bi-directional data strobe (DQS)
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transition with CK transition
- Auto & self refresh capability (4096 Cycles / 64ms)
- Single 2.5V ±0.2V power supply
- Programmable Read latency 2, 2.5 (clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (Sequential & Interleave)
- Edge aligned data output, center aligned data input
- Serial presence detect with EEPROM
- PCB : Height (1,181 mil), double sided component

PIN CONFIGURATIONS (Front side/Back side)

Pin	Front	Pin	Front	Pin	Back	Pin	Back
1	VREF	47	*DOS8	93	VSS	139	VSS
2	DQ0	48	A0	94	DQ4	140	*DM8
3	VSS	49	*CB2	95	DQ5	141	A10
4	DQ1	50	VSS	96	VDDQ	142	*CB6
5	DQS0	51	*CB3	97	DM0	143	VDDQ
6	DQ2	52	BA1	98	DQ6	144	*CB7
7	VDD	53	DQ32	99	DQ7	145	VSS
8	DQ3	54	VDDQ	100	VSS	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	VDD
11	VSS	57	DQ34	103	*A13	149	DM4
12	DQ8	58	VSS	104	VDDQ	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	VSS
15	VDDQ	61	DQ40	107	DM1	153	DQ44
16	CK1	62	VDDQ	108	VDD	154	/RAS
17	/CK1	63	/ME	109	DQ14	155	DQ45
18	VSS	64	DQ41	110	DQ15	156	CDDQ
19	DQ10	65	/CAS	111	CKE1	157	/CS0
20	DQ11	66	VSS	112	CDDQ	158	/CS1
21	CKE0	67	DQS5	113	*BA2	159	DM5
22	VDDQ	68	DQ42	114	DQ20	160	VSS
23	DQ16	69	DQ43	115	*A12	161	DQ46
24	DO17	70	VDD	116	VSS	162	DO47
25	DQS2	71	NC	117	DQ21	163	NC
26	VSS	72	DQ48	118	A11	164	VDDQ
27	A9	73	DQ49	119	DM2	165	DQ52
28	DQ18	74	VSS	120	VDD	166	DQ53
29	A7	75	/CK2	121	DQ22	167	NC
30	VDDQ	76	CK2	122	A8	168	VDD
31	DQ19	77	VDDQ	123	DQ23	169	DM6
32	A5	78	DQS6	124	VSS	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	VSS	80	DQ51	126	DQ28	172	VDDQ
35	DQ25	81	VSS	127	DQ29	173	NC
36	DQS3	82	VDDID	128	VDDQ	174	DQ60
37	A4	83	DQ56	129	DM3	175	DQ61
38	VDD	84	DQ57	130	A3	176	VSS
39	DQ26	85	VDD	131	DQ30	177	DM7
40	DQ27	86	DQS7	132	VSS	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	VSS	88	DQ59	134	*CB4	180	VDDQ
43	A1	89	VSS	135	*CB5	181	SA0
44	*CB0	90	WP	136	VDDQ	182	SA1
45	*CB1	91	SDA	137	CK0	183	SA2
46	VDD	92	SCL	138	/CK0	184	VDDSPD

PIN NAME

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 , BA1	Select bank Address
DQ0 ~ DQ63	Data input/output
DQS0 ~ DQS7	Data Strobe input/output
CK0 ~ CK2	Clock input
/CK0 ~ /CK2	Clock input
CKE0 , CKE1	Clock enable input
/CS0 , /CS1	Chip select input
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write enable
DM0 ~ DM7	Data-in mask
VDD	Power supply (2.5V)
VDDQ	Power supply for DQS (2.5V)
VSS	Ground
VREF	Power supply for reference
VDDSPD	Serial EEPROM power supply (2.5V~6V)
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ SA2	Address in EEPROM
VDDID	VDD identification flag
NC	No connection

* These pins are not used in this module.

FUNCTIONAL BLOCK DIAGRAM
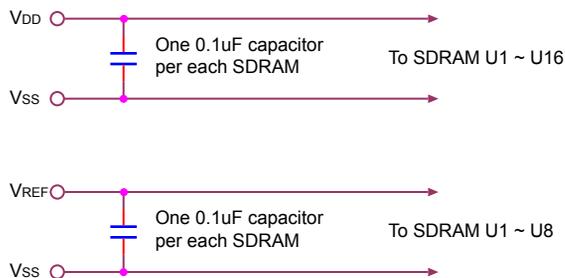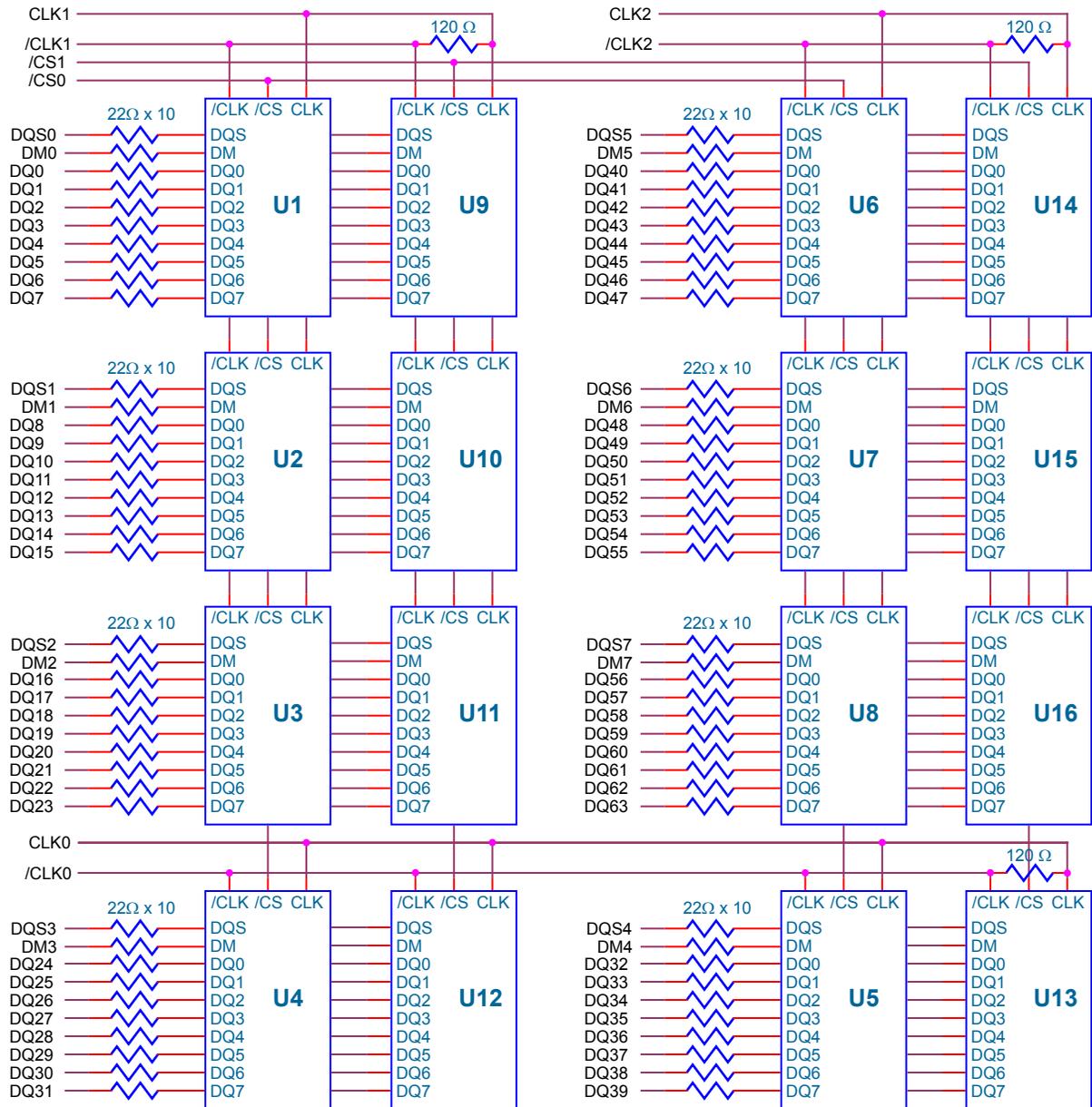
A0 ~ A11,BA0,BA1 → SDRAM U1 ~ U16
/RAS, /CAS, /WE → SDRAM U1 ~ U16
CKE0 → SDRAM U1 ~ U8
CKE1 → SDRAM U9 ~ U16

V_DD — One 0.1uF capacitor per each SDRAM — To SDRAM U1 ~ U16
V_SS

V_REF — One 0.1uF capacitor per each SDRAM — To SDRAM U1 ~ U8
V_SS

V_DDSPD
Serial PD
VDD SCL — SCL
WP SDA — SDA
A0 A1 A2
SA0 SA1 SA2
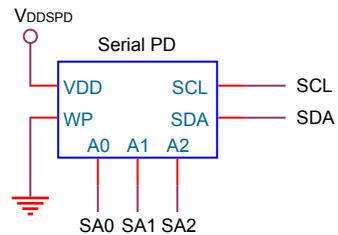
ABSOLUTE MAXIMUM RATIINGS

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{DD}	-1.0 ~ 3.6	V
I/O pins voltage relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Operating temperature	T_A	0 ~ +70	°C
Storage temperature	T_{STG}	-55 ~ +125	°C
Power dissipation	P_D	16	W

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RANTINGS" are exceeded. Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTIICS (SSTL_2 In/Out)

Recommended operating conditions (T_A = 0 to 70°C, V_{DD} = +2.5V ±0.2V)

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage	V_{DD}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	$0.49 \times V_{DD}$	$0.51 \times V_{DD}$	V	1
I/O Termination voltage (system)	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	$V_{IH(DC)}$	V_{REF}+0.15	V_{DD}+0.3	V	3
Input logic low voltage	$V_{IL(DC)}$	-0.3	V_{REF}-0.15	V	3
Input voltage level, CK and /CK inputs	$V_{IN(DC)}$	-0.3	V_{DD}+0.3	V	
Input differential voltage, CK and /CK inputs	$V_{ID(DC)}$	0.3	V_{DD}+0.6	V	4
Output high current (V_{OUT} = 1.95V)	I_{OH}	16.8	-	mA	
Output low current (V_{OUT} = 0.35V)	I_{OL}	-16.8	-	mA	
Input leakage current	I_I	-16	16	µA	5
Output leakage current	I_{OZ}	-40	40	µA	6

Note : 1. V_{REF} is expected to be equal to $0.5 \times V_{DD}$ of the transmitting devices, and must track variations in the DC level of the same. Peak-to-peak noise on V_{REF}, may not exceed 2% of the DC value.

2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.

3. These parameters should be tested at the pin on actual components. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHz.

4. V_{ID} is the magnitude of the difference between the input level on CK and the input on /CK.

5. Any input $0V \leq V_{IN} \leq V_{DD}$, V_{REF} pin $0V \leq V_{IN} \leq 1.35V$, All other pins not under test = 0 V

6. $0V \leq V_{OUT} \leq V_{DD}$, DQs are disabled.

I_{DD} CONDITIONS AND SPECIFICATIONS

Recommended operating conditions unless otherwise noted, T_A = 0 to 70°C, V_{DD} = +2.5V ±0.2V

| Parameter / Condition	Symbol	Max	Unit	Note
Operating current - One bank; Active-Precharge; tRC = tRC(Min); tCK = tCK(Min); DQ, DM and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle	I_{DD0}	1080	mA	
Operating current - One bank; Active-Read-Precharge; Burst = 2; tRC = tRC(Min); tCK = tCK(Min); I_{OUT} = 0 mA; Address and control inputs changing once per clock cycle	I_{DD1}	1520	mA	
Precharge power-down standby current; All banks idle; Power-down Mode; tCK = tCK(Min); CKE = LOW	I_{DD2P}	520	mA	
Idle standby current; /CS = HIGH; All banks idle; tCK = tCK(Min); CKE = HIGH; Address and control inputs changing once per clock cycle; V_{IN} = V_{REF} for DQ, DQS and DM	I_{DD2F}	680	mA	
Active power-down standby current; One banks active; Power-down Mode; tCK = tCK(Min); CKE = LOW	I_{DD3P}	560	mA	
Active standby current; /CS = HIGH; CKE = HIGH; One bank; Active-Precharge; tRC = tRAS(Max); tCK = tCK(Min) ; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once pre clock cycles	I_{DD3N}	680	mA	
Operating current; Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK = tCK(Min); I_{OUT} = 0 mA	I_{DD4R}	1640	mA	
Operating current; Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK = tCK(Min); DQ, DM and DQS inputs changing twice per clock cycle	I_{DD4W}	1520	mA	
Auto refresh current; tRC = tRC(Min); distributed refresh	I_{DD5}	1960	mA	
Self refresh current; CKE ≤ 0.2V; External clock should be on	I_{DD6}	80	mA	
Operating current; Four bank interleaving READs with BL = 4; Auto Precharge; tRC = tRC(min); tCK = tCK(min); Address and control inputs change only Active READ or WRITE commands	I_{DD7}	2560	mA	

AC INPUT OPERATING CONDITIONS

Recommended operating conditions (T_A = 0 to 70°C, V_{DD} = +2.5V ±0.2V)

Parameter / Condition	Symbol	Min	Max	Unit	Note
Input logic high voltage	$V_{IH(AC)}$	V_{REF}+0.31	-	V	1
Input logic low voltage	$V_{IL(AC)}$	-	V_{REF}-0.31	V	1
Input differential voltage, CK and /CK inputs	$V_{ID(DC)}$	0.7	V_{DD}+0.6	V	2
Input crossing point voltage, CK and /CK inputs	$V_{IX(DC)}$	$0.5 \times V_{DD}$-0.2	$0.5 \times V_{DD}$+0.2	V	3

Note : 1. These parameters should be tested at the pin on actual components. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHz.

2. V_{ID} is the magnitude of the difference between the input level on CK and the input on /CK.

3. The value of V_{IX} is expected to be equal $0.5 \times V_{DD}$ of the transmitting device and must track variations in the DC level of the same.

AC OPERATING TEST CONDITIONS (T_A = 0 to 70°C, V_{DD} = +2.5V ±0.2V)

Parameter	Value	Unit
Input reference voltage for Clock	$0.5 \times V_{DD}$	V
Input signal maximum peak swing	1.5	V
Input signal minimum slew rate	1.0	V
Input Levels(V_{IH}/V_{IL})	V_{REF}+0.31 / V_{REF}-0.31	V
Input timing measurement reference level	V_{REF}	V
Output timing measurement reference level	Vtt	V
Output load condition	See Load Circuit	
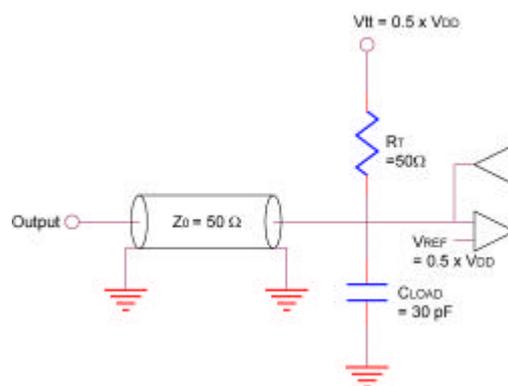
Output Load Circuit (SSTL_2)

AC TIMMING PARAMETERS AND SPECIFICATIONS

(These AC characteristics were tested on the component)

Parameter		Symbol	Min	Max	Unit	Note
Row cycle time		tRC	60	-	ns	
Refresh row cycle time		tRFC	72	-	ns	
Row active time		tRAS	42	70K	ns	
/RAS to /CAS delay		tRCD	18		ns	
Row precharge time		tRP	18		ns	5
Row active to Row active delay		tRRD	12		ns	5
Write recovery time		tWR	2.5		tCK	
Last data in to Read command		tCDLR	1		tCK	
Col. address to Col. address delay		tCCD	1		tCK	
Clock cycle time	CL = 2.0	tCK	7.5	12	ns	5
	CL = 2.5		6.0	12		
Clock high level width		tCH	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	tCK	
DQS-out access time from CK, /CK		tDQSCK	-0.6	+0.6	ns	
Output data access time from CK, /CK		tAC	-0.7	+0.7	ns	
Data strobe edge to output data edge		tDQSQ	-	+0.35	ns	
Read Preamble		tRPRE	0.9	1.1	tCK	
Read Post amble		tRPST	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		ns	2
DQS-in hold time		tWPREH	0.25		tCK	
DQS falling edge to CK rising-setup time		tDSS	0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		tCK	
DQS-in high level width		tDQSH	0.35		tCK	
DQS-in low level width		tDQSL	0.35		tCK	
DQS-in cycle time		tDSC	0.9	1.1	tCK	
Address and Control Input setup time		tIS	0.75		ns	6
Address and Control Input hold time		tIH	0.75		ns	6
Data-out high impedance time from CK, /CK		tHZ	tACmin - 400ps	tACmax - 400ps	ps	
Data-out low impedance time from CK, /CK		tLZ	tACmin - 400ps	tACmax - 400ps	ps	
Input Slew Rate (for input only pins)		tSL(I)	0.5		V/ns	6
Input Slew Rate (for I/O pins)		tSL(IO)	0.5		V/ns	7
Output Slew Rate (x8)		tSL(O)	1.0	4.5	V/ns	10
Output Slew Rate Matching Ratio (rise to fall)		tSLMR	0.67	1.5		

Parameter	Symbol	Min	Max	Unit	Note
Mode register set cycle time	tMRD	12		ns	
DQ & DM setup time to DQS	tDS	0.45		ns	7,8,9
DQ & DM hold time to DQS	tDH	0.45		ns	7,8,9
DQ & DM input pulse width	tDIPW	1.75		ns	
Power down exit time	tPDEX	10		ns	
Exit self refresh to write command	tXSW	95		ns	
Exit self refresh to bank active command	tXSA	75		ns	4
Exit self refresh to read command	tXSR	200		Cycle	
Refresh interval time	tREF	15.6		us	1
Output DQS valid window	tQH	tHPmin - tQHS		ns	5
Clock half period	tHP	tCLmin or tCHmin		ns	
Data hold skew factor	tQHS		0.5	ns	
DQS write post amble time	tWPST	0.4	0.6	tCK	3

Note : 1. Maximum burst refresh of 8

2. The specific requirement is that DQS be valid (High or Low) on or before this CK edge. The case shown (DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.

3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.

4. A write command can be applied with tRCD satisfied after this command.

5. For registered DINNs, tCL and tCH are ≥ 45% of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to cross talk (tJIT(crosstalk)) on the DIMM.

6. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate (V/ns)	ΔtIS (ps)	ΔtIH (ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase tIS /tIH in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate (V/ns)	ΔtIS (ps)	ΔTih (ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase tDS /tDH in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

8. I/O Setup/Hold Plateau Derating

I/O Input Level (mV)	ΔtIS (ps)	ΔtIH (ps)
±280	+50	+50

This derating table is used to increase tDS /tDH in the case where the input level is flat below VREF ± 310mV for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate (ns/V)	ΔtIS (ps)	ΔtIH (ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

This derating table is used to increase tDS/tDH in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is collated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 5V/ns and slew rate 2 =.4V/ns then the Delta Rise/Fall Rate =0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is fir system simulation purpose. It is guaranteed by design.

Input/Output CAPACITANCE

(V_{DD} = 2.5V, T_A = 25°C, f = 1MHz, V_{REF} = 1.25V ±100mV)

Pin	Symbol	Min	Max	Unit
Input Capacitance: Command and Address	C_{IN1}	65	81	pF
Input Capacitance: /CS0, /CS1	C_{IN2}	42	50	pF
Input Capacitance: CK0, /CK0, CK1, /CK1	C_{IN3}	42	50	pF
Input Capacitance: CKE0, CKE1	C_{IN4}	27	34	pF
Input/Output Capacitance: DQs, DQS	$C_{I/O}$	10	13	pF

COMMAND TRUTH TABLE

Command			CKE_{n-1}	CKE_n	/CS	/RAS	/CAS	/WE	$BA_{0,1}$	A_{10}/AP	A_{11},A_9~A_0	Note
Register	Extended MRS		H	X	L	L	L	L	OP code			1, 2
Register	Mode Register Set		H	X	L	L	L	L	OP code			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Address			H	X	L	L	H	H	V	Row address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column address (A_0~A_9)	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column address (A_0~A_9)	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down	Entry		H	L	H	X	X	X	X			
					L	V	V	V				
	Exit		L	H	X	X	X	X	X			
Precharge Power Down Mode	Entry		H	L	H	X	X	X	X			
					L	H	H	H				
	Exit		L	H	H	X	X	X	X			
					L	V	V	V				
DM			H			X			X			8
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

(V = Valid, X = Don't Care, H = Logic High, L = Logic Low)

Note : 1. OP Code : Operand Code. A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@EMRS/MRS)

    2. EMRS/ MRS can be issued only at all banks precharge state.

      A new command can be issued 2 clock cycles after EMRS or MRS.

    3. Auto refresh functions are same as the CBR refresh of DRAM.

      The automatically precharge without row precharge command is meant by "Auto".

      Auto/self refresh can be issued only at all banks precharge state.

    4. BA_0 ~ BA_1 : Bank select addresses.

      If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.

      If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.

      If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.

      If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.

    5. If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and all banks are selected.

    6. During burst write with auto precharge, new read/write command can not be issued.

      Another bank read/write command can be issued after the end of burst.

      New row active of the associated bank can be issued at tRP after the end of burst.

    7. Burst stop command is valid at every burst length.

    8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).

    9. This combination is not defined for any function, which means "No Operation (NOP)" in DDR SDRAM.

PACKAGE DIMENSIONS

Units: Millimeter
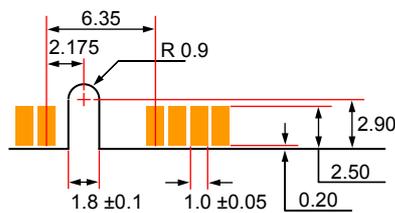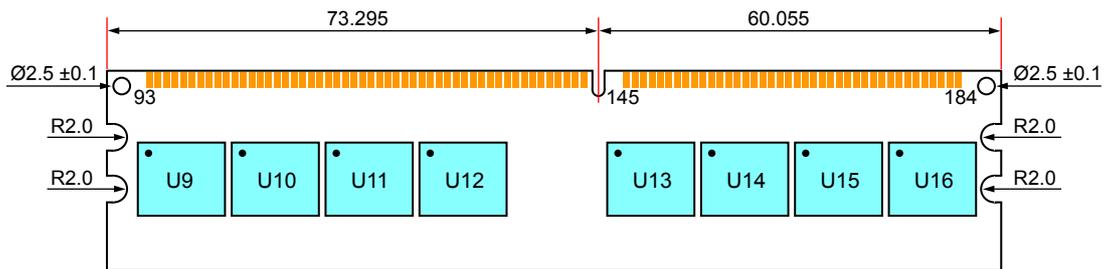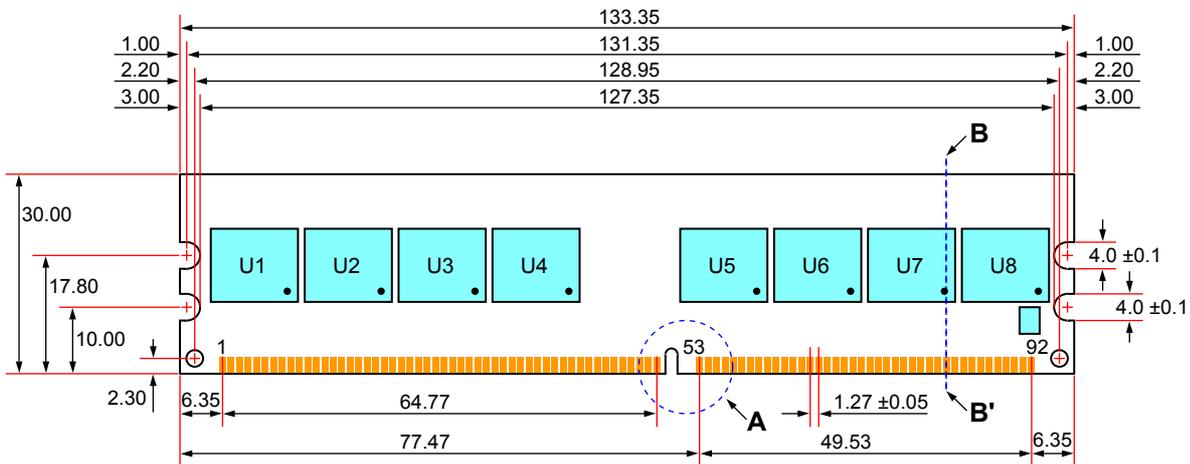
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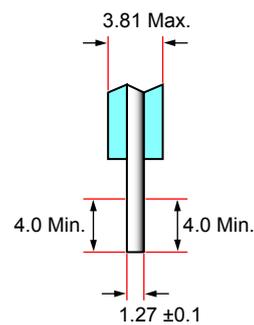
Section B-B'

Tolerance : ±0.15 unless otherwise specified

The used device is 16Mx8 SDRAM TinyBGA

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h
1	Total # of bytes of SPD memory device	256 bytes (2K-bit)	08h
2	Fundamental memory type	SDRAM DDR	07h
3	# of row address on this assembly	12	0Ch
4	# of column address on this assembly	10	0Ah
5	# of module Rows on this assembly	2 Rows	02h
6	Data width of this assembly	64 bits	40h
7	Data width of this assembly	-	00h
8	VDDQ and interface standard of this assembly	SSTL 2.5V	04h
9	DDR SDRAM cycle time from clock @CAS latency of 2.5	6.0ns	60h
10	DDR SDRAM access time from clock @CAS latency of 2.5	± 0.7ns	70h
11	DIMM configuration type (Non-parity , Parity , ECC)	Non-parity , ECC	00h
12	Refresh rate & type	15.6us, support self refresh	80h
13	Primary DDR SDRAM width	× 8	08h
14	Error checking DDR SDRAM data width	N/A	00h
15	Minimum clock delay for back-to-back random column	tCCD=1CLK	01h
16	DDR SDRAM device attributes: Burst lengths supported	2 , 4 , 8	0Eh
17	DDR SDRAM device attributes: # of banks on each DDR	4 banks	04h
18	DDR SDRAM device attributes: CAS Latency supported	2 &2.5	0Ch
19	DDR SDRAM device attributes: CS Latency	0 CLK	01h
20	DDR SDRAM device attributes: WE Latency	1 CLK	02h
21	DDR SDRAM module attributes	Registered address & Control inputs and On-card DLL	20h
22	DDR SDRAM device attributes: General	+/- 0.2 voltage tolerance	00h
23	DDR SDRAM cycle time @CAS latency of 2	7.5ns	75h
24	DDR SDRAM access time @CAS latency of 2	± 0.7ns	70h
25	SDRAM cycle time @CAS latency of 1.5	-	00h
26	SDRAM access time @CAS latency of 1.5	-	00h
27	Minimum row precharge time (=tRP)	18ns	48h
28	Minimum row active to row active delay (tRRD)	12ns	30h
29	Minimum RAS to CAS delay (=tRCD)	18ns	48h
30	Minimum activate precharge time (=tRAS)	42ns	2Ah
31	Module Row density	128MB	20h
32	Command and Address signal input setup time	0.75ns	75h
33	Command and Address signal input hold time	0.75ns	75h
34	Data signal input setup time	0.45ns	45h
35	Data signal input hold time	0.45ns	45h
36~61	Superset information (maybe used in future)	-	00h
62	SPD data revision code	Initial release	00h
63	Checksum for bytes 0 ~ 62		E8h

SERIAL PRESENCE DETECT INFORMATION

64	Manufacturer JEDEC ID code	kingmax	7Fh
65	Manufacturer JEDEC ID code	kingmax	7Fh
66	Manufacturer JEDEC ID code	kingmax	7Fh
67	Manufacturer JEDEC ID code	kingmax	25h
68~71	Manufacturer JEDEC ID code	-	00h
72	Manufacturing location	Hsin Chu (A)	41h
73	Manufacturer part # (Memory module)	M	4Dh
74	Manufacturer part # (184 pin DIMM)	P	50h
75	Manufacturer part # (DDR 333)	M	4Dh
76	Manufacturer part # (Module density: 256MB)	B	42h
77	Manufacturer part # (Module density: 256MB)	6	36h
78	Manufacturer part # (Vdd = 2.5V)	2	32h
79	Manufacturer part # (DDR SDRAM)	D	44h
80	Manufacturer part #	"-"	2Dh
81	Manufacturer part # (DDR SDRAM type: 16Mb × 8)	6	36h
82	Manufacturer part # (DDR SDRAM type: 16Mb × 8)	8	38h
83	Manufacturer part # (Kingmax logo)	K	4Bh
84	Manufacturer part # (Kingmax logo)	X	58h
85	Manufacturer part # (CL=2.5)	3	33h
86	Manufacturer part #	"-"	2Dh
87	Manufacturer part # (option for die source)	*	*
88	Manufacturer part # (option for module version)	*	*
89	Manufacturer part # (option for die version)	*	*
90	Manufacturer part # (reserve)	-	00h
91	Manufacturer revision code (reserve)	-	00h
92	Manufacturer revision code (reserve)	-	00h
93	Manufacturing date (Work Year) - BCD	2002	02h
94	Manufacturing date (Work Week) - BCD (reserve)	-	00h
95~98	Assemble serial # -BCD (reserve)	-	00h
99~125	Manufacturer specific data (may be used in future)	-	00h
126	Intel specification for frequency	Undefined	00h
127	Intel specification details for 100MHz support	Undefined	00h
128+	Unused storage locations	-	FFh