

## FDB8860

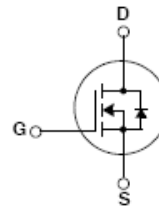
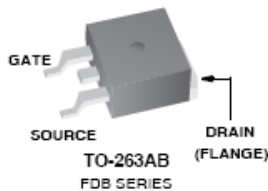
### N-Channel Logic Level PowerTrench® MOSFET 30V, 80A, 2.6mΩ

#### Features

- $R_{DS(ON)} = 1.9m\Omega$  (Typ),  $V_{GS} = 5V$ ,  $I_D = 80A$
- $Q_{g(5)} = 89nC$  (Typ),  $V_{GS} = 5V$
- Low Miller Charge
- Low  $Q_{RR}$  Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- Qualified to AEC Q101
- RoHS Compliant

#### Applications

- 12V Automotive Load Control
- Start / Alternator Systems
- Electronic Power Steering Systems
- ABS
- DC-DC Converters



## MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current Continuous ( $V_{GS} = 10\text{V}$ , $T_C < 163^\circ\text{C}$ )	80	A
	Continuous ( $V_{GS} = 5\text{V}$ , $T_C < 162^\circ\text{C}$ )	80	A
	Continuous ( $V_{GS} = 10\text{V}$ , $T_C = 25^\circ\text{C}$ , with $R_{\theta JA} = 43^\circ\text{C/W}$ )	31	A
	Pulsed	Figure 4	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)	947	mJ
$P_D$	Power Dissipation	254	W
	Derate above $25^\circ\text{C}$	1.7	$\text{W}/^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to +175	$^\circ\text{C}$

## Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case	0.59	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 2)	62	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-263, $1\text{in}^2$ copper pad area	43	$^\circ\text{C/W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB8860	FDB8860	TO-263AB	330mm	24mm	800units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 1\text{mA}$ , $V_{GS} = 0\text{V}$	30	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$ $V_{GS} = 0\text{V}$ $T_J = 150^\circ\text{C}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$	1	1.7	3	V
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = 80\text{A}$ , $V_{GS} = 10\text{V}$	-	1.6	2.3	m $\Omega$
		$I_D = 80\text{A}$ , $V_{GS} = 5\text{V}$	-	1.9	2.6	
		$I_D = 80\text{A}$ , $V_{GS} = 4.5\text{V}$	-	2.1	2.7	
		$I_D = 80\text{A}$ , $V_{GS} = 10\text{V}$ , $T_J = 175^\circ\text{C}$	-	2.5	3.6	

### Dynamic Characteristics

$C_{ISS}$	Input Capacitance	$V_{DS} = 15\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	-	9460	12585	pF	
$C_{OSS}$	Output Capacitance		-	1710	2275	pF	
$C_{RSS}$	Reverse Transfer Capacitance		-	1050	1575	pF	
$R_G$	Gate Resistance	$f = 1\text{MHz}$	-	1.8	-	$\Omega$	
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V	$V_{DD} = 15\text{V}$ $I_D = 80\text{A}$ $I_g = 1.0\text{mA}$	-	165	214	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0\text{V}$ to 5V		-	89	115	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 1V		-	9.1	12	nC
$Q_{gs}$	Gate to Source Gate Charge			-	26	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau			-	18	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge			-	33	-	nC

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

**Switching Characteristics**

$t_{(on)}$	Turn-On Time	$V_{DD} = 15\text{V}, I_D = 80\text{A}$ $V_{GS} = 5\text{V}, R_{GS} = 1\Omega$	-	-	340	ns
$t_{d(on)}$	Turn-On Delay Time		-	14	-	ns
$t_r$	Turn-On Rise Time		-	213	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	79	-	ns
$t_f$	Turn-Off Fall Time		-	49	-	ns
$t_{off}$	Turn-Off Time		-	-	192	ns

**Drain-Source Diode Characteristics**

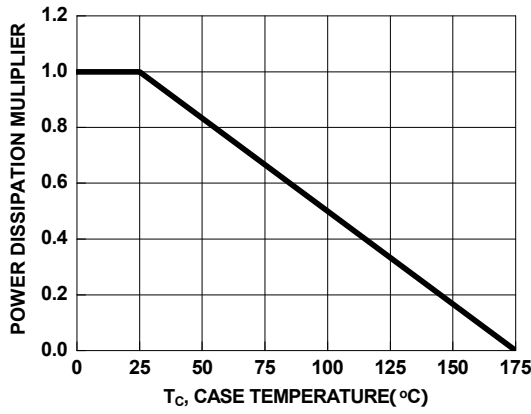
$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 80\text{A}$	-	-	1.25	V
		$I_{SD} = 40\text{A}$	-	-	1.0	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 80\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	43	ns
$Q_{rr}$	Reverse Recovery Charge	$I_{SD} = 80\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	29	nC

**Notes:**

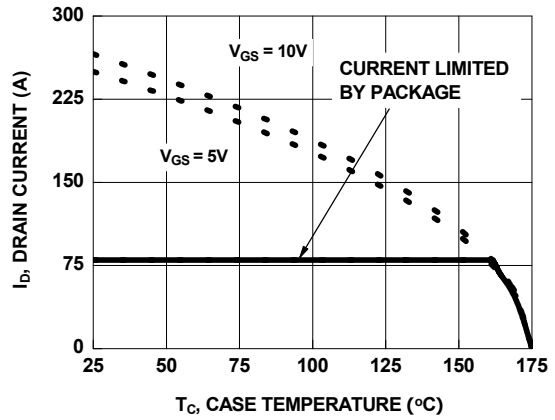
- 1: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.47\text{mH}$ ,  $I_{AS} = 64\text{A}$ ,  $V_{DD} = 30\text{V}$ ,  $V_{GS} = 10\text{V}$ .
- 2: Pulse width = 100s

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>  
 All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

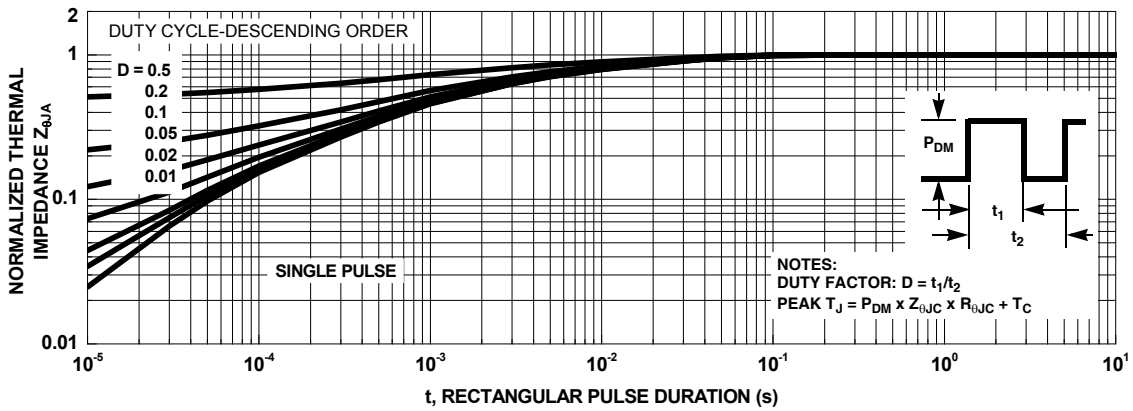
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



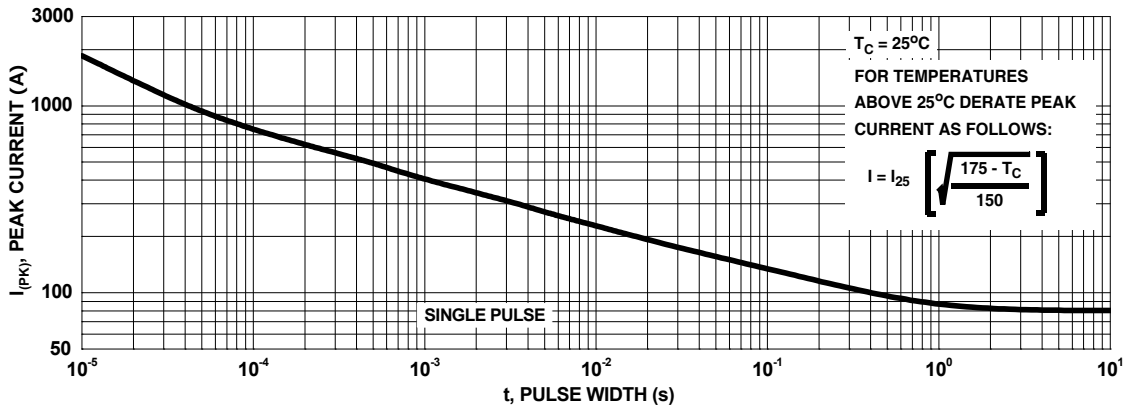
**Figure 1. Normalized Power Dissipation vs Case Temperature**



**Figure 2. Maximum Continuous Drain Current vs Case Temperature**

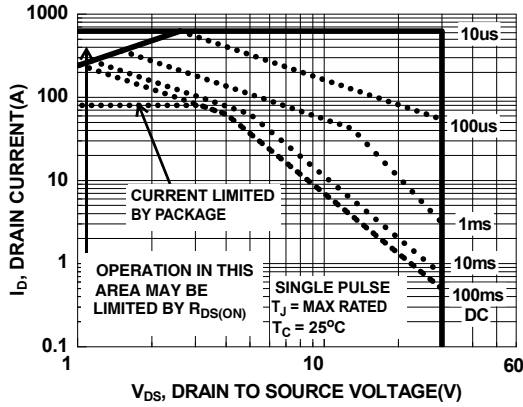


**Figure 3. Normalized Maximum Transient Thermal Impedance**

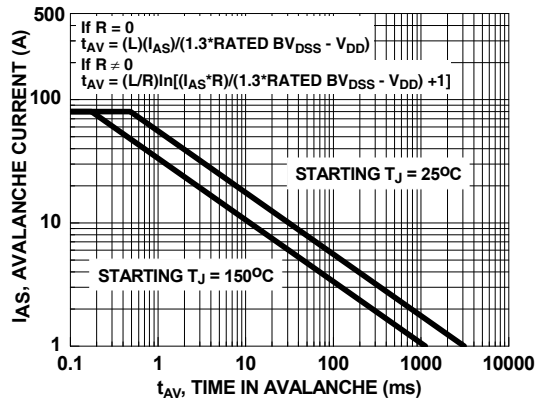


**Figure 4. Peak Current Capability**

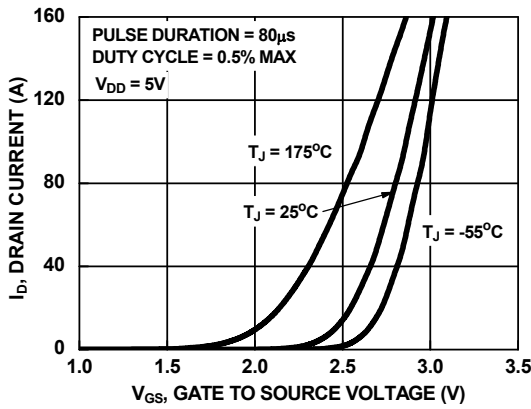
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



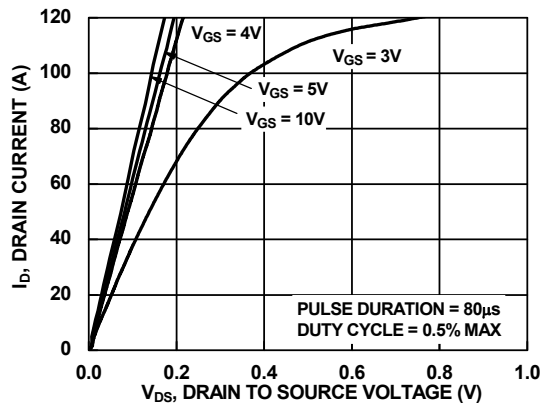
**Figure 5. Forward Bias Safe Operating Area**



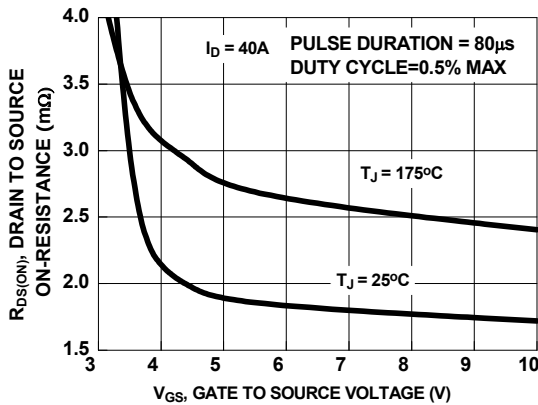
NOTE: Refer to Fairchild Application Notes AN7514 and AN7515  
**Figure 6. Unclamped Inductive Switching Capability**



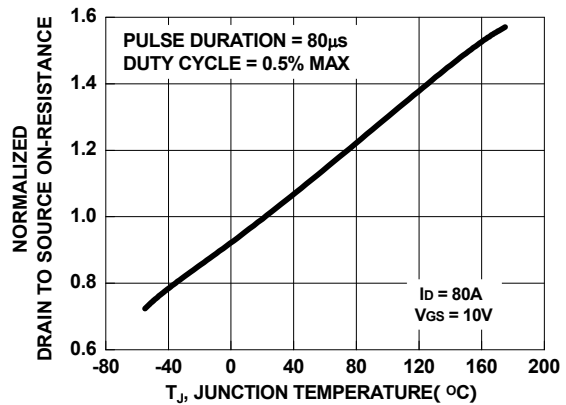
**Figure 7. Transfer Characteristics**



**Figure 8. Saturation Characteristics**

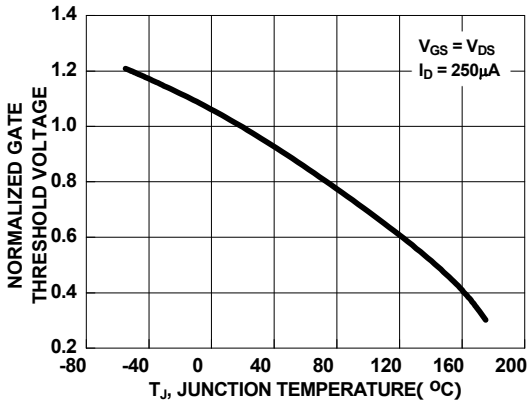


**Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage**

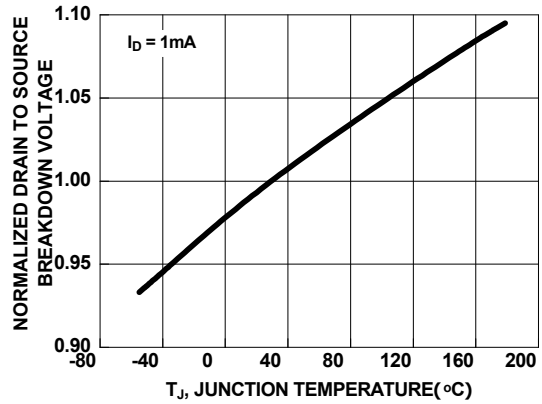


**Figure 10. Normalized Drain to Source On-Resistance vs Junction Temperature**

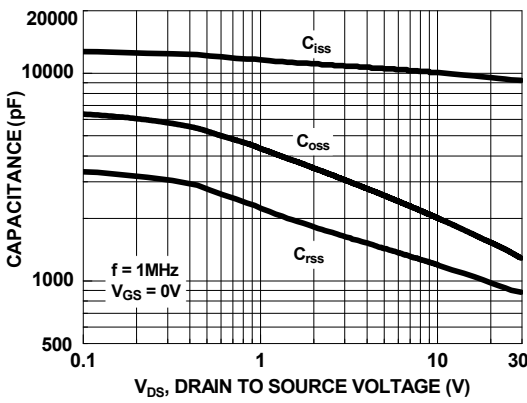
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



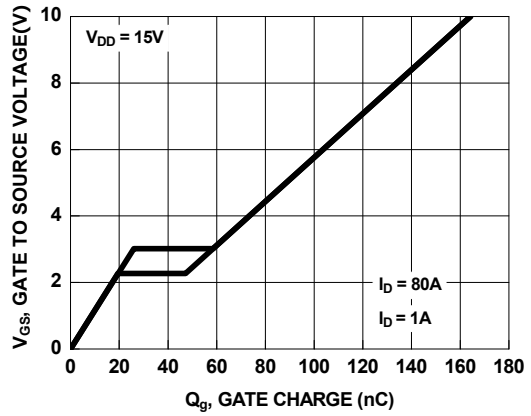
**Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature**



**Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**



**Figure 13. Capacitance vs Drain to Source Voltage**








**Figure 14. Gate Charge vs Gate to Source Voltage**



## TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACEx®	FPS™	PDP-SPM™	The Power Franchise®
Build it Now™	F-PFS™	Power-SPM™	the power franchise
CorePLUS™	FRFET®	PowerTrench®	TinyBoost™
CorePOWER™	Global Power ResourceSM	Programmable Active Droop™	TinyBuck™
CROSSVOLT™	Green FPS™	QFET®	TinyLogic®
CTL™	Green FPS™ e-Series™	QST™	TINYOPTO™
Current Transfer Logic™	GTO™	Quiet Series™	TinyPower™
EcoSPARK®	IntelliMAX™	RapidConfigure™	TinyPWM™
EfficientMax™	ISOPLANAR™	Saving our world 1mW at a time™	TinyWire™
EZSWITCH™ *	MegaBuck™	SmartMax™	µSerDes™
 ™	MICROCOUPLER™	SMART START™	
 ™	MicroFET™	SPM®	UHC®
Fairchild®	MicroPak™	STEALTH™	Ultra FRFET™
Fairchild Semiconductor®	MillerDrive™	SuperFET™	UniFET™
FACT Quiet Series™	MotionMax™	SuperSOT™-3	VCX™
FACT®	Motion-SPM™	SuperSOT™-6	VisualMax™
FAST®	OPTOLOGIC®	SuperSOT™-8	
FastvCore™	OPTOPLANAR®	SuperMOS™	
FlashWriter® *			

\* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I34