

# RJK0305DPB

## Silicon N Channel Power MOS FET Power Switching

REJ03G1353-0900

Rev.9.00

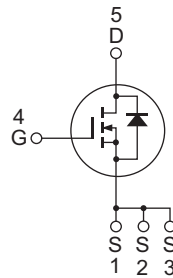
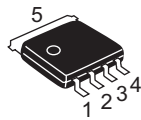
Apr 19, 2006

### Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance  
 $R_{DS(on)} = 6.7 \text{ m}\Omega$  typ. (at  $V_{GS} = 10 \text{ V}$ )

### Outline

RENESAS Package code: PTZZ0005DA-A  
(Package name: LFPAK)



1, 2, 3 Source  
4 Gate  
5 Drain

### Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	30	V
Gate to source voltage	$V_{GSS}$	+16/-12	V
Drain current	$I_D$	30	A
Drain peak current	$I_{D(pulse)}$ <sup>Note 1</sup>	120	A
Body-drain diode reverse drain current	$I_{DR}$	30	A
Avalanche current	$I_{AP}$ <sup>Note 2</sup>	10	A
Avalanche energy	$E_{AR}$ <sup>Note 2</sup>	10	mJ
Channel dissipation	$P_{ch}$ <sup>Note 3</sup>	45	W
Channel to Case Thermal Resistance	$\theta_{ch-C}$	2.78	$^\circ\text{C/W}$
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

- Notes: 1.  $PW \leq 10 \mu\text{s}$ , duty cycle  $\leq 1\%$   
 2. Value at  $T_{ch} = 25^\circ\text{C}$ ,  $R_g \geq 50 \Omega$   
 3.  $T_c = 25^\circ\text{C}$

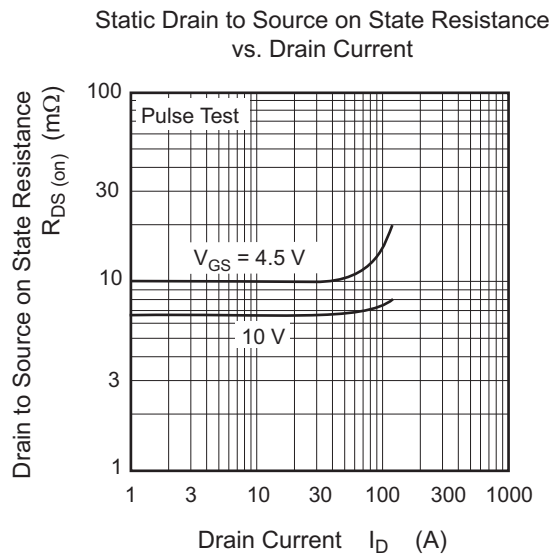
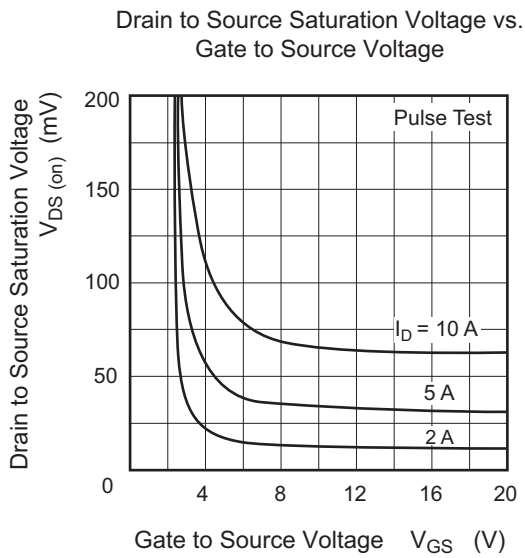
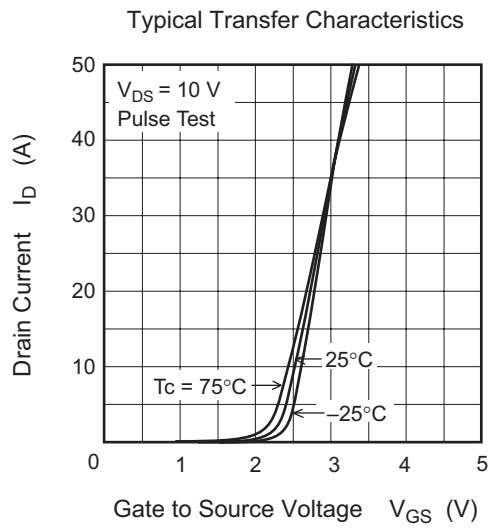
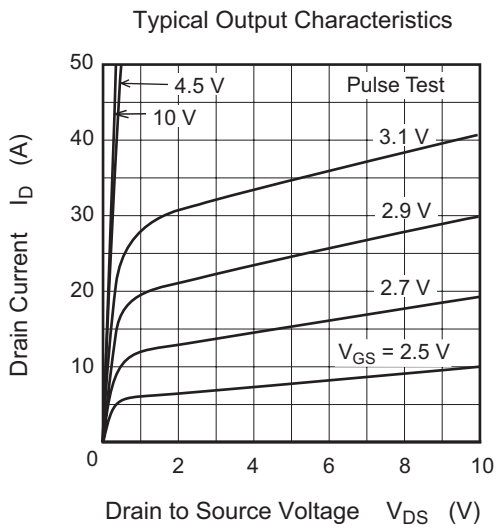
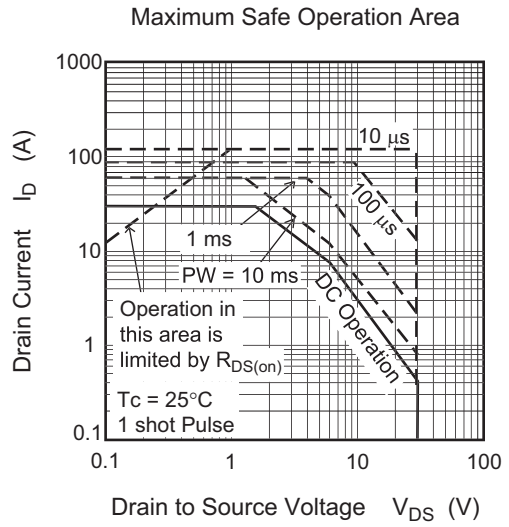
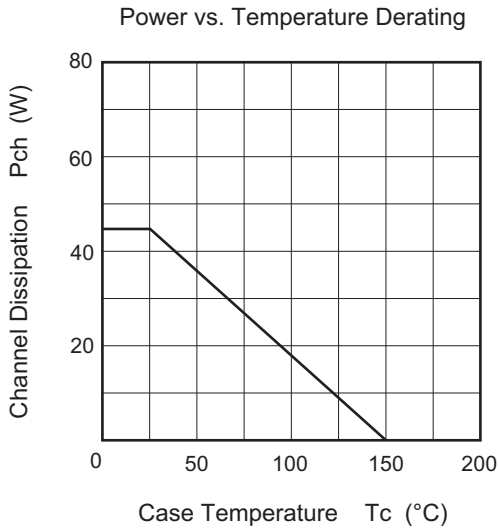
## Electrical Characteristics

(Ta = 25°C)

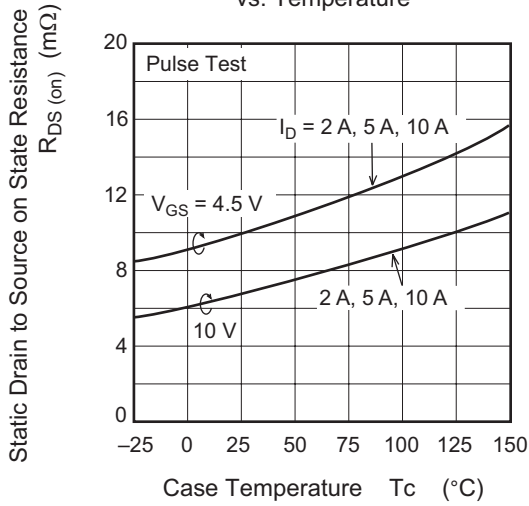
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = +16/-12 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 30 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	6.7	8.0	$\text{m}\Omega$	$I_D = 15 \text{ A}, V_{GS} = 10 \text{ V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	10	13	$\text{m}\Omega$	$I_D = 15 \text{ A}, V_{GS} = 4.5 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	—	45	—	S	$I_D = 15 \text{ A}, V_{DS} = 10 \text{ V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	1250	—	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz}$
Output capacitance	$C_{oss}$	—	530	—	pF	
Reverse transfer capacitance	$C_{rss}$	—	70	—	pF	
Gate Resistance	$R_g$	—	0.6	—	$\Omega$	
Total gate charge	$Q_g$	—	8	—	nC	$V_{DD} = 10 \text{ V}, V_{GS} = 4.5 \text{ V},$ $I_D = 30 \text{ A}$
Gate to source charge	$Q_{gs}$	—	3.6	—	nC	
Gate to drain charge	$Q_{gd}$	—	1.5	—	nC	
Turn-on delay time	$t_{d(on)}$	—	7.0	—	ns	$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A},$ $V_{DD} \cong 10 \text{ V}, R_L = 0.67 \Omega,$ $R_g = 4.7 \Omega$
Rise time	$t_r$	—	3.0	—	ns	
Turn-off delay time	$t_{d(off)}$	—	35	—	ns	
Fall time	$t_f$	—	3.0	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	0.85	1.08	V	$I_F = 30 \text{ A}, V_{GS} = 0$ <sup>Note4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	30	—	ns	$I_F = 30 \text{ A}, V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

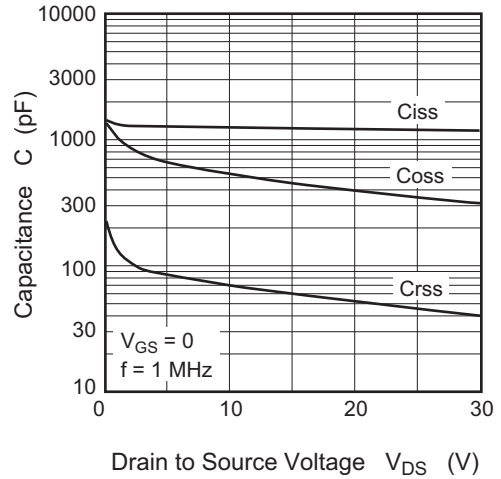
### Main Characteristics



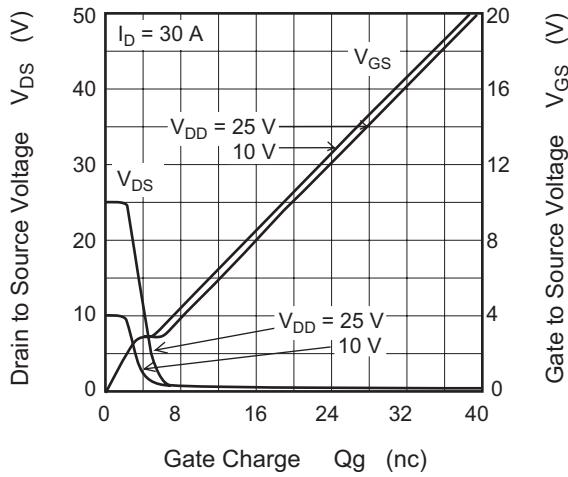
Static Drain to Source on State Resistance vs. Temperature



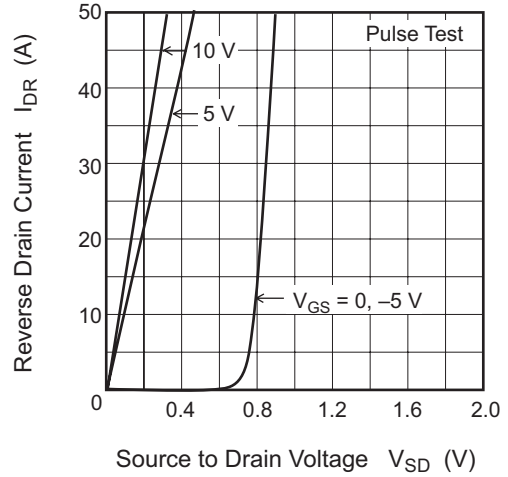
Typical Capacitance vs. Drain to Source Voltage



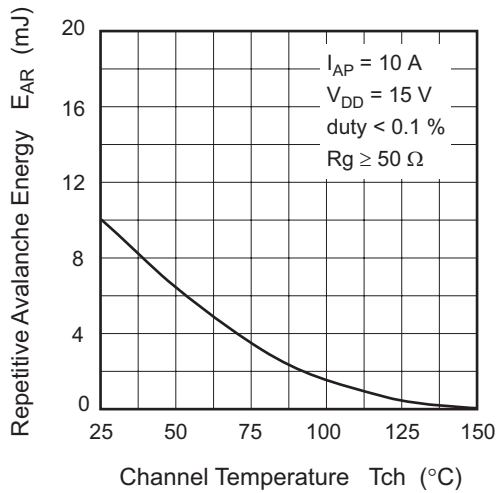
Dynamic Input Characteristics



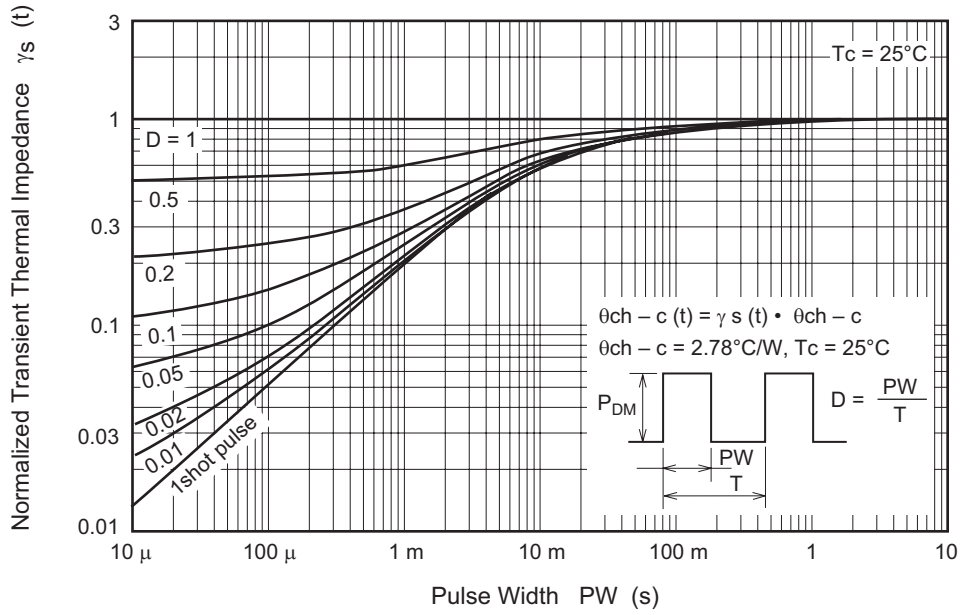
Reverse Drain Current vs. Source to Drain Voltage



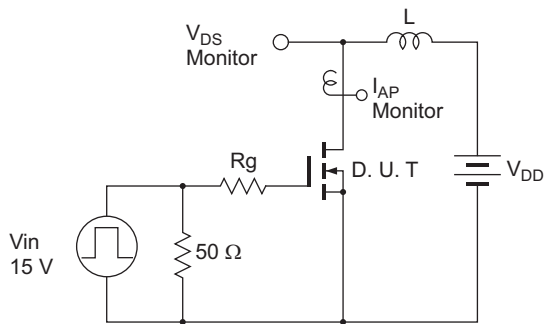
Maximum Avalanche Energy vs. Channel Temperature Derating



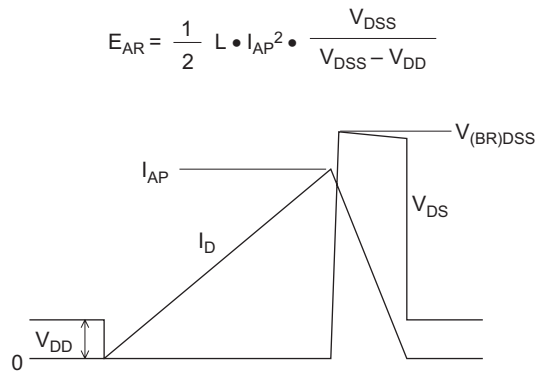
Normalized Transient Thermal Impedance vs. Pulse Width



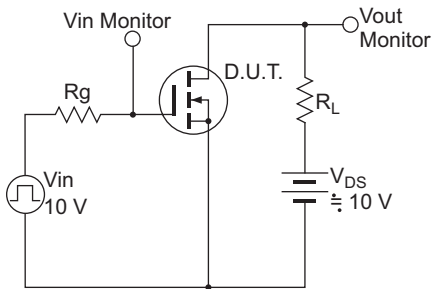
Avalanche Test Circuit



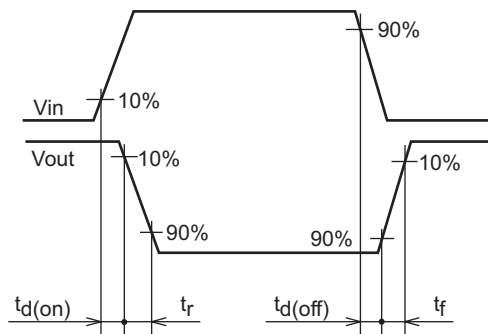
Avalanche Waveform



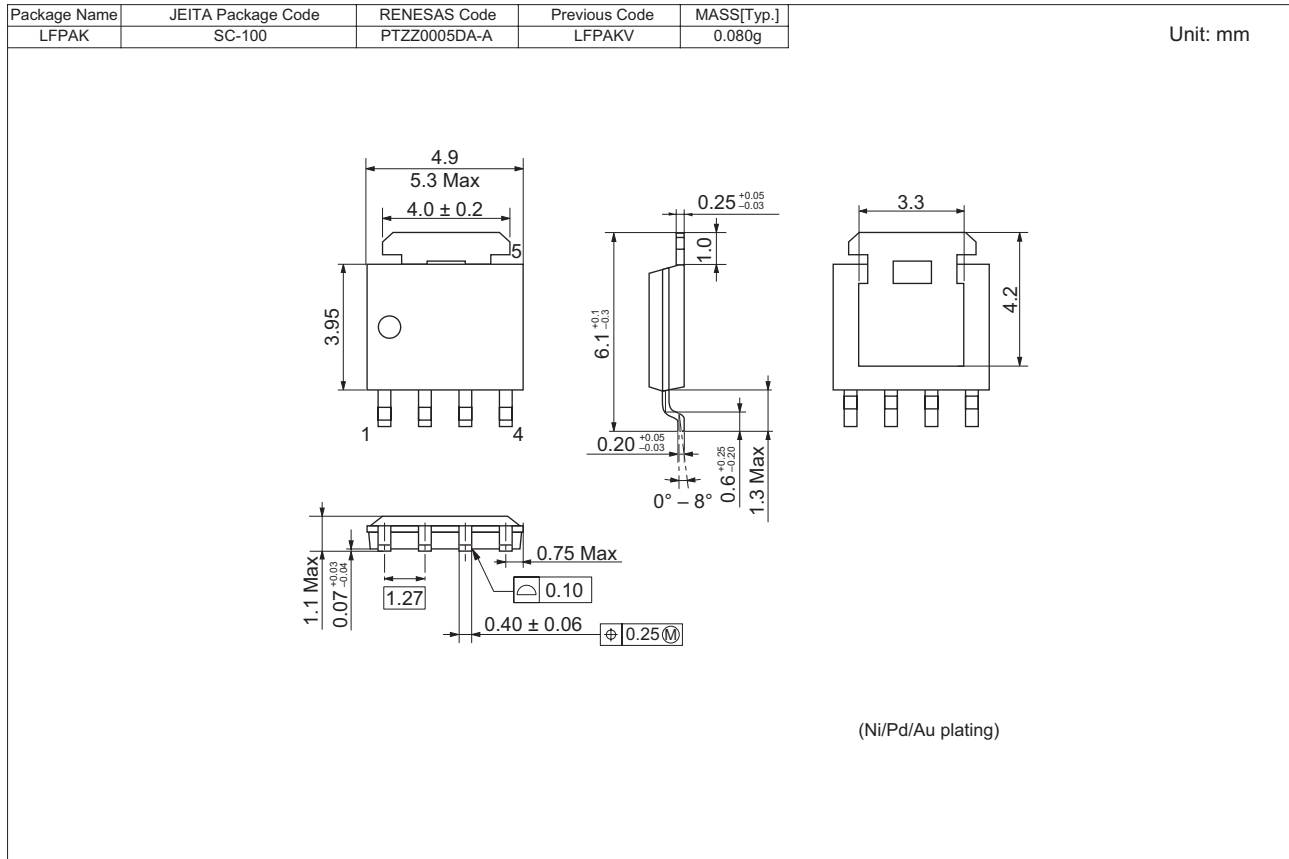
Switching Time Test Circuit



Switching Time Waveform



### Package Dimensions



### Ordering Information

Part Name	Quantity	Shipping Container
RJK0305DPB-00-J0	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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