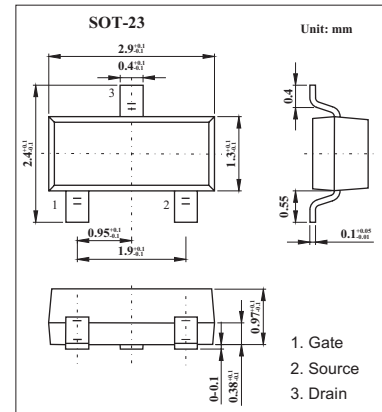
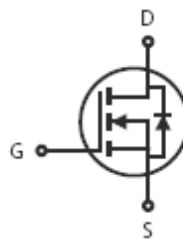


## N-Channel Enhancement Mode Field Effect Transistor

## KI2300(SI2300)

## ■ Features

- $V_{DS}=20V, R_{DS(ON)}=40m\Omega @ V_{GS}=4.5V, I_D=5.0A$
- $V_{DS}=20V, R_{DS(ON)}=60m\Omega @ V_{GS}=2.5V, I_D=4.0A$
- $V_{DS}=20V, R_{DS(ON)}=75m\Omega @ V_{GS}=1.8V, I_D=1.0A$

■ Absolute Maximum Ratings  $T_a = 25^\circ C$ 

Parameter	Symbol	Rating	Unit	
Drain-Source Voltage	$V_{DS}$	20	V	
Gate-Source Voltage	$V_{GS}$	$\pm 10$	V	
Drain-Current	$I_D$	-Continuous * $T_J=125^\circ C$	3.8	A
		-Pulsed	15	A
Power Dissipation *	$P_D$	1.25	W	
Thermal Resistance, Junction- to-Ambient	$R_{thJA}$	100	$^\circ C/W$	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ C$	

\* Surface Mounted on FR 4 Board,  $t \leq 10$  sec.

## KI2300(SI2300)

## ■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V			1	uA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage *	V <sub>GS(th)</sub>	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	0.6	0.78	1.5	V
Drain- Source on-state Resistance *	R <sub>DS(ON)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =5.0A		32	40	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =4.0A		50	60	mΩ
		V <sub>GS</sub> =1.8V, I <sub>D</sub> =1.0A		62	75	mΩ
On-State Drain Current *	I <sub>D(ON)</sub>	V <sub>DS</sub> =5V, V <sub>GS</sub> =4.5V	18			A
Forward Transconductance *	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =5A	5			S
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V, f = 1.0MHZ		888		pF
Output Capacitance	C <sub>OSS</sub>			144		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			115		pF
Turn-On Delay Time	t <sub>D(on)</sub>			31.8		ns
Rise Time	t <sub>r</sub>	V <sub>DD</sub> =10V, I <sub>D</sub> =1A, V <sub>GS</sub> =4.5V, R <sub>L</sub> =10Ω, R <sub>GEN</sub> =6Ω		14.5		ns
Turn-Off Delay Time	t <sub>D(off)</sub>			50.3		ns
Fall Time	t <sub>f</sub>			31.9		ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 3.5A, V <sub>GS</sub> = 4.5V		16.8		nC
Gate-Source Charge	Q <sub>gs</sub>			2.5		nC
Gate-Drain Charge	Q <sub>gd</sub>			5.4		nC
Drain-Source Diode Forward Current *	I <sub>S</sub>				1.25	A
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =1.25A		0.825	1.2	V

\* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%