

Silicon PNP Power Transistors

2SA765

DESCRIPTION

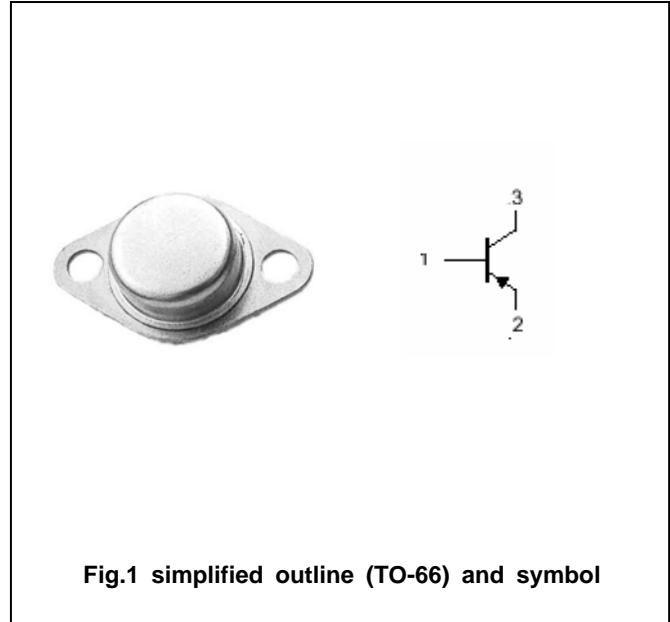
- With TO-66 package
- Low collector saturation voltage

APPLICATIONS

- Designed for general-purpose power amplifier and applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

Absolute maximum ratings($T_a = ^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-80	V
V_{CEO}	Collector-emitter voltage	Open base	-80	V
V_{EBO}	Emitter-base voltage	Open collector	-6	V
I_C	Collector current		-6	A
P_C	Collector power dissipation	$T_C = 25^\circ\text{C}$	40	W
T_j	Junction temperature		150	$^\circ\text{C}$
T_{stg}	Storage temperature		-55~150	$^\circ\text{C}$

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CHARACTERISTICS

T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-10mA ; I _B =0	-80			V
V _{(BR)CBO}	Collector-base breakdown voltage	I _C =-1mA ; I _E =0	-80			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-4A; I _B =-0.4A			-1.5	V
V _{BEsat}	Base-emitter saturation voltage	I _C =-4A; I _B =-0.4A			-2.0	V
I _{CBO}	Collector cut-off current	V _{CB} =-80V; I _E =0			-10	μ A
I _{EBO}	Emitter cut-off current	V _{EB} =-6V; I _C =0			-10	μ A
h _{FE}	DC current gain	I _C =-1A ; V _{CE} =-4V	50			
f _T	Transition frequency	I _C =-0.5A ; V _{CE} =-12V		10		MHz

PACKAGE OUTLINE

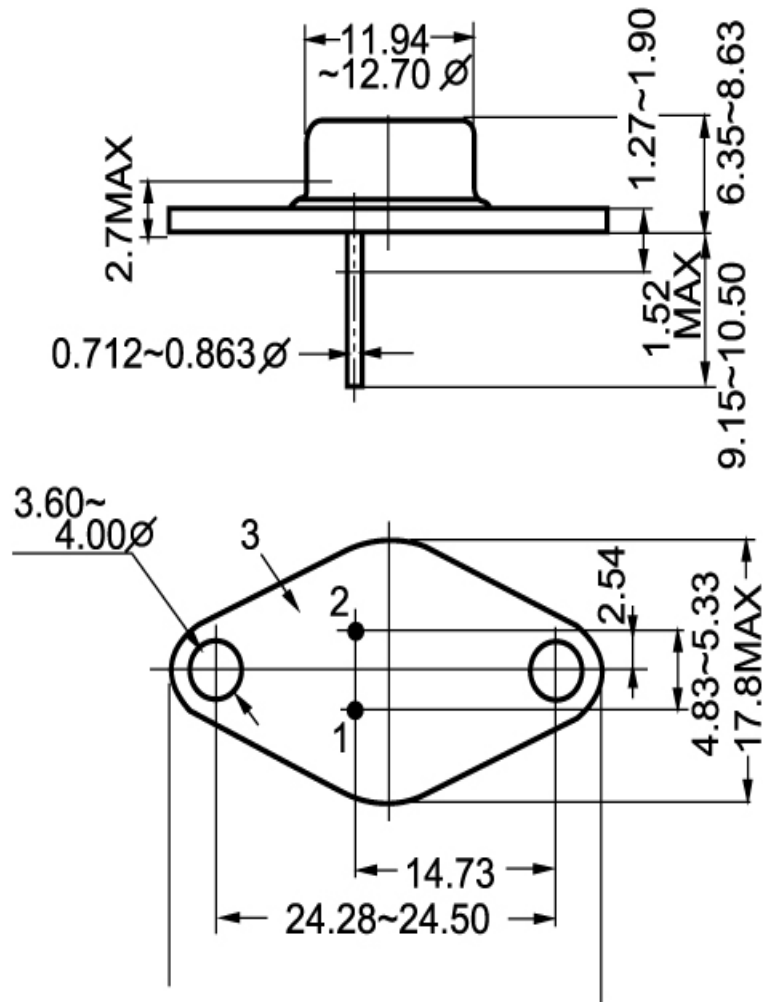


Fig.2 outline dimensions