SC660E

SMBus System Clock Buffer for Mobile Applications

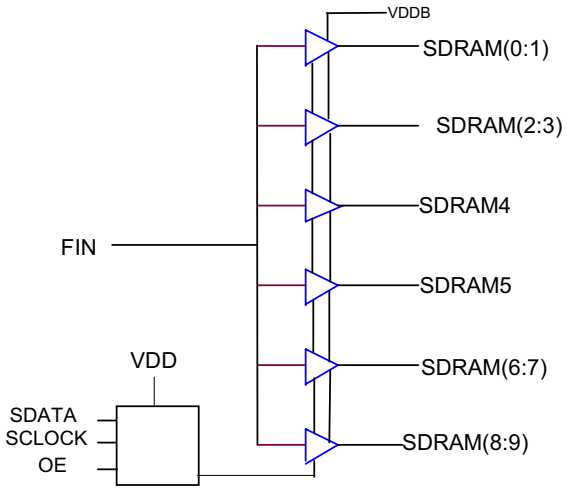
Features

- 10 output buffers for high clock fanout applications
- Each output can be internally disabled for EMI and power consumption reduction.
- Separate power supply for each group of 2 clock outputs for mixed voltage application.
- < 250ps skew between output clocks.
- 28-pin SSOP package for minimum board space
- Single output Tristate pin for testability

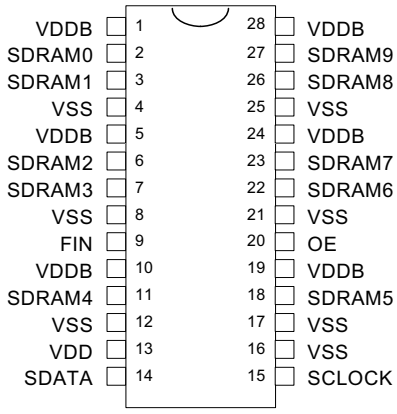
Product Description

The device is a high fanout system clock distributor. Its primary application is to create the large quantity of clocks needed to support a wide range of clock loads that are referenced to a single existing clock. Loads of up to 30 pF are supported. Primary application of this component is where long traces are used to transport clocks from their generating devices to their loads. The creation of EMI and the degradation of waveform rise and fall times is greatly reduced by running a single reference clock trace to this device and then using it to regenerate the clock that drives shorter traces by using the SC660 to generate the clocks at the target devices EMI is therefore minimized and board real estate is saved.

Block Diagram



Pin Configuration



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Pin Description

Pin No.	Name	PWR	I/O	Type	Description
9	FIN	-	I	PAD	This pin is connected to the input reference clock. This clock must be in the range of 10.0 to 100.0 Mhz.
2,3,6,7,11,18,22,23 ,26,27	Sdram(0:9)	VddB	O	BUF1	Low skew output clocks.
20	OE	-	I	PAD	Buffer Output Enable pin. This pin is low it is used to place all output clocks (CLK1:10) in a tri state condition. This feature facilitates in production board level testing to be easily implemented for the clocks that this device produces. Has internal pull-up resistor.
14	Sdata	Vdd	I/O	PAD	Serial Data for SMBus control interface. This pin receives data streams from the SMBus bus and outputs an acknowledge for valid data.
15	Sclock	Vdd	I	PAD	Serial Clock for SMBus control interface.
4, 8, 12, 16, 17, 21, 25	Vss		PWR	-	Ground pins for clock output buffers. These pins must be returned to the same potential to reduce output clock skew.
1, 5, 10, 19, 24, 28	VddB	-	PWR	-	Power for output clock buffers.
13	Vdd	-	PWR	-	Pin for device core logic.

Maximum Ratings[1]

Input Voltage Relative to VSS:.....VSS-0.3V

Input Voltage Relative to VDDQ or AVDD: ..... VDD+0.3V

Storage Temperature: .....-65°C to + 150°C

Operating Temperature:..... 0°C to +85°C

Maximum Power Supply:.....3.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

Note:

1. The voltage on any input or I/O pin cannot exceed the power pin during the power-up. Power supply sequencing is NOT required.

2-Wire SMBus Control Interface

The 2-wire control interface implements a write only slave interface. The device cannot be read back. Sub-addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled.

During normal data transfer, the SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit as the LSB. Data is transferred MSB first.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The device will not respond to any other control interface conditions. Previously set control registers are retained.

Serial Control Registers

Following the acknowledge of the Address Byte, two additional bytes must be sent:

1. "**Command Code** " byte, and
2. "**Byte Count**" byte.

Although the data (bits) in the command is considered "don't care"; it must be sent and will be acknowledged.

After the Command Code and the Byte Count have been acknowledged, the sequence (Byte 0, Byte 1, and Byte 2) described below will be valid and acknowledged.

Byte 0: Function Select Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	-	reserved
6	1	-	reserved
5	1	-	reserved
4	1	-	reserved
3	1	7	SDRAM3 (Active = 1, Forced low = 0)
2	1	6	SDRAM2 (Active = 1, Forced low = 0)
1	1	3	SDRAM1 (Active = 1, Forced low = 0)
0	1	2	SDRAM0 (Active = 1, Forced low = 0)

Byte 1: Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	27	SDRAM9 (Active = 1, Forced low = 0)
6	1	26	SDRAM8 (Active = 1, Forced low = 0)
5	1	23	SDRAM7 (Active = 1, Forced low = 0)
4	1	22	SDRAM6 (Active = 1, Forced low = 0)
3	1	-	reserved
2	1	-	reserved
1	1	-	reserved
0	1	-	reserved

Byte 2: Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	18	SDRAM5 (Active = 1, Forced low = 0)
6	1	11	SDRAM4 (Active = 1, Forced low = 0)
5	0	-	Not Used
4	0	-	Not Used
3	0	-	Not Used
2	0	-	Not Used
1	1	-	Not Used
0	1	-	Not Used

Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Units	Conditions
VIL	Input Low Voltage	-	-	0.8	Vdc	-
VIH	Input High Voltage	2.0	-	-	Vdc	-
IIL	Input Low Current	-66	-	-	µA	
IIH	Input High Current	-	-	66	µA	
VOL	Output Low Voltage IOL = 40mA	-	-	0.4	Vdc	All Outputs (see buffer spec)
VOH	Output High Voltage IOH = 30mA	2.4	-	-	Vdc	All Outputs Using 3.3V Power (see buffer spec)
Ioz	Tri-State leakage Current	-	-	10	µA	
Idd_{66}	Dynamic Supply Current	-	-	160	mA	Input frequency = 66 Mhz - All outputs on and at 30 pF load
Idd_{100}		-	-	220	mA	Input frequency 100 Mhz - All outputs on and at 30 pF load
Isdd	Static Supply Current	-	-	4	mA	All outputs disabled no input clock
ISC	Short Circuit Current	25	-	-	mA	1 output at a time - 30 seconds
TIR	Input Rise Time	2.4	-	-	nS	.8 to 2.4 volts
VDD = VDD1 thru VDD5 =3.3V ±5%, , TA = -40ºC to +85ºC						

Switching Characteristics

Parameter	Description	Min.	Typ.	Max.	Units	Conditions
	Output Duty Cycle	45	50	55	%	Measured at 1.5V (50/50 in)
-	Buffer out/out Skew All Buffer Outputs	-	-	250	pS	35 pF Load Measured at 1.5V
tSKEW	Buffer input to output Skew	2.0	4.0	5.0	nS	
tSKEW	Jitter Cycle to Cycle [2]			50	pS	@ 35 pF loading
TJCC	Jitter Absolute (Peak to Peak)[2]			150	pS	@ 35 pF loading
VDD = VDD1 thru VDD5 =3.3V ±5%, , TA = -40ºC to +85ºC						

TB40_ Type Buffer Characteristics (All Clock Outputs)

Parameter	Description	Min.	Typ.	Max.	Units	Conditions
IOH_{min}	Pull-Up Current Min	30	-	39	mA	Vout = VDD - .5V
IOH_{max}	Pull-Up Current Max	75	-	109	mA	Vout = 1.5V
IOL_{min}	Pull-Down Current Min	30	-	40	mA	Vout = 0.4
IOL_{max}	Pull-Down Current Max	75	-	103	mA	Vout = 1.2V
Zo	Dynamic Output Impedance	8	-	15	Ohms	66 and 100 MHz
TRF_{min}	Rise/Fall Time Min Between 0.4 V and 2.4 V	-	-	1.33	nS	30 pF Load
TRF_{max}	Rise/Fall Time Max Between 0.4 V and 2.4 V	-	-	1.33	nS	30 pF Load
VDD = VDD1 thru VDD5 =3.3V ±5%, , TA = -40ºC to +85ºC						

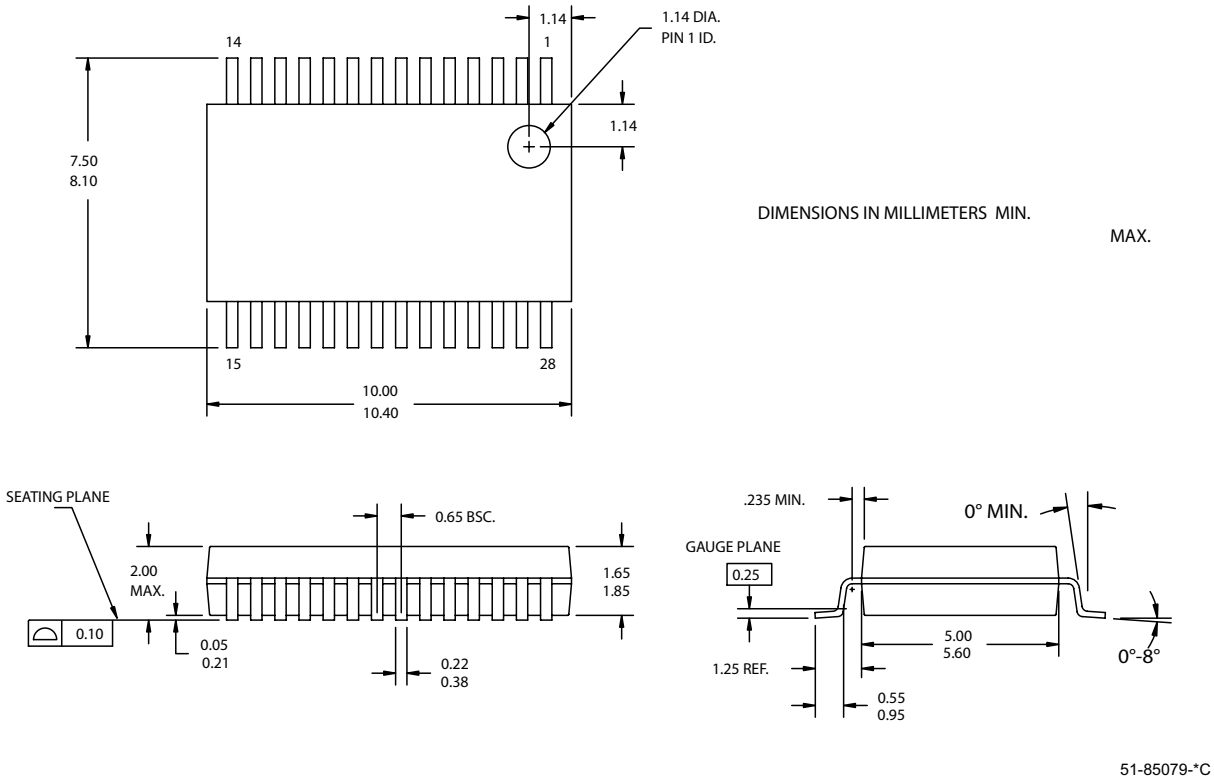
Note:
2. This jitter is additive to the input clock's jitter.

Ordering Information

Part Number	Package Type	Product Flow
SC660EYB	28-pin SSOP	Commercial,–40° to 85°C

Package Diagrams

28-Lead (5.3 mm) Shrunk Small Outline Package O28



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