Silicon NPN Power Transistors 2SD665

DESCRIPTION

·With TO-3 package
·Complement to type 2SB645
·High power dissipation

APPLICATIONS

·Power amplifier applications
·Power switching applications
·DC-DC converters

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings(Ta=□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	200	V
V_{CEO}	Collector-emitter voltage	Open base	200	V
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current		15	A
I_B	Base current		4	A
P_C	Collector power dissipation	T_C=25□	150	W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-55~150	□

Silicon NPN Power Transistors 2SD665

CHARACTERISTICS

Tj=25□ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C=25mA ;I_B=0	200			V
V_{CEsat}	Collector-emitter saturation voltage	I_C=10A; I_B=1A			2.0	V
V_{BEsat}	Base-emitter saturation voltage	I_C=10A; I_B=1A			2.5	V
I_{CBO}	Collector cut-off current	V_{CB}=200V; I_E=0			0.1	mA
I_{EBO}	Emitter cut-off current	V_{EB}=5V; I_C=0			0.1	mA
h_{FE}	DC current gain	I_C=1A ; V_{CE}=5V	40		140	
C_{OB}	Output capacitance	I_E=0 ; V_{CB}=10V;f=1.0MHz		300		pF
f_T	Transition frequency	I_C=1A ; V_{CE}=5V		15		MHz

◆ **h_{FE} Classifications**

O	R
40-80	70-140

PACKAGE OUTLINE

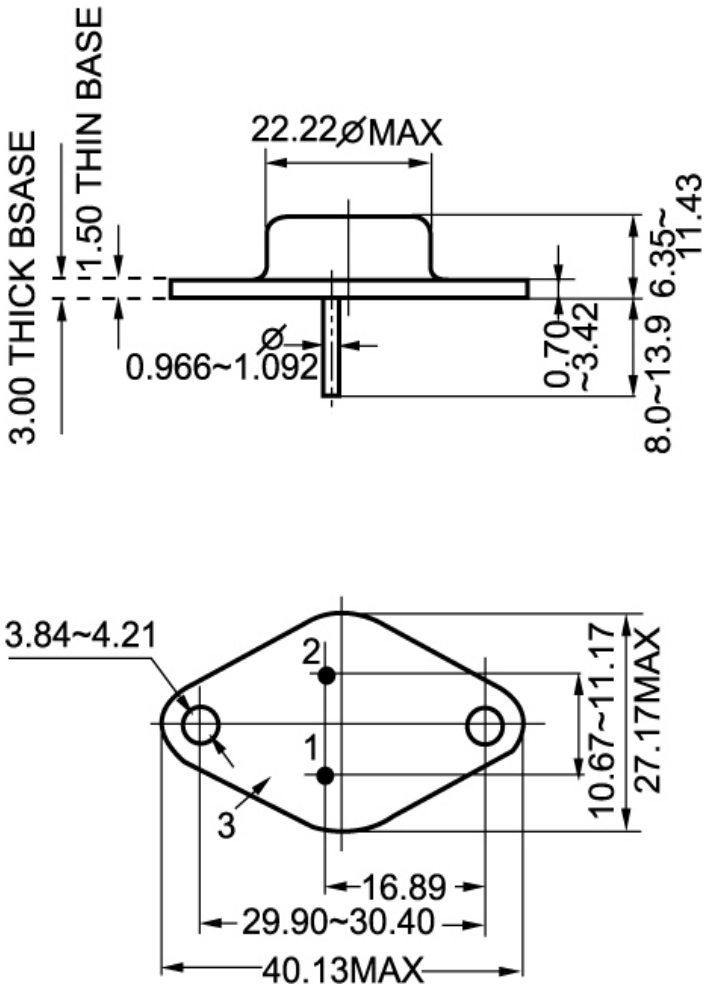

Fig.2 outline dimensions (unindicated tolerance:±0.1mm)